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0.5 V and 0.43 pJ/bit Capacitive Sensor Interface for Passive Wireless Sensor Systems

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Abstract: This paper presents an ultra low-power and low-voltage pulse-width modulation based ratiometric capacitive sensor interface. The interface was designed and fabricated in a standard 90 nm CMOS 1P9M technology. The measurements show an effective resolution of 10 bits using 0.5 V of supply voltage. The active occupied area is only 0.0045 mm^2 and the Figure of Merit (FOM), which takes into account the energy required per conversion bit, is 0.43 pJ/bit. Furthermore, the results show low sensitivity to PVT variations due to the proposed ratiometric architecture. In addition, the sensor interface was connected to a commercial pressure transducer and the measurements of the resulting complete pressure sensor show a FOM of 0.226 pJ/bit with an effective linear resolution of 7.64 bits. The results validate the use of the proposed interface as part of a pressure sensor, and its low-power and low-voltage characteristics make it suitable for wireless sensor networks and low power consumer electronics.

Keywords: capacitive-sensor interface; low-power sensor interface; period modulation; pressure sensor

1. Introduction

Sensor usage is undergoing a great growth, due in particular to its inclusion in new generation wireless sensor networks (WSN) and consumer electronics. The main challenge to their implementation is reducing the power consumption of the sensor nodes, which limits the battery life of the sensor

devices [1]. In the specific case of passive WSN, a reduction in sensor power consumption together with low supply voltages that enable the use of high efficiency power harvesting modules [2] would make it possible to increase the communication range of the sensors.

Therefore, there is great interest in the development of low-power and low-voltage sensor systems. With this objective, novel architectures based on capacitive transducers and time to digital conversion have been reported recently [3–5]. In these novel architectures, capacitive transducers are preferred over resistive transducers due to their high relative sensitivity, low temperature dependence and virtually negligible power consumption [6]. These novel sensor interfaces are based on period modulation (PM) or pulse-width modulation (PWM) instead of using a signal conditioning stage and analog-to-digital converters (ADC). This way, the capacitive value of the transducer modulates the width/period of a pulse generated through a capacitance-to-time converter such an oscillator or similar. The transducer capacitance dependent pulses are subsequently digitized using a simple time-to-digital converter (*i.e.*, a digital counter). These interfaces are quite flexible and the resolution can be easily traded for measurement time by counting the duration of multiple output periods [4]. In addition, they may have very low power-consumption and active area [3–5] in comparison with traditional architectures.

This work describes an energy-efficient and ultra low-power, low-voltage PWM based capacitive-sensor interface. The paper is organized as follows. In Section 2, the operating principle and design considerations of the interface are presented. Section 3 discusses the circuit implementation and the experimental results. Finally, the paper is concluded in Section 4.

2. Operating Principle

In this section the architecture of the proposed interface and the key points of the design are discussed.

2.1. Architecture

The architecture of the proposed interface, presented in Figure 1, is based on a relaxation oscillator formed by an inverter (INV), two capacitors (C_{MEMS} and C_{REF}), a constant current source (i_{REF}) and two switches (SW_1 and SW_2). In addition to the C_{MEMS} capacitor that represents the capacitive sensor transducer, the interface also measures the value of an integrated C_{REF} capacitor. This allows ratiometric measurements of C_{MEMS} against the C_{REF}, simplifying the sensor calibration and making it robust against PVTs.

As Figure 2 shows, the capacitance to time conversion starts when the discharge signal ("Discharge") goes from "0" to "1". At this moment, node "V_1" is shortcut to ground through switch "SW_2". Switch "SW_1", which is controlled by the "Mode" signal, selects which capacitor is discharged. When the "Discharge" signal falls to "0", "SW_2" is opened and the conversion starts. At that moment, the capacitor selected by the "Mode" signal starts charging with the current i_{REF} and voltage "V_1" rises. When voltage "V_1" is above the inverter switching point (V_{SP}), "V_2" goes down and stays down until a discharge pulse arrives again to the "SW_2" switch.
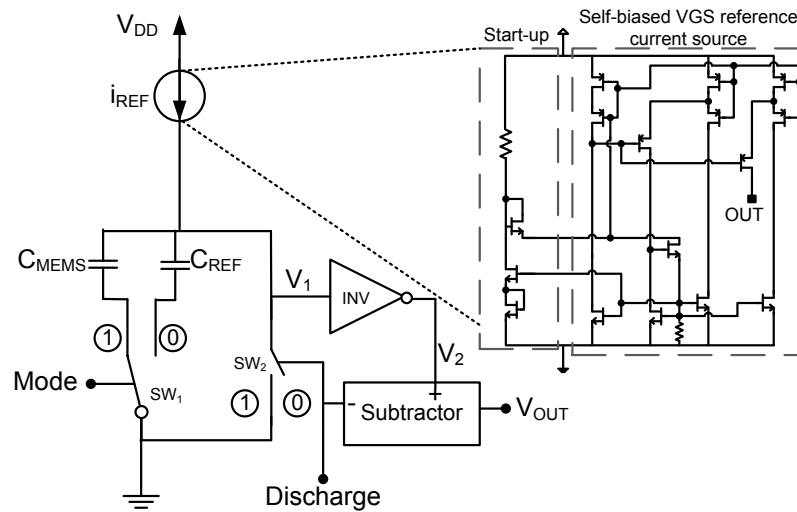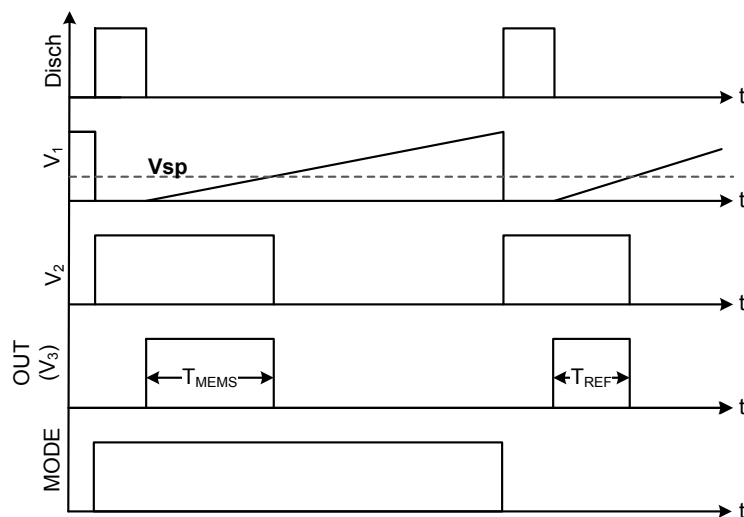
Figure 1. Proposed architecture.

Figure 2. Signal diagram during a measurement.

The output of the capacitance-to-time conversion (T) is the length of the pulse that results from subtracting the "Discharge" signal from the "V_2" signal. This length is defined by the time required by "V_1" to rise from "0" to "V_{SP}" and it is obtained by using the capacitance charging formula presented in Equation (1). Equation (2) shows the pulse width (T) obtained after rearranging and solving the equation for this specific case.

$$i_{\text{REF}} = C \frac{dV_1}{dt} \tag{1}$$

$$T = t_{(V_1=V_{SP})} - t_{(V_1=0)} = \frac{C * V_{SP}}{i_{\text{REF}}} \tag{2}$$

The capacitance-to-time conversion of both capacitors is done in series and controlled by the "Mode" signal. As the conversion of both capacitors is done using the same current source and comparator, the effect of PVT errors in both generated pulses is similar and the size of the circuit is reduced. Once both C_{MEMS} and C_{REF} have been converted into T_{MEMS} and T_{REF}, the time-to-digital conversion is performed using

two counters and a fast oscillator with frequency F_{OSC} to sample the length of both pulses. The digitalized value for C_{MEMS} and C_{REF} are described by Equations (3) and (4).

$$D_{MEMS} = \frac{C_{MEMS} F_{OSC} V_{SP}}{i_{REF}} \tag{3}$$

$$D_{REF} = \frac{C_{REF} F_{OSC} V_{SP}}{i_{REF}} \tag{4}$$

The main advantage of this architecture is that as D_{MEMS} and D_{REF} are generated and sampled using the same current source, inverter and oscillator, the average values of V_{SP}, i_{REF} and oscillator frequency can be considered as a first order approximation to be equal during both pulses generation. Moreover, if the pulses are generated one right after the other, the effect of PVT variations are equivalent and proportional in D_{MEMS} and D_{REF}. Therefore, as Equation (5) shows, if a ratiometric system is used to measure C_{MEMS} against C_{REF}, the ratio between both measured pulse lengths (D_{MEMS} and D_{REF}) is the ratio between the capacitor values and does not depend on any other design parameter or their PVT variations. Therefore, as C_{REF} has a constant value and the value of C_{MEMS} depends on the physical magnitude to be measured through the transducer, this magnitude can be easily estimated from Equation (5).

$$R = \frac{D_{MEMS}}{D_{REF}} = \frac{C_{MEMS}}{C_{REF}} \tag{5}$$

2.2. PVT Variations

As Equation (5) shows, the output of the interface depends uniquely in the ratio between two capacitors, C_{REF} and C_{MEMS}. As C_{MEMS} is the value to be estimated with the interface, the PVT variations that need to be compensated for at the output are C_{REF} variations.

As far as process variations goes, a single-point calibration is enough to determine C_{REF} nominal value and compensate for its effects in the output ratio.

First order effects caused by voltage variations, current variations and inverter threshold variations, are compensated for at architecture level due to the ratiometric output and the current source that isolates the capacitor from the voltage supply.

Last but not least, temperature variations depend on the implemented C_{REF} capacitor and its characteristics. Integrated capacitors have small-medium temperature coefficient and in some applications its effect could be negligible. However, in high temperature range or high accuracy applications, a temperature calibration may be necessary to achieve the desired accuracy in the measurements.

2.3. Parasitic Capacitance

The parasitic capacitance at node "V_1" affects directly to Equation (5) and might introduce offset and slope deviations. However, it was observed that after parasitic post-layout extraction this parasitic capacitor was in the order of femto-farads, small in comparison with C_{REF} and C_{MEMS} that are around 10 pF. Also test set-up parasitic capacitance was observed to be very small when compared to C_{REF} and C_{MEMS}. Therefore, its effect in the equation is not critical and may be neglected in many applications or compensated for partially with the previously mentioned single-point process calibration. In any case,

the parasitic capacitor will be constant during the operation of the interface. This means that, it does not affect to the linearity of the interface. Therefore, in the worst case, when parasitic capacitance is comparable to C_{REF} and C_{MEMS}, a traditional two-point process calibration would be enough to totally compensate for its effects, even in most critical applications. In the characterization of the interface, no influence of this parasitic capacitor was observed.

2.4. Resolution

In order to obtain a resolution of N bits, the difference in the MEMS counter output (D_{MEMS}) between the minimum value of C_{MEMS} (C_{ZS}) and the maximum value of C_{MEMS} (C_{FS}) conversion should be greater than 2^N. Therefore, the sampling oscillator period (T_{OSC}) must satisfy the condition shown in Equation (6), where $T_{MEMS}(C_{FS})$ and $T_{MEMS}(C_{ZS})$ refer to the pulse width correspondent to C_{FS} and C_{ZS} conversion respectively; and ΔT_{MEMS} refers to the variation range of T_{MEMS}.

$$T_{OSC} < \frac{T_{MEMS}(C_{FS}) - T_{MEMS}(C_{ZS})}{2^N} = \frac{\Delta T_{MEMS}}{2^N} \tag{6}$$

2.5. Current Source

The current source is an important block of the design as the minimum supply voltage is limited by this block. Taking into account the importance of working at low operation voltages in wireless passive applications to increase harvesting efficiency [2], it is critical to design the current source for very low voltage operation. As shown in Figure 1, a self-biased VGS reference current source with a current mirroring technique based on [7] to ensure very high output impedance when working at voltages as low as 0.5 V has been implemented.

2.6. Model Validation

The ratiometric output presented in Equation (5) is based on the assumptions that inverter and subtractor delay is neglectable in comparison with T_{MEMS} and that V_{SP} is constant during the conversion of two subsequent pulses with input capacitance in the range between C_{ZS} and C_{FS}. In order to check that these assumptions are correct and to validate Equation (5) the following conditions must be met.

2.6.1. Delay

The most intuitive criteria for neglecting the inverter and subtractor cumulative delay effect at the output of the capacitance-to-time converter is to assure that it is below the sensitivity (LSB) of the time-to-digital converter. As detailed in section III, in order to obtain a resolution of 10 bits for the implemented MEMS transducer a fast oscillator of 75.6 MHz is necessary. Therefore, if the maximum delay for every fabrication corner and supply voltage is below its period (13.22 ns), this effect could be neglected. Figure 3 shows the post-layout simulated cumulative delay for different supply voltages and fabrication corners. As shown, for supply voltages of 0.5 V or higher the effect of the delay is below 1 LSB, and therefore could be considered negligible.
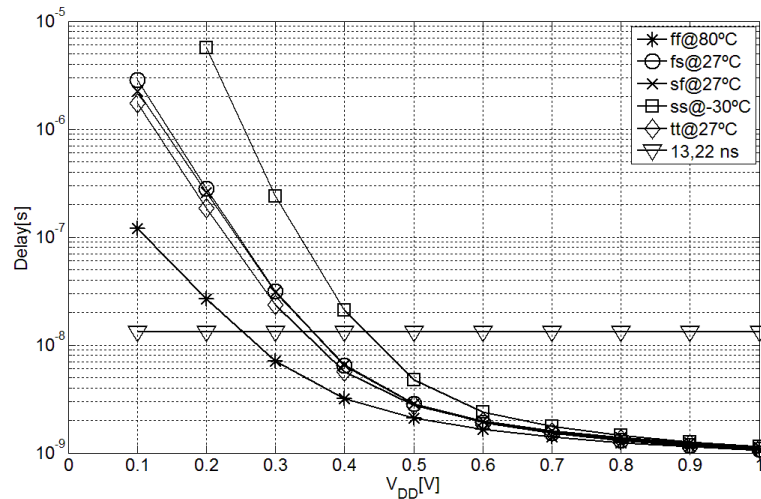
Figure 3. Cumulative inverter and subtractor delay in different fabrication corners with different supply voltages.

2.6.2. Switching Voltage

Ideally, the switching point (V_{SP}) of the inverter is constant and equal to $V_{DD}/2$. However, it usually changes when the input voltage slope ($\alpha = \dfrac{dV}{dT}$) changes.

$$\alpha = \frac{dV}{dT} = \frac{i_{REF}}{C} \tag{7}$$

In this design, because α depends on C and i_{REF} (Equation (7), V_{SP} may change during different C_{MEMS} measurements, adding nonlinearities to the measurements. Equations (8) and (9) show T_{MEMS} generated as result of C_{ZS} and C_{FS} conversion with constant V_{SP}. The only difference between both equations is the k factor between capacitor values ($C_{FS} = C_{ZS} * k$).

$$T_{MEMS}(C_{ZS}) = \frac{C_{ZS} * V_{SP}}{i_{REF}} = \frac{V_{SP}}{\alpha} \tag{8}$$

$$T_{MEMS}(C_{FS}) = \frac{C_{FS} * V_{SP}}{i_{REF}} = k\frac{C_{ZS} * V_{SP}}{i_{REF}} = k\frac{V_{SP}}{\alpha} \tag{9}$$

Equations (10) and (11) show the same expressions but include the influence of V_{SP} on the output time of the converter when measuring C_{MEMS}. In order to ensure that this variation doesn't affect the linearity of the interface, the design needs to meet the condition expressed in Equation (12), where the influence of V_{SP} on the output time is less than one LSB.

$$T'_{MEMS}(C_{ZS}) = \frac{C_{ZS} * V_{SP\_ZS}}{i_{REF}} = \frac{V_{SP\_ZS}}{\alpha} \tag{10}$$

$$T'_{MEMS}(C_{FS}) = \frac{C_{FS} * V_{SP\_FS}}{i_{REF}} = k\frac{V_{SP\_FS}}{\alpha} \tag{11}$$

$$|T'_{MEMS}(C_{FS}) - k * T'_{MEMS}(C_{ZS})| < \frac{T'_{MEMS}(C_{ZS})(k-1)}{2^N} \tag{12}$$

Substituting Equations (10) and (11) in Equation (12) and developing the expression, the maximum allowable V_{SP} variation is obtained in Equation (13), as a function of the k and the number of bits of the interface.

$$|V_{SP\_FS} - V_{SP\_ZS}| < \frac{V_{SP\_ZS}(k+1)}{k*2^N} \tag{13}$$

Equation (13) has been validated at simulation level with N equal to 10 and K, C_{ZS} and C_{FS} corresponding to a commercial capacitive pressure transducer [8]. The results show that as long as $T_{MEMS}(C_{ZS})$ is bigger than 20.44 μs, Equation (13) is satisfied and the V_{SP} variations effect could be neglected as its influence on the capacitance-to-time converter is below one LSB.

3. Experimental Section

The capacitive sensor interface based on capacitance-to-time conversion was fabricated in standard 90 nm CMOS 1P9M technology. Figure 4 shows the layout and a microphotograph of the fabricated chip, with an active area of 0.045 mm^2. In the layout the different parts of the design are identified: (1) Supply-to-ground capacitors, (2) capacitance-to-time converter, (3) output buffer and (4) integrated C_{REF} capacitor. The time to digital conversion has not been included in this implementation in order to compare the design with the state of the art (Table 1).

The design has been optimized to work with a commercial capacitive pressure transducer [8] that acts as C_{MEMS}. The transducer shows an output variation between 7.82 pF and 11.79 pF with an input range between 30 kPa and 120 kPa. Regarding C_{REF}, it is a standard integrated MIM cap with a value of 9 pF.
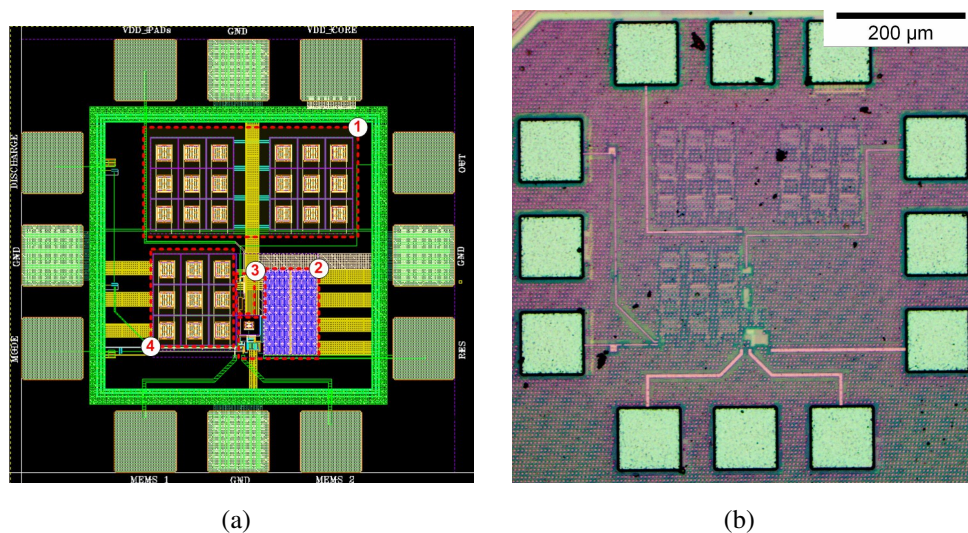

(a) (b)

Figure 4. (**a**) Layout plot and (**b**) photograph of the chip.

3.1. Results

3.1.1. Capacitance-to-Time Conversion

Five dies were connected to different capacitors with a supply voltage of 0.5 V to check the operating principle of the interface. Figure 5 shows the evolution of T_{MEMS} against C_{MEMS}.

This graph demonstrates the interface conversion capability within the 4.5 pF to 15.2 pF capacitance dynamic range. However, the interface has been optimized to work with [8] commercial pressure transducer, which has a capacitance range between 7.82 pF and 11.79 pF. The minimum $\triangle T_{MEMS}$ or dynamic range corresponding to this capacitance range is 13.54 μs, so according to Equation (6) a fast oscillator of 75.6 MHz will be sufficient in the following time-to-digital converter to ensure a 10 bits resolution. According to our measurements, inside the operation range of [8] the sensor performance in terms of noise effect, average current consumption and minimum supply voltage is homogeneous.

The fabrication process variations are the cause of the interchip offset variation presented in Figure 5 due to changes in i_{REF} and transistor speed. The same effect was reported in T_{REF} measurements. This way, when C_{MEMS} is equal to 12.1 pF, the measured variations in the pulse length between dies are $\pm 8.53\%$ in the case of T_{MEMS} and $\pm 8.18\%$ in the case of T_{REF}.
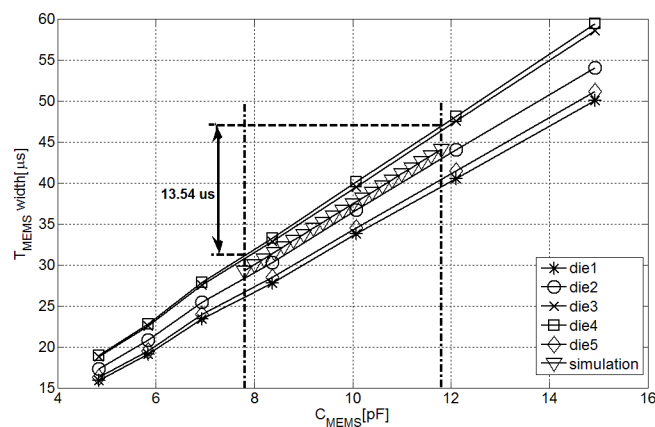

Figure 5. Measurement-pulse length in the fabricated interfaces with different C_{MEMS}.

According to the operating principle of the architecture, the differences due to i_{REF} and transistors parameter variations should be compensated when the ratio between T_{MEMS} and T_{REF} is applied. Figure 6 shows this premise. Without any calibration the output ratio compensates these effects and the interchip variation of the measurements is reduced to $\pm 0.98\%$, which is caused by C_{REF} process variations and can be compensated by a single-point calibration.
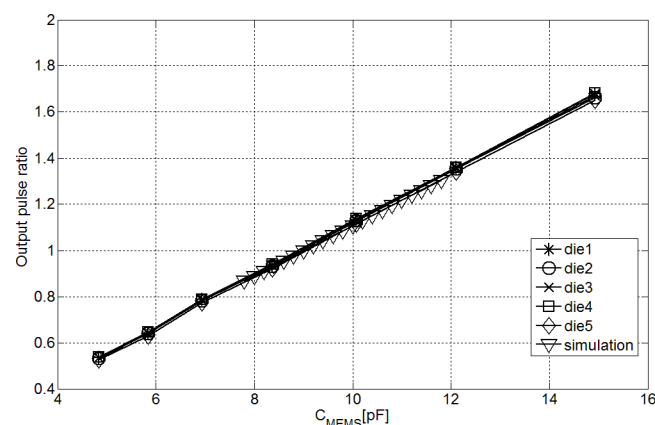

Figure 6. Output ratio in the fabricated interfaces with different C_{MEMS}.

In order to evaluate the supply voltage variation effect in the measurements, first, the static current consumption of the interface has been evaluated with different supply voltages. As Figure 7 shows, the DC current is stable with voltages above 0.4 V, once that the minimum supply voltage of the current source is reached. Considering that minimum supply voltage is one of the desired characteristics for the interface, it has been set at 0.5 V, leaving a margin of 100 mV from the current source minimum.
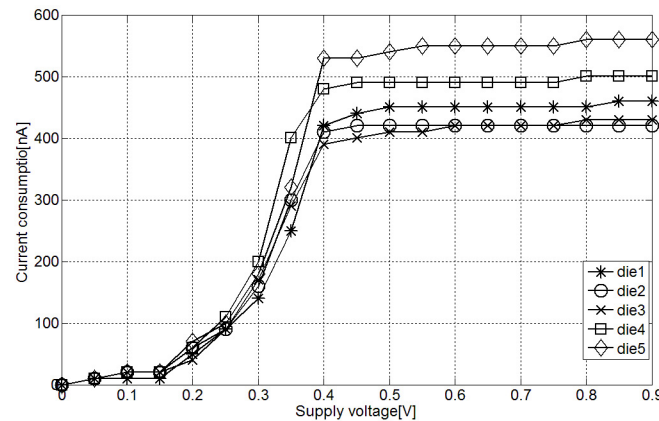

Figure 7. Measured DC current consumption at different supply voltages.

In Figure 8 the effect of voltage variations in the interface output is evaluated. The ratiometric architecture and high output impedance current source compensates for first order voltage variation effects in the measurement, reporting a variation around $\pm 0.1\%$ in the output within 0.4 V to 0.6 V supply voltage range.
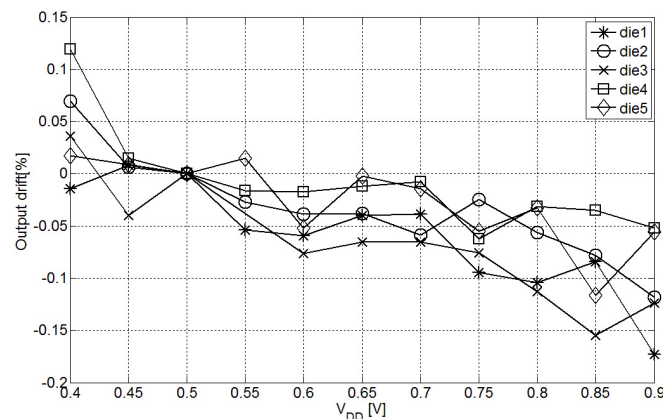

Figure 8. Supply voltage variation effect in the output ratio.

Regarding the measurement time, the system requires a maximum time of 47 μs to convert C_{MEMS} and 35.4 μs to convert C_{REF}. The discharge pulses are set to 10 μs each, so the complete measuring time required by the interface is 102.4 μs with a measured average current consumption of 0.882 μA.

Next, the noise characterization of the fabricated converters, which has a thermal origin, was carried out. Figure 9 shows the result of the converter output ratio (T_{MEMS}/T_{REF}) noise characterization in five different dies measuring a 10 pF C_{MEMS}. The RMS error due to noise in the conversion is presented, depending on the number of averaged samples per measurement. It can be observed that the RMS

noise error is reduced when the number of averaged samples per measurement rises. If the average of 10 samples is used to obtain a measurement, the value of the Effective Resolution (ER) corresponding to the RMS noise is above 10 bits. This increases the measuring time of the converter to 1.02 ms.
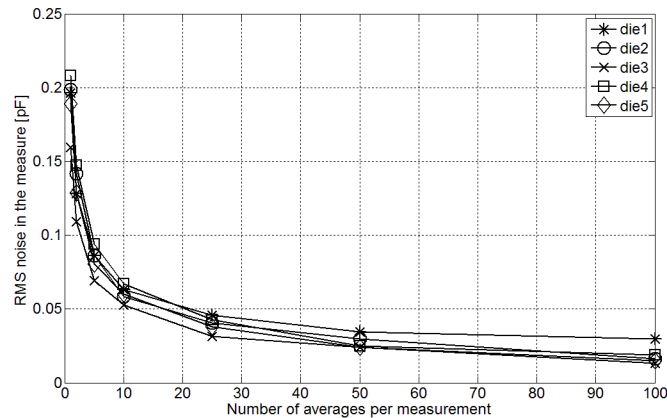

Figure 9. RMS noise in the measurements when converting a 10 pF C$_{MEMS}$.

3.1.2. Pressure-to-Time Conversion

In order to test the behavior of the capacitance-to-time interface working as part of a pressure sensor, it was connected to a MEMS pressure-to-capacitance transducer [8]. Taking into account that the MEMS transducer requires a three-point calibration the objective of this characterization is to evaluate the error generated in the pressure measurements that cannot be compensated for with the three-point calibration.
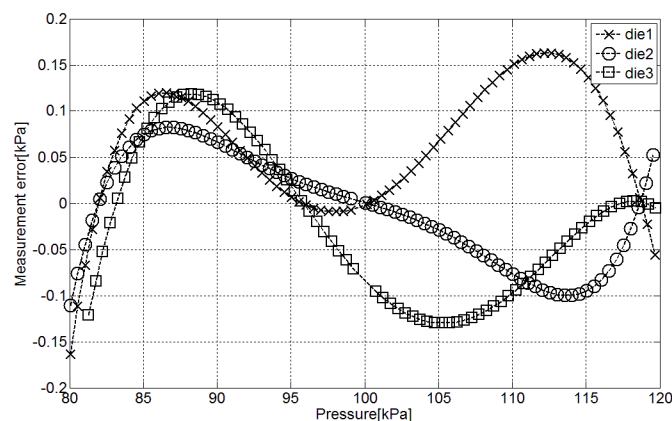

Figure 10. Error in the pressure estimation with the fabricated pressure sensor.

The difference between pressure measured in a pressure reference (GE DPI 620) and same pressure estimated through the proposed interface is presented in Figure 10. The mean accuracy of the pressure sensor due to the accumulative nonlinearities of the MEMS pressure transducer and the fabricated sensor interface after three-point calibration is approximately ± 0.1 kPa in the range between 80 kPa and 120 kPa. This way, the conversion inaccuracy is $\pm 0.25\%$ of the measuring range which corresponds to an effective linear resolution around 7.6 bit with an LSB of 0.2 kPa. According to the measurements presented in Figure 9 the ER of the interface is around 9 bit with a single sample per measurement, enough with this linear resolution. Therefore, a measuring time of 102 μs with an average current

consumption of 0.882 µA will be sufficient to perform the pressure measurements with 7.6 bits of resolution.

3.2. Discussion

A performance summary and a comparison with other state-of-the-art capacitive-sensor interfaces are shown in Table 1. The reported figure-of-merit (FOM) normalizes the energy consumption to the resolution. It is derived from the well-known FOM for evaluating general purpose ADCs [4], and is calculated as in Equation (14), where I_{AV}, T_{MEAS} and ER correspond to the average current consumption, measurement time and Effective Resolution respectively.

$$FOM(J/bit) = \frac{I_{AV}V_{DD}T_{MEAS}}{2^{ER}} \tag{14}$$

Table 1. Comparison of reported capacitive sensor interfaces.

Ref.	Type	Tech (µm)	Act. Area (mm^2)	Input Cap. (pF)	Supply (V)	Current Cons.	Meas. Time.	Eff. Res. (bit)	Out	FOM
ISCC'14 [9]	SAR ADC	0.18	0.49	2.5\75.3	1.2–0.9	160 nA	4 ms	13.3	Digital	0.063 pJ
TCASII'11 [10]	ΣΔ	0.35	0.048	–0.5\0.5	3.3	436 µA	0.128 ms	11	Digital	90 pJ
A-SSCC'11 [11]	ΣΔ	0.16	0.25	0.4\1.2	1.8	5.85 µA	10 ms	13	Time	13 pJ
ESSCIRC'11 [5]	PM	0.13	0.0725	6\6.3	0.3	0.9 µA	1 ms	6.1	Time	3.9 pJ
JSSC'12 [4]	PM	0.35	0.51	6.8	3.3	64 µA	7.6 ms	15	Time	49 pJ
ESSCIRC'08 [6]	PWM	0.32	0.528	0.5\0.76	3	28 µA	0.033 ms	8	Time	10.8 pJ
TIM'12 [3]	PWM	0.35	0.09	2.5\2.82	3	18 µA	0.04 ms	9.3	Time	3.4pJ
This work	PWM	0.09	0.045	10	0.5	0.882$µA$	1.02 ms	10	Time	0.43 pJ

A minimum FOM together with a minimum supply voltage and a minimum active area are the desired characteristics for wireless passive sensor systems. As shown in Table 1, where the proposed capacitance sensor interface is compared with the state of the art, the proposed design performs extremely well in these three characteristics, allowing a FOM of 0.43 pJ/bit, a supply voltage of 0.5 V an area of 0.045 mm^2 to be obtained. Regarding the area, the proposed circuit is the smallest. The supply voltage is the second smallest, only improved by [5], which reports and outstanding supply voltage of 0.3 V but has a noisy output with only 6.1 bits of ER.

As far as conversion efficiency goes (FOM), the presented design is the second most efficient only improved by [9]. The main strength of [9] is an array of nine capacitors that is adjusted in each measurement and acts as reference capacitor. This technique allows the circuit to cover a huge input capacitance range (2.5 pF to 75 pF) without loosing linearity, increasing the resolution of the sensor up to 13.3 bits. This high resolution together with a very low current consumption leads to a very low FOM. However, the implementation of the capacitor array requires area 10 times larger than the one used in this work.

Therefore, it can be concluded that the presented design has a remarkable overall behavior in terms of supply voltage, design size and FOM. These good features are also validated in the complete pressure sensor. In this case, as a single sample per measurement (no averaging) is enough to ensure a resolution of 7.64 bits, the energy per measurement is reduced to 45.06 pJ and the FOM to only 0.226 pJ/bit.

In order to complete the presented capacitance to time interface, a low power and high efficiency time to digital converter is necessary. In [12] a compatible converter is presented which reports a supply voltage of 0.6 V and a power consumption of 0.53 μW. The combination of these two devices would form an ultra low voltage and low power pressure sensor.

4. Conclusions

Given the great interest in the development of low-power and low-voltage sensor systems for WSN and consumer electronics, this paper presented an ultra low-power and low-voltage pulse-width modulation based capacitive sensor interface. The system is based on a simple relaxation oscillator that generates a pulse whose width depends on the value of a capacitive MEMS transducer. In addition, the interface includes an integrated reference capacitor that is also converted to time in order to perform ratiometric measurements of the MEMS transducer and reduce PVT variation effects.

The interface has been designed and fabricated in standard 90 nm CMOS 1P9M technology and measurement results show improved efficiency and reduced chip area relative to reported interfaces based on time conversion. In order to validate the suitability of the interface as part of a pressure sensor it has been successfully connected to a commercial pressure transducer. The results demonstrate the suitability of the proposed architecture for WSN and low-power consumer electronics, and they reinforce the use of time-conversion based sensor interfaces over traditional ADCs in these applications.

Author Contributions

Andoni Beriain and Roc Berenguer designed and measured the sensor interface. Iñigo Gutierrez and Hector Solar act as external consultants during the design and characterization of the device. In addition they contributed substantially to the preparation of the manuscript.

Conflicts of Interest

The authors declare no conflict of interest.

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