

Article

A Time-of-Flight Range Sensor Using Four-Tap Lock-In Pixels with High near Infrared Sensitivity for LiDAR Applications

Sanggwon Lee ¹, Keita Yasutomi ², Masato Morita ¹, Hodaka Kawanishi ¹ and Shoji Kawahito ^{1,2,*}

¹ Graduate School of Science and Technology, Shizuoka University, Hamamatsu, Shizuoka 432-8011, Japan; sglee@idl.rie.shizuoka.ac.jp (S.L.); mmori@idl.rie.shizuoka.ac.jp (M.M.); hkawa@idl.rie.shizuoka.ac.jp (H.K.)

² Research Institute of Electronics, Shizuoka University, Hamamatsu, Shizuoka 432-8011, Japan; kyasu@idl.rie.shizuoka.ac.jp

* Correspondence: kawahito@idl.rie.shizuoka.ac.jp; Tel.: +81-53-478-1313

Received: 7 November 2019; Accepted: 22 December 2019; Published: 23 December 2019



Abstract: In this paper, a back-illuminated (BSI) time-of-flight (TOF) sensor using 0.2 μm silicon-on-insulator (SOI) complementary metal oxide semiconductor (CMOS) technology is developed for long-range laser imaging detection and ranging (LiDAR) application. A 200 μm -thick bulk silicon in the SOI substrate is fully depleted by applying high negative voltage at the backside for higher quantum efficiency (QE) in a near-infrared (NIR) region. The proposed SOI-based four-tap charge modulator achieves a high-speed charge modulation and high modulation contrast of 71% in a NIR region. In addition, in-pixel drain function is used for short-pulse TOF measurements. A distance measurement up to 27 m is carried out with +1.8~−3.0% linearity error and range resolution of 4.5 cm in outdoor conditions. The measured QE of 55% is attained at 940 nm which is suitable for outdoor use due to the reduced spectral components of solar radiation.

Keywords: CMOS image sensor; SOI detector; backside-illumination; time-of-flight; lock-in pixel

1. Introduction

Recently, much attentions have been paid to complementary metal oxide semiconductor (CMOS)-based time-of-flight (TOF) range image sensors to be used for a variety of applications such as AR/VR/MR, security systems, drones, robots and autonomous vehicles [1–4]. These near-future applications require more distance in its measurement range and higher tolerance and resolution under high ambient light operation for outdoor use. There are two types of TOF range image sensors: direct and indirect TOF range image sensors. For a long-range laser imaging detection and ranging (LiDAR) application, direct-type TOF range image sensors are believed to be suitable. A single photon avalanche diode (SPAD) is a key device for CMOS-based direct TOF imagers with sufficient spatial resolution. Indeed, recently several SPAD-based LiDARs with measurable distance of over 100 m have been reported [5–7]. However, SPAD-based direct TOF sensors need relatively complicated circuits with high-speed clocking for time-stamp measurements of photons and statistical processing for removing the influence of ambient light and wide dynamic range, and, as a result, SPAD-based direct TOF sensors have a difficulty of having high spatial resolution, or large pixel number. Another issue of current SPAD-based imagers is low photon detection efficiency (PDE) at near-infrared (NIR) region. For outdoor use of TOF range imagers, a NIR band centered at 940 nm is useful for relaxing the influence of direct sun light where the spectral components of solar radiation. However, SPAD-based LiDARs with enhanced NIR sensitivity has often the PDE of less than 10% at 940 nm band [8,9].

On the other hand, current indirect TOF sensors based on lock-in pixels are useful devices for 3D depth imaging of a few meters or up to several meters [10–12]. As a 1Mpixel indirect TOF image sensor has demonstrated [13], indirect types are good for having high spatial resolution. Although the indirect TOF image sensors often suffer from multipath reflections and retro-reflector or associated stray light signals, numerous methods to mitigate those effects have been reported [14–16], and the subject is still developing actively. Using very high continuous-wave (CW) modulation frequency for demodulators in the TOF pixel, the depth resolution has been greatly improved if the distance is a few meters. However, the issue of indirect TOF imagers is its applicable distance, tolerance to ambient light, depth resolution under strong ambient light. The operation of 3D range image sensors under such aggressive conditions is increasingly demanded for the above-mentioned applications to be realized.

To address the issues for next-generation applications of TOF imagers, this paper proposes a backside illuminated (BSI) silicon-on-insulator (SOI) based four-tap lock-in pixel indirect TOF imager using short-pulse modulation [17]. The proposed indirect TOF pixel has multi-tapped gates for signal outputs and a high-speed charge draining gate and uses short light pulse (small duty) for TOF measurements [18,19]. This technique allows us to use range-shifted TOF measurements that cover wide distances while having relatively high depth resolution, even under strong ambient light, by exploiting the feature of power-concentrated short light pulse, short-time gating for demodulation, and draining ambient light components during the off-state of signal light pulse. For high quantum efficiency (QE) and high-speed carrier response, a thick substrate of 200 μm is used as a BSI photodetector, and is fully depleted by applying high back bias voltage to achieve high-speed charge modulation as well as high QE in a NIR 940 nm band. The SOI active layer is used for a gate structure to modulate a channel potential that realizes charge modulation. Recently, various BSI technologies with a fully-depleted thick substrate [20–25] have been reported. The SOI-based pixel detector (SOIPIX) structure used in this paper is one of such technologies, but suitable for simultaneously integrating X-ray or near-infrared photon detectors and high-density CMOS circuits in a pixel as a 3D stacking manner [25,26]. A proof-of-concept TOF sensor chip based on the SOIPIX technology has been implemented and tested. A high QE and resulting high range resolution in long-range TOF measurements have been demonstrated.

The remainder of this paper is organized as follows. Section 2 describes the pixel structure and operation. Section 3 treats TOF measurement algorithms using range-shifted short pulses. The results of implementation of a TOF sensor chip are given in Section 4. Section 5 presents concluding remarks.

2. Lock-In Pixel Structure and Operation

2.1. Silicon-On Insulator (SOI) Lock-In Pixel Detector

The SOI-based lock-in pixel detector as shown in Figure 1 is based on the SOIPIX technology [25–27] and realized by adding a photo-charge modulation structure implemented by highly-doped thin Si (SOI) as the gate, the BOX (buried oxide) as the insulator, and the substrate Si as the semiconductor layer. Although the thin SOI layer is basically used for CMOS readout circuits, in the charge modulator area the Si active layer with n+ highly doped and typically used for a source or drain of SOI transistors forms a transfer gate. In the front surface region of the substrate in the charge modulator area, the buried n-well (n_1) layer is formed for creating a buried channel of the charge modulator. The structure for the charge modulation is illustrated based on a two-tap lock-in pixel for simplicity. The SOI transfer gates (G_1 and G_2) modulate the channel potential for high-speed lock-in detection. A constant negative bias is applied to the center gate (G_C) in order to make the front-surface pinning to the potential of the front-surface bias, V_{BB2} . For the stable operation of SOI circuits, the rest of the area is occupied with the buried p-well layers (p_1) under the BOX surface. In order to reduce dark current and carrier trapping at the Si-SiO₂ interface and simultaneously collecting photo-carriers generated at deep inside of substrate Si, stacking of two buried p-wells (p_1 and p_2), and buried n-well (n_1) is used at this region other than the area of the charge modulator. The p_1 layer has a relatively high doping concentration that is around 10^5 – 10^6 times higher than the substrate (p-). It neutralizes the front surface of the

substrate for pinning the potential to the front-surface bias (V_{BB2}). This layer also acts as the shielding from the photo-charge detector of the substrate to SOI circuits. The p_2 layer creates a potential barrier under the n^+ floating diffusions (FDs) to reduce the parasitic photo-sensitivity of FDs. The n_1 created under p_2 is fully depleted and acts as a buried channel for horizontally drifting photo-carriers which are drifted to the channel from deep inside of the substrate by the vertical electric field when the reverse bias is applied at the back substrate contact (p^+). This n_1 layer is also used for preventing a punch-through hole current from the buried p -wells to the substrate by creating a potential barrier to holes in the p -wells.

Figure 2 shows the conceptual potential diagram for the SOI-based lock-in pixel detector. By applying high negative backside bias (V_{BB1}), a vertical electrical field is formed as shown in the right-side potential distribution on $Z - Z'$ (in Figure 2b). The photo-electrons generated at the deep inside of the substrate are accelerated toward the buried channel (n_1). Because of the potential barrier by the p_2/n_1 junction and the lateral electric field created in the depleted buried channel (n_1), the electrons are transferred to the central region of the pixel along the potential distribution on $X_1 - X_1'$ and then to the front surface just under the transfer gates. The photo-electrons generated at the deep inside of substrate just under the charge modulator are directly accelerated to the channel region of the charge modulator. Depending on the applied gate voltage to the transfer gates, G_1 and G_2 , a potential slope to accelerate carriers to left to right or right to left is created at the buried channel as shown in the left-side potential distribution on $X_2 - X_2'$ (in Figure 2a). By applying the gating pulses for G_1 and G_2 consecutively as shown in the timing diagram of Figure 2c, the signal N_1 (orange colored) as a result of overlapping of light pulse with the gating time of G_1 is accumulated in the FD_1 node and the signal N_2 (gray colored) due to that of G_2 is accumulated in the FD_2 node. Since the difference between N_1 and N_2 depends on the delay of the light pulse, or the TOF, the TOF can be measured by knowing the charge amounts of N_1 and N_2 . The details are described in Section 3 for the case of four-tap lock-in pixels.

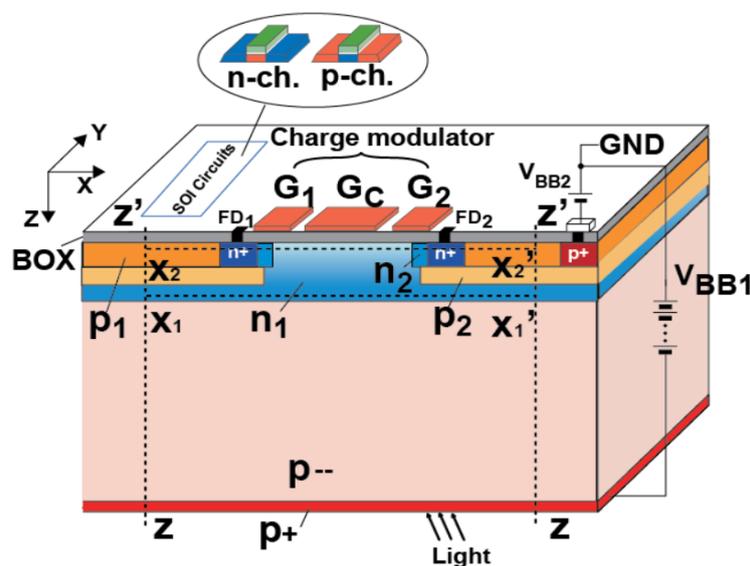


Figure 1. Proposed silicon-on-insulator (SOI)-based lock-in pixel detector structure.

2.2. SOI-Based Four-Tap Lock-In Pixel for TOF Sensors

Figure 3a shows the top view of the SOI-based four-tap lock-in charge modulator. It has four transfer gates (G_1 , G_2 , G_3 , and G_4) for transferring those time-gated signals and drain gates (G_D) for draining unwanted photo-generated electrons. Generated and gathered signal charges at the front-surface of the charge modulator are transferred to one of four FDs, i.e., FD_1 , FD_2 , FD_3 , or FD_4 by applying high voltage level to one of four transfer gates, G_1 , G_2 , G_3 , or G_4 , and low voltage level to the

others. For draining signal or unwanted charges, G_D is set to high level and the other gates are set to low level.

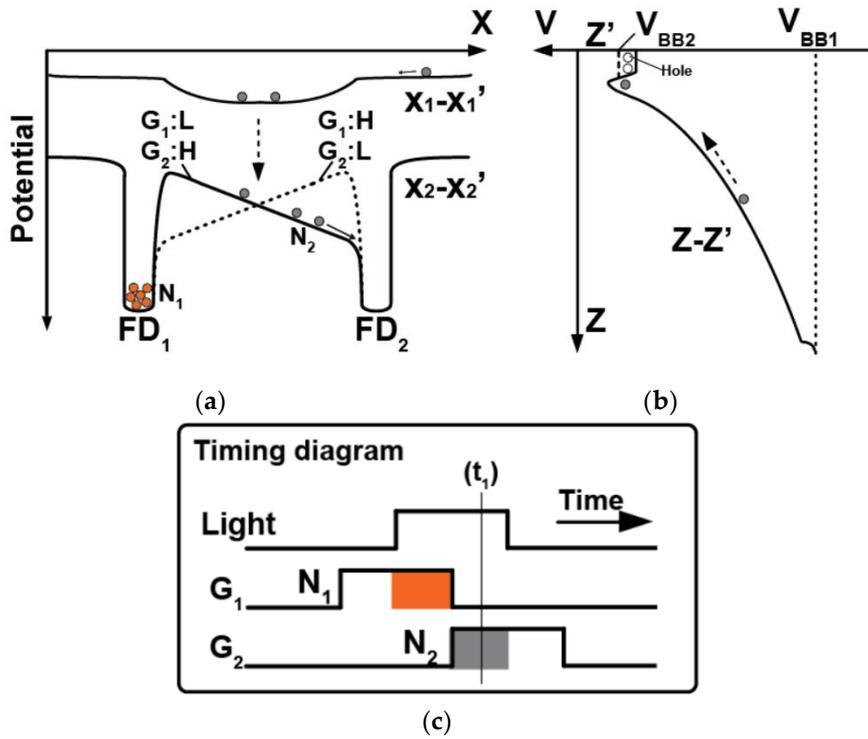


Figure 2. Concept of potential design and its timing diagram for the proposed SOI-based lock-in detector (two-tap). The potential distributions (a) for $X_1 - X_1'$ and $X_2 - X_2'$ axes (b) for $Z - Z'$ axis (See Figure 1). Those potential distributions are drawn at the timing of t_1 in (c).

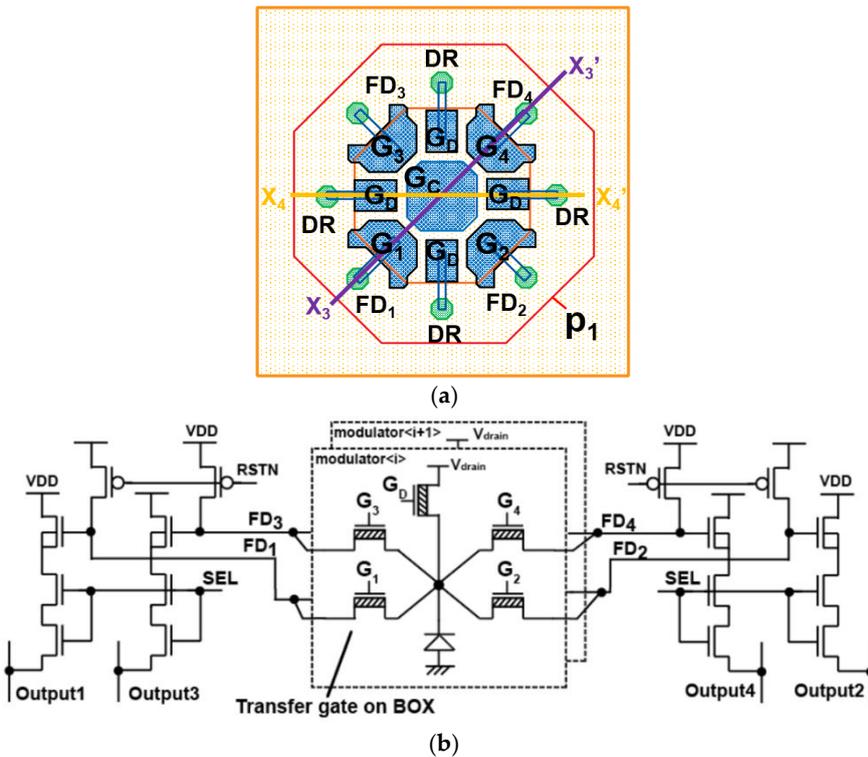


Figure 3. Developed four-tap lock-in pixel. (a) Pixel layout and (b) its equivalent circuit.

As shown in Figure 3b, the unit pixel consists of two charge modulators whose FD nodes are connected in parallel, hence charge signals of the same node name are summed in the charge domain. The source of pMOS reset transistors and the gate of source follower transistors are connected to the four FDs, and together with select transistors, 4-channel 3T-type active pixel readout circuits are implemented for each pixel. The maximum rating voltage (VDS) of nMOS is 2.5 V in the SOI technology. To guarantee that the VDS of transistors is smaller than the maximum rating, the two nMOS transistors are connected in series for the select transistors. The size of charge modulator is $18 \times 18 \mu\text{m}^2$ and the area of a unit pixel including two modulators is $36 \times 18 \mu\text{m}^2$. The photo-charge generated in the substrate detector within the area of $36 \mu\text{m} \times 18 \mu\text{m}$ is collected in either one of the two modulators and the modulated charges of them are summed up. In the SOI layer, the structure for the two modulator units occupies 54% of the area of $36 \mu\text{m} \times 18 \mu\text{m}$ and the other area (46%) is used for readout circuits including reset, select and source follower transistors and interconnections. Therefore, without losing the 100% fill-factor, the two modulator units and readout circuits are implemented in the area of $36 \mu\text{m} \times 18 \mu\text{m}$. The pixel size is chosen because the size of the readout circuit is designed with $9 \mu\text{m}$.

The simulated potential diagram of the designed four-tap lock-in pixel along cross-sections $X_3 - X_3'$ and $X_4 - X_4'$ in Figure 3a and 3D potential distributions are shown in Figure 4. Figure 4a,c show a charge transfer mode by G_1 and Figure 4b,d show a charge drain mode by G_D . For the transfer mode by G_1 , the gate voltage of G_1 is set to high and those of the other gates (G_2 , G_3 , G_4 , and G_D) are set to low. For the drain mode, G_D is set to high and the other gates are set to low. In these simulations, the thickness of the BOX layer is set to 200 nm and the V_{BB2} potential of -3.5 V is applied. Even with the thick BOX layer, potential modulation in the channel is observed. Since any potential barriers or dips are not observed, a high-speed charge modulation is expected.

The electron trajectories of generated signal and their charge transfer time are shown in Figure 5. In the simulations, signal electrons are placed on different initial points: $(X, Y, Z) = (1, 1, 192)$, $(3, 3, 60)$, $(4.6, 4.6, 192)$, $(9, 9, 192)$, $(14, 12, 120)$, and $(14.6, 11, 192)$, where G_1 is set to high. Figure 5a shows the electron trajectories from 0 to $200 \mu\text{m}$ and Figure 5b shows its enlarged figure from 0 to $10 \mu\text{m}$. Figure 5c shows the charge transfer time from the initial positions to FD_1 . From the simulation result of Figure 5, the generated electron is transferred to the FD_1 within 15 ns.

Figure 6 shows the timing diagram for the four-tap lock-in pixel operation. One sensing cycle operation includes an integration period and the readout period. Each integration period contains N lighting cycles with the period of T_C and in each lighting cycle, four transfer gates are opened consecutively with the width of T_0 and the rest of time are used for photo-charge draining by opening the drain gate. To obtain a sufficiently large signal for calculating depth resolution, the number of lighting cycles, N , is increased. During the readout period, the G_D is always set to high and the other gates are set to low to drain unexpected signals. The accumulated signals transferred at FD nodes (FD_1 , FD_2 , FD_3 , and FD_4) are read out through the in-pixel source followers. By using four output signals, the depth calculation is carried out. The details are described in Section 3.

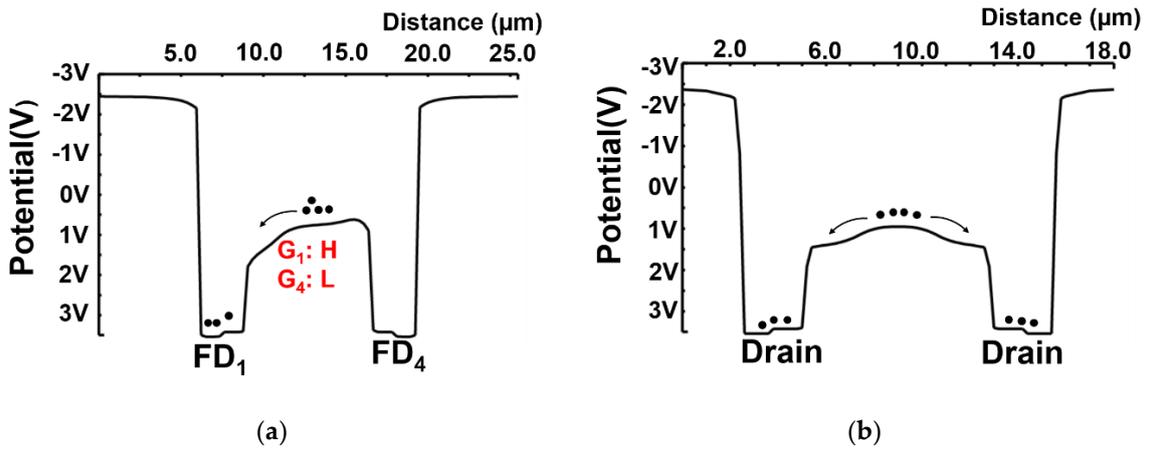


Figure 4. Cont.

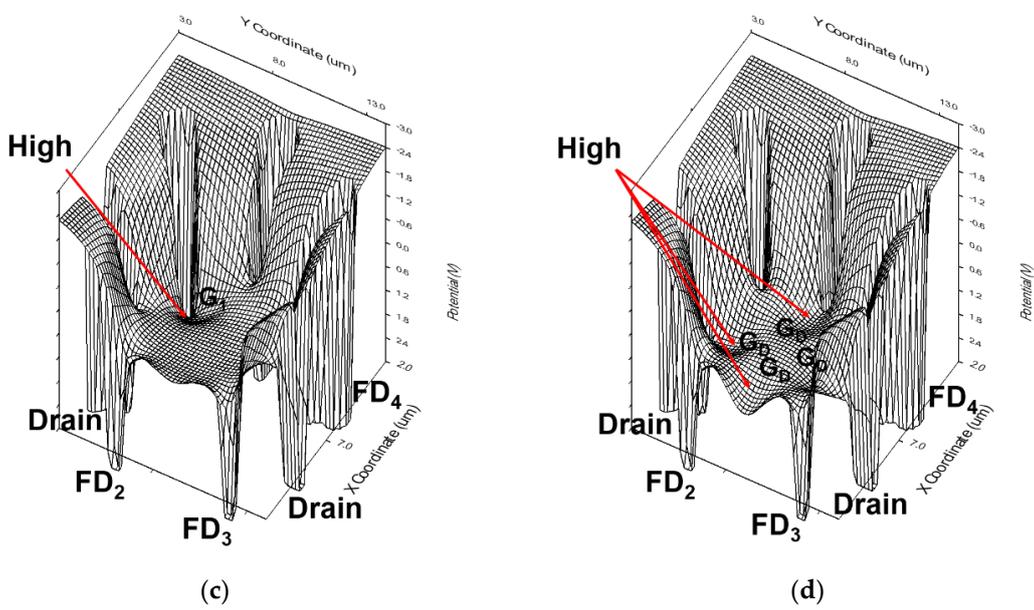


Figure 4. Simulation results for potential diagrams of a four-tap pixel. (a,c) $G_1 = \text{high}$, $G_2, G_3, G_4; G_D = \text{low}$ (Transfer mode) (b,d) $G_D = \text{high}$; $G_1, G_2, G_3, G_4 = \text{low}$ (Drain mode).

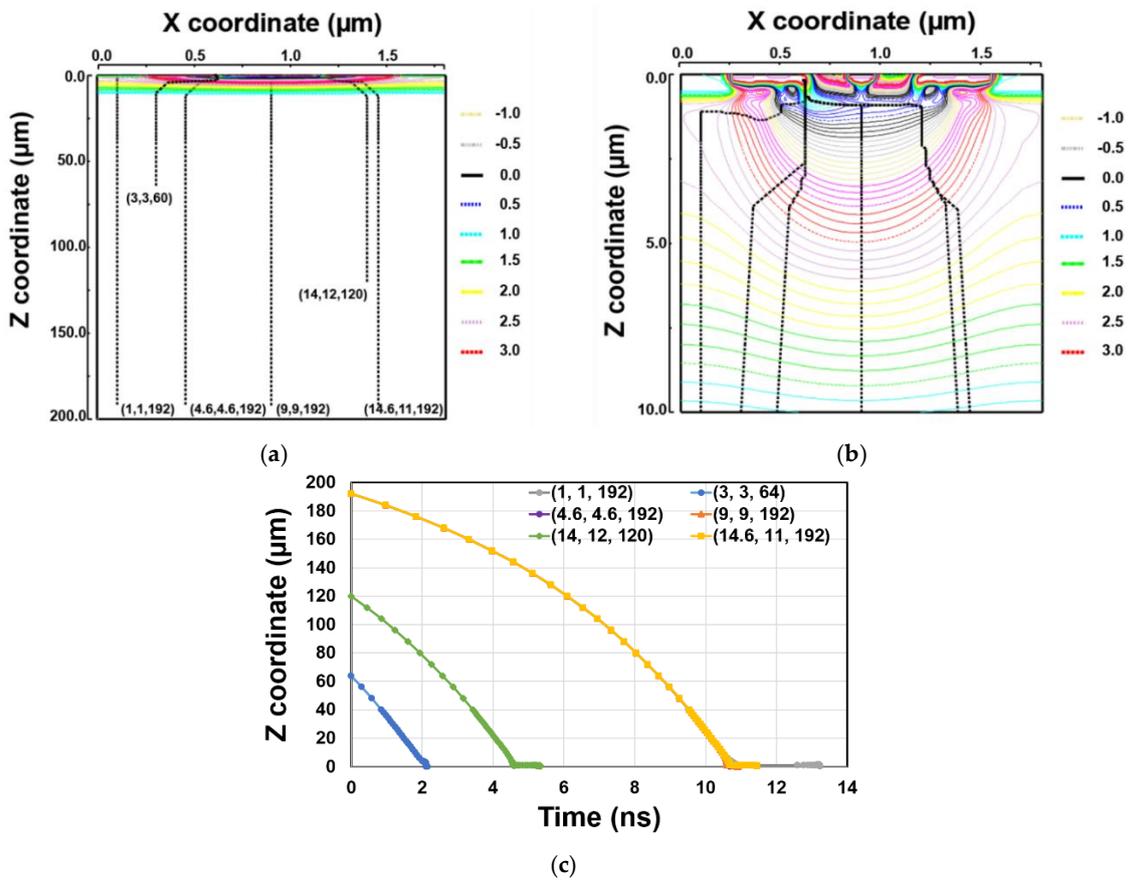


Figure 5. Simulation results for charge transfer. (a) $Z = 0\text{--}200\ \mu\text{m}$. (b) $Z = 0\text{--}10\ \mu\text{m}$ (zoomed). (c) Charge transfer time to FD_1 node. Electrons are placed at (1, 1, 192), (3, 3, 60), (4.6, 4.6, 192), (9, 9, 192), (14, 12, 120), and (14.6, 11, 192).

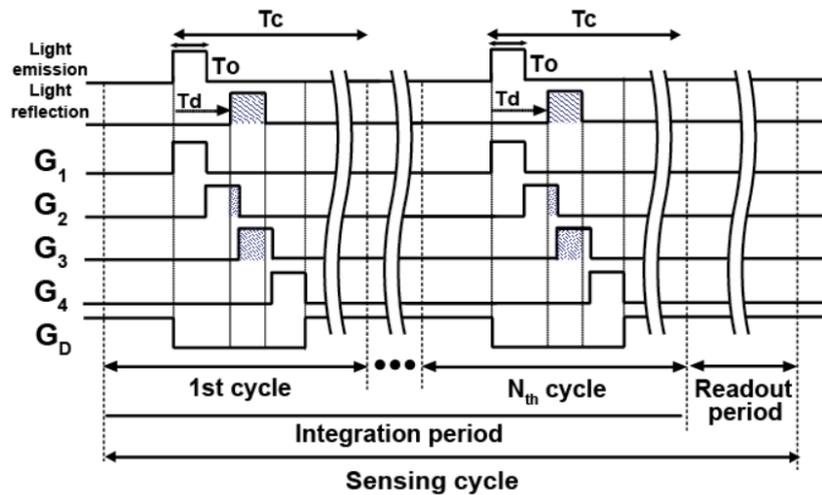


Figure 6. The timing diagram for the four-tap lock-in pixel.

3. TOF Range Calculation and Resolution with Four-Tap Lock-On-Pixel and Short Pulse Modulation

Figure 7 shows the timing diagram for the gating and the corresponding response of the signal outputs to the TOF of the light pulse, T_d . The pixel output signals, S_1 , S_2 , S_3 , and S_4 , respond to the light pulse delay with a triangular shape as shown in Figure 7. Therefore, the difference of S_1 and S_3 ,

$S_{13} = (S_1 - S_3)$ and $S_{24} = (S_2 - S_4)$ respond linearly to the TOF of light pulse within a range of $2T_0$. The functions of T_d , calculated by the difference of the signals gated by G_1 and that by G_3 , i.e., S_{13} and gated by G_2 and that by G_4 , i.e., S_{24} normalized by the signal amplitude $S_A = (|S_{13}| + |S_{24}|)$ are expressed as:

$$X_R = 1 - \frac{S_{13}}{S_A} \quad (1)$$

and

$$Y_R = 2 - \frac{S_{24}}{S_A} \quad (2)$$

respectively. X_R responds linearly to T_d from 0 to $2T_0$ and Y_R responds linearly to T_d from T_0 to $3T_0$. By combining these two responses to T_d , the depth range corresponds to the TOF range of 3 times T_0 can be measured as:

$$D = D_{TW}\{X_R(1 - Z) + Y_R Z\} \quad (3)$$

where $D_{TW} = (0.5cT_0; c$ is the velocity of light) is the unit depth determined by the light pulse width and Z is a factor of choosing X_R or Y_R or blending X_R and Y_R expressed as:

$$Z = \begin{cases} 1 & (\text{if } Y_R \geq 1.9 \& X_R \geq 0.9) \\ 0.5 & (\text{if } Y_R < 1.9 \& X_R \geq 0.9) \\ 0 & (\text{if } X_R < 0.9) \end{cases} \quad (4)$$

The measurable range (D_{TW}) is proportional to the pulse width of light source as shown in Equation (3), while the range resolution is inversely proportional to the pulse width as described later. As a result, the short pulse width leads to a better range resolution and reducing background light influence at the cost of a reduced measurable range. The pulse width can be adjusted arbitrarily depending on the required range resolution determined by its application.

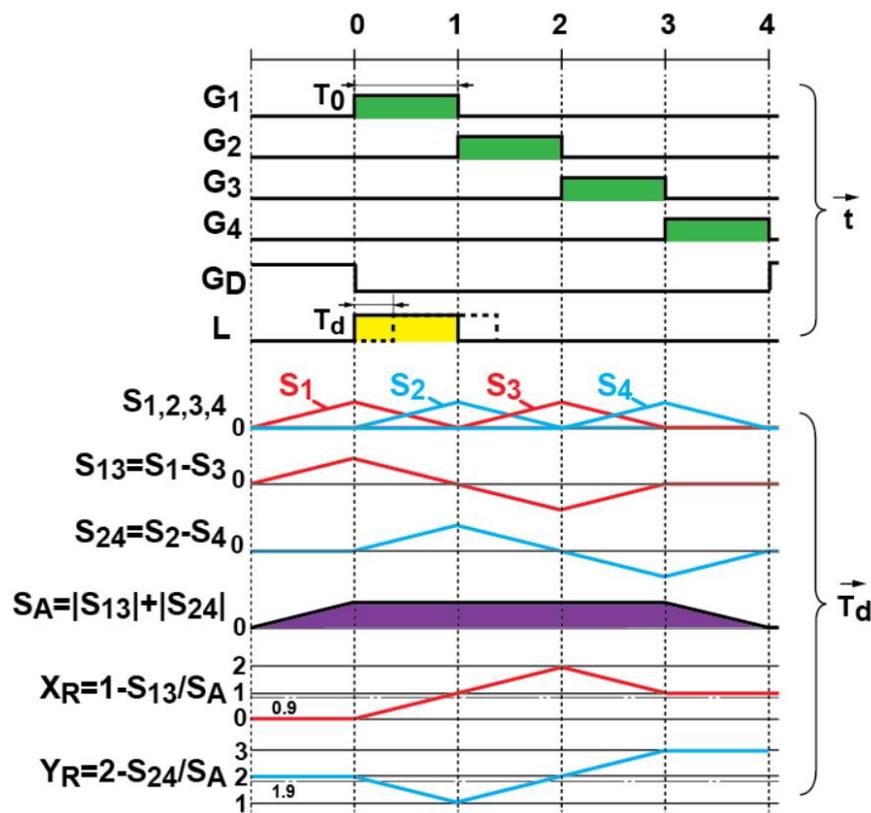


Figure 7. The timing diagram for the gating and the corresponding response of the signal outputs to the time-of-flight (TOF) of the light pulse, T_d .

4. Results and Discussion

4.1. Implemented TOF Sensor Chip

A prototype TOF range sensor with the proposed four-tap lock-in pixel is implemented using a $0.2 \mu\text{m}$ SOI detector technology [17]. The die micrograph and block diagram of the implemented chip are shown in Figure 8. Since the TOF sensor tested here is implemented in a part of a multi-purpose CIS chip, the chip area relevant to this paper only is shown in Figure 8. The TOF sensor is comprised of a four-tap gate driver, a small pixel array with 4×96 pixels, a readout circuit with 16 columns, and a scanner. Figure 8 also shows the schematic of the readout circuit. The readout circuit consists of a switched-capacitor amplifier (first stage) using two capacitors, C_1 and C_2 , and two sample-and-hold circuits (second stage) using two capacitors, C_L . Using the first stage, the pixel fixed pattern noise (FPN) is cancelled and the signal component is amplified by the capacitor ratio of C_1/C_2 . In the second stage, the reset level and signal level of the first stage output are sampled in C_L and the FPN of the first stage is cancelled. The sampled reset and signal levels at each column are sequentially read out using a scanner by connecting them to final buffer amplifiers sequentially. The difference of the two outputs is taken and digitized by an external 14-bits analog-to-digital converter (ADC).

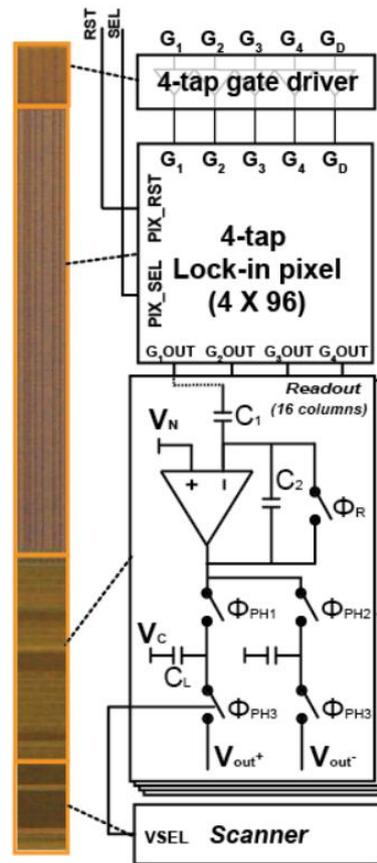


Figure 8. Chip micrograph and block diagram of the designed prototype sensor.

4.2. Measurement Results

Figure 9 shows the measured photo-response of the four-tap lock-in pixel as a function of light intensity. A white light source box (Kyoritsu, LB-8623) is used. In this measurement, the G_1 is always set to high and the other gates (G_2 , G_3 , and G_4) are always set to low during the exposure period. A linear response to light intensity for the G_1 before it is saturated is obtained. The parasitic sensitivity to the other signals is due to light or charge leakage. From this result, the extinction ratio defined by $(S_1/(S_1 + S_2 + S_3 + S_4)) \times 100\%$ measured at the signal level of 90% of the saturation is 84.7%.

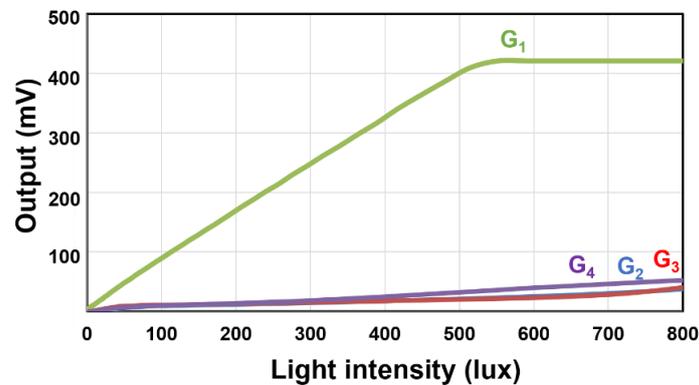


Figure 9. Photo-response as a function of light intensity. (at $G_1 = \text{High}$ and $G_2, G_3, G_4 = \text{Low}$).

Figure 10 shows the measurement results for modulation characteristics with different backside voltage (V_{BB1}). In this measurement, a 930 nm short-pulse laser (LDB-160B manufactured by Tama Electric Inc.) is used as the light source and is irradiated to the pixel. The pulse width and the cycle

time of the laser are set to <100 ps and 520 ns, respectively. The delay time of the laser trigger is scanned from 0 to 300 ns with the step of 1 ns. The gate pulse width of the pixel is set to 40 ns. For each measurement point on the delay, the number of irradiated light pulses is set to 50. The V_{BB1} is set to -20 V, -30 V, and -40 V. The ideal response is a rectangular shape to the pulse delay. For V_{BB1} of -20 V (Figure 10a), the response to the light pulse delay is much distorted because of the slow photo-carrier response, indicating the substrate is not fully depleted but partially neutralized. For V_{BB1} of -30 V (Figure 10b) and -40 V (Figure 10c), the response to the light pulse delay has a rectangular shape, indicating that the substrate is fully depleted by the backgate bias voltage of <-30 V, and photo-carriers are acquired speedily by drift of the carriers in the depletion region. The modulation contrast averaged for all gates, C_M , is calculated by:

$$C_M = \frac{1}{4} \sum_{i=1}^4 \left[\max \left(\frac{2S_i - S_{SUM}}{S_{SUM}} \right) \right] \quad (5)$$

where S_{SUM} is the sum of gates ($S_1 + S_2 + S_3 + S_4$). For the V_{BB1} of -30 V, the modulation contrast of 71% is obtained.

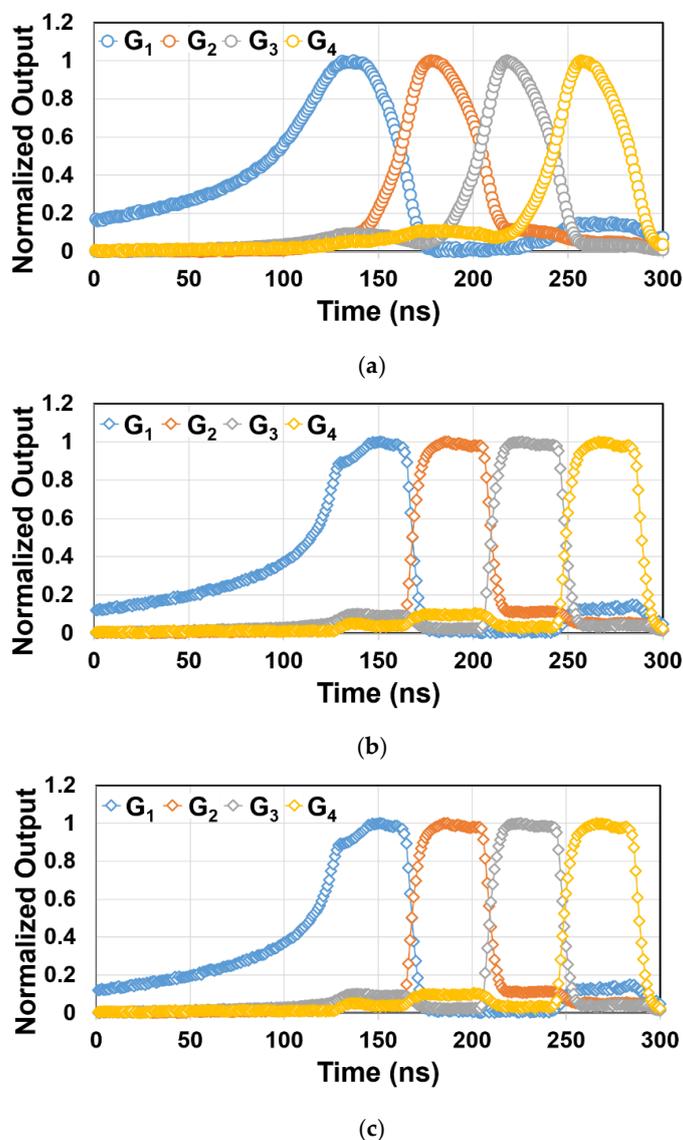


Figure 10. Modulation characteristic with various backside voltage using a 930 nm short pulse laser (a) $V_{BB1} = -20$ V, (b) $V_{BB1} = -30$ V, (c) $V_{BB1} = -40$ V.

As shown in Figure 10, the signal due to the G_1 gating for all the backgate bias voltages has a long preceding tail in the response to the delay. This indicates that the drain is not well functioning. The major reason for this is that the drain terminal in the chip is floating. As a result, in the draining phase, the unwanted signal charge is remained in the buried channel due to the lack of drain potential and then the charge is going to the FD_1 when the G_1 gate is opened. This problem can be solved by re-designing of the chip that the drain potential is fixed.

Figure 11 shows the measured quantum efficiency (QE) from the visible to the NIR regions with error bars for every wavelength and the ideal QE curves with attenuation factors (T_1). In this measurement, the G_1 gate is always turned on and the other gates (G_2 , G_3 , G_4 , and G_D) are turned off. The QE measured by the signal due to the G_1 gating only has an influence of sensitivity loss due to the charge and light leakage to the other gates, or parasitic sensitivity of the other gates. This QE including the gating efficiency determines the TOF sensor performances such as depth resolution and is regarded as an effective QE. The QE measured with the sum of all the signals due to G_1 , G_2 , G_3 , and G_4 gating is also shown in Figure 11 for a reference and the ideal QE curves are plotted. The ideal QE is calculated by:

$$QE(\lambda) = \frac{(1 - T_1)}{L_a(\lambda)} \int_{z_1}^{z_2} \exp\left(-\frac{z}{L_a(\lambda)}\right) dz \quad (6)$$

where $L_a(\lambda)$ is an absorption coefficient of the silicon and Z_1 and Z_2 are minimum and maximum depths of the depletion layer from the backside of the substrate. T_1 is an overall attenuation factor including a loss due to a surface light reflection and a signal acquisition loss due to the imperfect charge modulation. In the fitting calculation, Z_1 and Z_2 are assumed to be $0.45 \mu\text{m}$ and $198 \mu\text{m}$ from the doping profile and the substrate thickness, and the least-square method is used where the data of overall wavelength are taken into account. The T_1 of S_1 and S_{SUM} are estimated to 0.41 and 0.28, respectively. In Figure 11, the QE calculated with no attenuation factor ($T_1 = 0$) is also shown. Since the QE calculation is based on a simple assumption in which the attenuation factors are supposed to be independent of wavelengths, the fitting results are not always the same as the measurement results. However, the overall curve is similar to the ideal QE calculation. A high QE of 55% at 940 nm is obtained with S_1 and a QE of >65% is obtained with S_{SUM} . With an improvement of the design by reducing the parasitic sensitivity of the ungated outputs, a 10% higher effective QE will be realized.

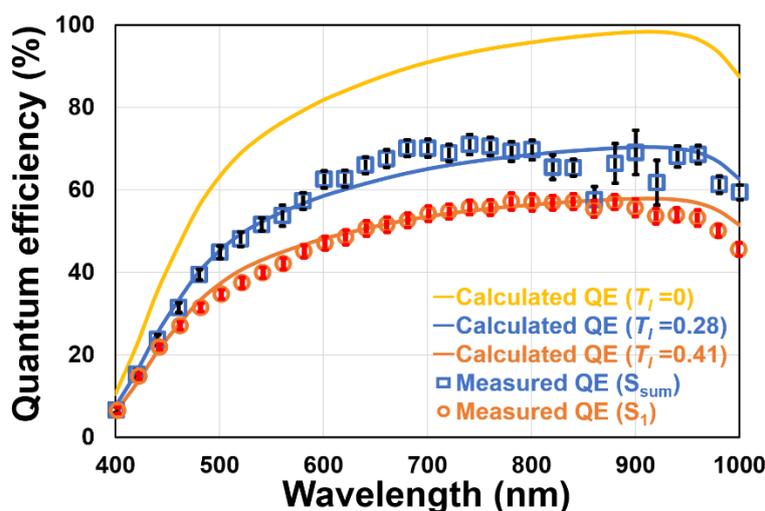


Figure 11. Measured quantum efficiency from the visible region to the near-infrared (NIR) region. The ideal quantum efficiencies (QEs) with various attenuation factors (T_1) are calculated by Equation (6). S_{SUM} is the sum of signals from all the gates ($S_1 + S_2 + S_3 + S_4$).

4.3. Distance Measurement

Figure 12 shows a measurement setup of the implemented TOF sensor for depth measurements. The laser pulse is synchronized with the TOF imager via a delay controller and is emitted to an object. Figure 13a,b show the measured distance and range resolution as a function of actual distance from 11 m to 27 m with a 1-m step. The measurement is done in outdoor and the background light level due to sun light is 75klux at the object plane. A 940 nm laser with an averaged light power density of 7.2 W/m² (1.8 W peak) at 30 m and a target with high reflective white paper are used for the long-distance measurement. An optical bandpass filter at 940 nm with 10 nm full width at half maximum (FWHM) is used. In this measurement, the pulse width for both the light and gate pulses is set to 40 ns, which corresponds to a unit measurable range of 6 m in a one time-window. The number of lighting cycles (shown in Figure 6) is 1000 with the cycle time of 520 ns and the TOF measurement time is 520 μs. The setting of pulse width and the laser cycle is to use a small duty light pulse. The use of small duty cycle allows us to have a high signal-to-noise ratio under high ambient light and given average light power. The use of a large cycle time (small duty cycle) is also necessary for avoiding an ambiguity of TOF measurements. By using the four-tap lock-in pixel structure, three time-windows (totally 18 m) can be measured as described in Section 3. By using a gating-time offset, the measurable range can be shifted arbitrarily. This technique is called a range-shift method [18]. Using a gating-time offset of 6.7 ns, for example, the range from 1 m to 18 m can be measured. Using the gating-time offset of 60 ns, the range from 9 m to 27 m can be measured. In Figure 12, the gating-time offset of 60 ns is used and because of the limitation of our measurement setup, the measurement result for the range from 11 m to 27 m only is shown. In the present measurement setup, there is a difficulty of accurate measurements of distance below 11 m. This is because the implemented TOF sensor has a very small number of horizontal pixels (4 pixels), the spread angle of the laser used in the distance measurement is also relatively small. As a result, the alignment of the reflected light to the pixel areas becomes difficult, particularly for the closer distance.

In Figure 13a, the distance nonlinearity error is measured to be +1.8~−3.0%. Figure 13b shows the measured and theoretically calculated range resolution. The theoretical range resolution, σ_D , within one time window is given by

$$\sigma_D = \frac{D_{TW}}{C_D \sqrt{N_S}} \times \sqrt{\frac{C_D N_{TOF} (N_S - N_{TOF})}{N_S^2} + 2 \left(1 - 2 \frac{N_{TOF}}{N_S} + 2 \frac{N_{TOF}^2}{N_S^2} \right) \left(\frac{1 - C_D}{4} + \frac{N_a}{N_S} + \frac{\sigma_R^2}{N_S} \right)} \quad (7)$$

where N_S is total signal electrons, N_{TOF} is signal electrons associated with TOF, N_a is the background light signal, σ_R is the dark noise. The derivation of Equation (7) is similar to [3,18]. Unlike in [3], a factor of modulation contrast, C_D , is included in Equation (7). The C_D takes a value from 0 to 1 and ideally equals 1. The number of total signal electrons (N_S) is expressed as

$$N_S = \frac{\lambda}{hc} \times QE \times A_{pix} \times FF \times T_a \times \frac{P}{W \times H} \times \frac{RT_L}{4F_N^2} \quad (8)$$

where h is the plank constant, A_{pix} is the area of the pixel, FF is fill factor of the pixel, T_a is the integration time, P is peak power of the laser source, $P/(W \times H)$ is power density on the sensor plane through a lens with transmission efficiency (T_L) and F-number (F_N) by an object with reflectivity (R).

The measured range resolution, which is also called the standard deviation of depth or depth noise, is 4.5 cm at 27 m. The measurement result of range resolution at 27 m suddenly worsen compared to the theoretical calculation. A possible reason for this is the jitter on the light pulse. The point of 27 m corresponds to the edge of measurable range, where the reflected light pulse is integrated by G_4 gate only or a part of the reflected light pulse is drained by G_D . Although the jitter of the light trigger is also induced at the transition edge of G_1 – G_2 , G_2 – G_3 , or G_3 – G_4 , the behavior and the resulting influence at the edge of measurable range is expected to be different from the others. Figure 14 shows

the histogram of distance at (a) 24 m and (b) 27 m. Because of the jitter or other unexpected noise sources, the distribution is not a simple Gaussian distribution at 27 m. The sensor performance and characteristics are summarized in Table 1.

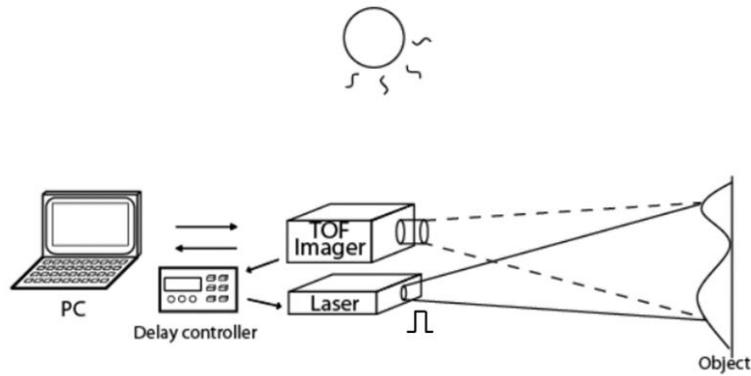
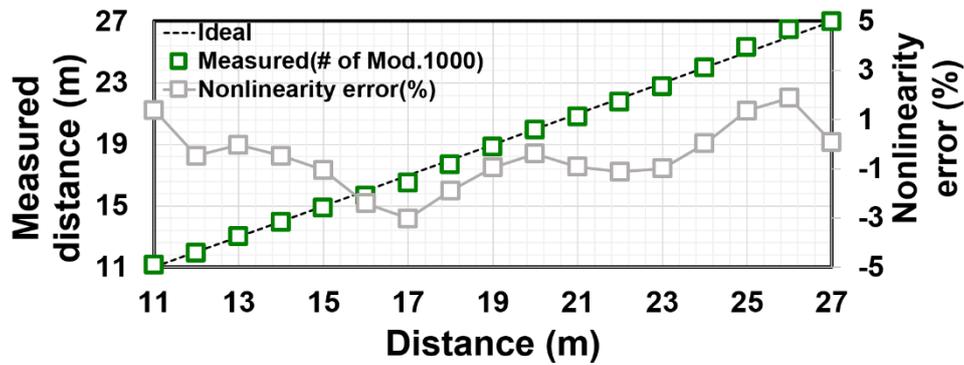
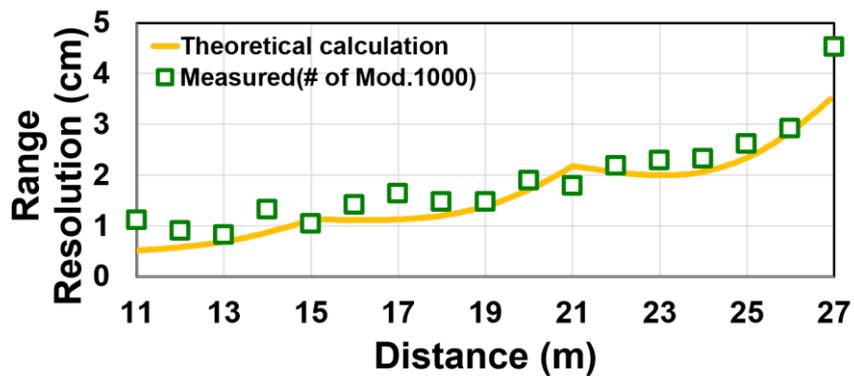


Figure 12. Setup of the implemented TOF sensor for depth measurement. The laser emission is controlled by the delay controller synchronized with the TOF imager.



(a)



(b)

Figure 13. Distance plot: (a) Measured and ideal; (b) measured and calculated range resolution.

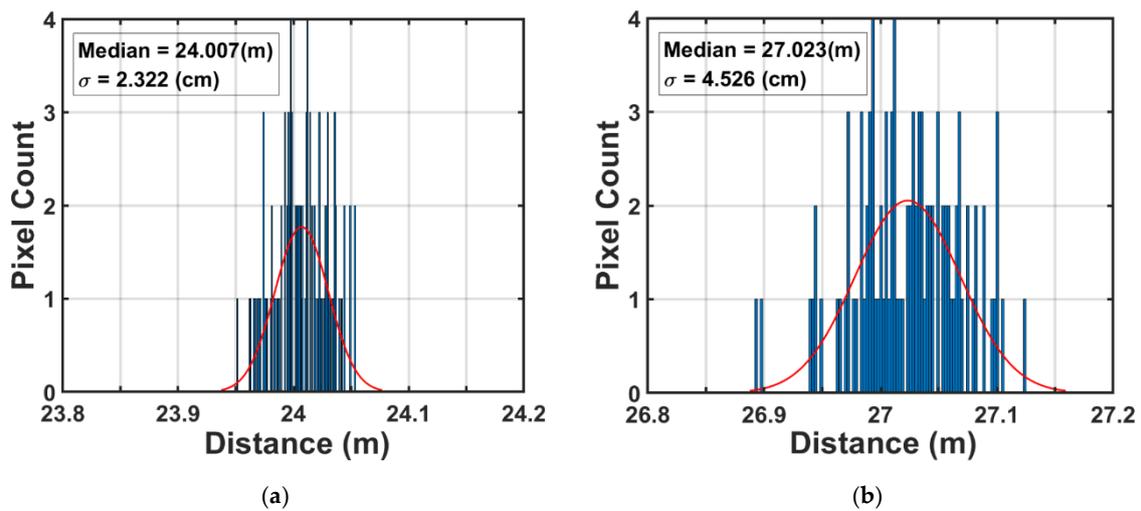


Figure 14. Histogram of distance at (a) 24 m and (b) 27 m.

Table 1. Performance summary.

Parameter	Value
Process	0.2 μm SOI-CMOS technology
Pixel size	36 μm \times 18 μm
Fill factor	100% (Backside illumination)
Substrate thickness	200 μm
Modulation	Light and Gate Pulse Width: 40 ns Cycle time of light pulse: 520 ns Duty ratio: 7.7%
Modulation contrast	71% with 930 nm short-pulse laser
Light source	Wavelength: 940 nm Power density: 7.2 W/m ² @ 30 m
Integration time	520 μs (1000 cycle)
Quantum efficiency	55% (at 940 nm)
Linearity error	+1.8~−3.0%
Range resolution	4.5 cm (at 27 m, outdoor (75klux))

5. Conclusions

This paper presents a TOF range imager with SOI-based lock-in pixels for long-range outdoor applications. The proposed TOF range imager has fully depleted bulk silicon for the backside illumination to enhance the responsivity in the NIR region. By using the SOI technology, a 200 μm thick substrate is used as a photodetector and the SOI active layer is used for the transfer gate to modulate the channel potential. The implemented four-tap lock-in pixel structure demonstrates a high-speed charge modulation and high modulation contrast of 71% at 40 ns gate width. The prototype TOF chip also demonstrates the distance measurement up to 27 m with +1.8~−3.0% linearity error and the measured range resolution of less than 4.5 cm using background light cancelling method. Moreover, the QE of 55% at 940 nm is obtained. From this work, we successfully confirm the multi-tap lock-in pixel range sensor with high QE at NIR region.

Author Contributions: K.Y. and S.K. proposed the device concept and provided the overall guidance of the project. S.L. and K.Y. designed the chip. S.L., M.M., and H.K. measured the chip. S.L., K.Y., and S.K. drafted the manuscript. All authors have read and agreed to the published version of the manuscript.

Funding: This study was partly supported by the Japan Society for the Promotion of Science (JSPS) KAKENHI Grand Number JP25109003 and the Center of Innovation Program from Japan Science and Technology Agency, JST.

Acknowledgments: The authors thanks to Lapis Semiconductor Inc. for the chip fabrication, and Y. Arai of KEK and SOIPIX team for helpful discussion.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Shcherbakova, O.; Pancheri, L.; Dalla Betta, G.-F.; Massari, N.; Stoppa, D. 3D camera based on linear-mode gain-modulated avalanche photodiodes. In Proceedings of the 2013 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC), San Francisco, CA, USA, 17–21 February 2013; pp. 490–491.
2. Akita, H.; Takai, I.; Azuma, K.; Hata, T.; Ozaki, N. An Imager using 2-D Single-Photon Avalanche Diode Array in 0.18- μm CMOS for Automotive LIDAR Application. In Proceedings of the 2017 Symposium on VLSI Circuits, Kyoto, Japan, 5–8 June 2017.
3. Kawahito, S.; Abdul Halin, I.; Ushinaga, T.; Sawada, T.; Homma, M.; Maeda, Y. A CMOS time-of-flight range image sensor with gates-on-field-oxide structure. *IEEE Sens. J.* **2007**, *7*, 1578–1586. [[CrossRef](#)]
4. Lange, R.; Seitz, P. Solid-state time-of-flight range camera. *IEEE J. Quantum Electron.* **2001**, *37*, 390–397. [[CrossRef](#)]
5. Niclass, C.; Soga, M.; Matsubara, H.; Ogawa, M.; Kagami, M. A 0.18- μm CMOS SoC for a 100-M-range 10-frame/s 200 96-pixel time-of-flight depth sensor. *IEEE J. Solid State Circuits* **2014**, *49*, 315–330. [[CrossRef](#)]
6. McCarthy, A.; Collins, R.J.; Krichel, N.J.; Fernández, V.; Wallace, A.M.; Buller, G.S. Long-range time-of flight scanning sensor based on high-speed time-correlated single-photon counting. *Appl. Opt.* **2009**, *48*, 6241–6251. [[CrossRef](#)] [[PubMed](#)]
7. Ximenes, A.R.; Padmanabhan, P.; Lee, M.-J.; Yamashita, Y.; Yaung, D.N.; Charbon, E. A 256×256 45/65nm 3D-Stacked SPAD Based Direct TOF Image Sensor for LiDAR Applications with Optical Polar Modulation for up to 18.6dB Interference Suppression. In Proceedings of the 2018 IEEE International Solid-State Circuits Conference—(ISSCC), San Francisco, CA, USA, 11–15 February 2018; pp. 96–97.
8. Takai, I.; Matsubara, H.; Soga, M.; Ohta, M.; Ogawa, M.; Yamashita, T. Single-Photon Avalanche Diode with Enhanced NIR-Sensitivity for Automotive LIDAR Systems. *Sensors* **2016**, *16*, 459. [[CrossRef](#)] [[PubMed](#)]
9. Webster, E.A.G.; Richardson, J.A.; Grant, L.A.; Renshaw, D.; Henderson, R.K. A Single-Photon Avalanche Diode in 90-nm CMOS Imaging Technology with 44% Photon Detection Efficiency at 690 nm. *IEEE Electron Device Lett.* **2012**, *33*, 694–696. [[CrossRef](#)]
10. Han, S.-M.; Takasawa, T.; Akahori, T.; Yasutomi, K.; Kagawa, K.; Kawahito, S. 7.4 A 413×240 -pixel sub-centimeter resolution time-of-flight CMOS image sensor with in-pixel background canceling using lateral-electric-field charge modulators. In Proceedings of the 2014 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC), San Francisco, CA, USA, 9–13 February 2014; pp. 130–131.
11. Stoppa, D.; Massari, N.; Pancheri, L.; Malfatti, M.; Perenzoni, M.; Gonzo, L. A range image sensor based on 10- μm lock-in pixels in 0.18- μm CMOS imaging technology. *IEEE J. Solid State Circuits* **2011**, *46*, 248–258. [[CrossRef](#)]
12. Yasutomi, K.; Usui, T.; Han, S.-M.; Takasawa, T.; Kagawa, K.; Kawahito, K. A Submillimeter Range Resolution Time-of-Flight Range Imager with Column-wise Skew Calibration. *IEEE Trans. Electron Devices* **2015**, *63*, 82–188. [[CrossRef](#)]
13. Bamji, C.S.; Mehta, S.; Thompson, B.; Elkhatib, T.; Wurster, S.; Akkaya, O.; Payne, A.; Godbaz, J.; Fenton, M.; Rajasekaran, V.; et al. 1Mpixel 65 nm BSI 320 MHz Demodulated TOF Image Sensor with 3.5 μm Global Shutter Pixels and Analog Binning. In Proceedings of the 2018 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 11–15 February 2018; pp. 94–95.
14. Naik, N.; Kadambi, A.; Rhemann, C.; Izadi, S.; Raskar, R.; Bing Kang, S. A light transport model for mitigating multipath interference in time-of-flight sensors. In Proceedings of the IEEE Conference on Computer Vision and Pattern Recognition (CVPR), Boston, MA, USA, 7–12 June 2015; pp. 73–81.
15. Bhandari, A.; Kadambi, A.; Whyte, R.; Barsi, C.; Feigin, M.; Dorrington, A.; Raskar, R. Resolving multipath interference in time-of-flight imaging via modulation frequency diversity and sparse regularization. *Opt. Lett.* **2014**, *39*, 1705–1708. [[CrossRef](#)] [[PubMed](#)]
16. Achar, S.; Bartels, J.R.; Whittaker, W.L.; Kutulakos, K.N.; Narasimhan, S.G. Epipolar time-of-flight imaging. *ACM Trans. Gr.* **2017**, *36*, 37. [[CrossRef](#)]

17. Lee, S.; Yasutomi, K.; Nam, H.H.; Morita, M.; Kawahito, S. A Back-Illuminated Time-of-Flight Image Sensor with SOI-based Fully Depleted Detector Technology for LiDAR application. In Proceedings of the Eurosensors 2018 Conference, Graz, Austria, 9–12 September 2018.
18. Sawada, T.; Ito, K.; Nakayama, M.; Kawahito, S. A range-shift technique for TOF range image sensors. *IEEE Trans. Sens. Micromach.* **2009**, *129*, 421–425. [[CrossRef](#)]
19. Kawahito, S.; Yasutomi, K.; Mars, K.; Kagawa, K.; Aoyama, S. Hybrid Time-of-Flight Range Image Sensors Using High-Speed Multiple-Tap Charge Modulation Pixels. In Proceedings of the International Display Workshops INP2-2, Nagoya, Japan, 12–14 December 2018.
20. Stefanov, K.D.; Clarke, A.S.; Ivory, J.; Holland, A.D. Fully Depleted, Monolithic Pinned Photodiode CMOS Image Sensor Using Reverse Substrate Bias. In Proceedings of the 2017 International Image Sensor Society (IISW), Hiroshima, Japan, 30 May–2 June 2017; pp. P109–P112.
21. Stefanov Konstantin, D.; Clarke Andrew, S.; Holland Andrew, D. Fully Depleted Pinned Photodiode CMOS Image Sensor with Reverse Substrate Bias. *IEEE Electron Device Lett.* **2017**, *38*, 64–66. [[CrossRef](#)]
22. Lauxtermann, S.; Vangapally, V. A Fully Depleted Backside Illuminated CMOS Imager with VGA Resolution and 15-micron Pixel Pitch. In Proceedings of the International Image Sensor Workshop (IISW), Snowbird, UT, USA, 12–16 June 2013.
23. Suss, A.; Wu, L.; Bacq, J.-L.; Spagnolo, A.; Coppejans, P.; Motsnyi, V.; Haspelslagh, L.; Borremans, J.; Rosmeulen, M. A Fully Depleted 52 μm GS CIS Pixel with 6 ns Charge Transfer, 7 e⁻rms Read Noise, 80 $\mu\text{V}/\text{e}^{-}\text{CG}$ and >80% VIS-QE. In Proceedings of the International Image Sensor Workshop (IISW), Snowbird, UT, USA, 12–16 June 2013; pp. R402–R405.
24. Popp, M.; Coi, B.D.; Huber, D.; Ferrat, P.; Ledergerber, M. High speed, backside illuminated 1024 \times 1 line imager with charge domain frame store in Espros Photonic CMOSTM technology. In Proceedings of the International Image Sensor Workshop (IISW), Snowbird, UT, USA, 12–16 June 2013.
25. Arai, Y.; Miyoshi, T.; Unno, Y.; Tsuboyama, T.; Terada, S.; Ikegami, Y.; Ichimiya, R.; Kohriki, T.; Tauchi, K.; Ikemoto, Y.; et al. Developments of SOI pixel process technology. *Nucl. Instrum. Methods Phys. Res. A* **2011**, *636*, S31–S36. [[CrossRef](#)]
26. Kamehama, H.; Kawahito, S.; Shrestha, S.; Nakanishi, S.; Yasitomi, K.; Takeda, A.; Tsuru, T.G.; Arai, Y. A low-noise X-ray astronomical silicon-on-insulator pixel detector using a pinned depleted diode structure. *Sensors* **2018**, *18*, 27. [[CrossRef](#)] [[PubMed](#)]
27. Miyoshi, T.; Arai, Y.; Chiba, T.; Fujita, Y.; Hara, K.; Honda, S.; Igarashi, Y.; Ikegami, Y.; Ikemoto, Y.; Kohriki, T.; et al. Monolithic pixel detectors with 0.2 μm FD-SOI pixel process technology. *Nucl. Instrum. Methods Phys. Res. A* **2013**, *732*, 530–534. [[CrossRef](#)]



© 2019 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (<http://creativecommons.org/licenses/by/4.0/>).