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Frequency-Adaptive Modified Comb-Filter-Based Phase-Locked Loop for a Doubly-Fed Adjustable-Speed Pumped-Storage Hydropower Plant under Distorted Grid Conditions

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Abstract: The control system of a doubly-fed adjustable-speed pumped-storage hydropower plant needs phase-locked loops (PLLs) to obtain the phase angle of grid voltage. The main drawback of a comb-filter-based phase-locked loop (CF-PLL) is the slow dynamic response. This paper presents a modified comb-filter-based phase-locked loop (MCF-PLL) by improving the pole-zero pattern of the comb filter, and gives the parameters' setting method of the controller, based on the discrete model of MCF-PLL. In order to improve the disturbance resistibility of MCF-PLL when the power grid's frequency changes, this paper proposes a frequency-adaptive modified, comb-filter-based, phase-locked loop (FAMCF-PLL) and its digital implementation scheme. Experimental results show that FAMCF-PLL has good steady-state and dynamic performance under distorted grid conditions. Furthermore, FAMCF-PLL can determine the phase angle of the grid voltage, which is locked when it is applied to a doubly-fed adjustable-speed pumped-storage hydropower experimental platform.

Keywords: adjustable speed pumped storage hydropower plant; distorted grid conditions; FAMCF-PLL; versa module eurocard (VME) bus

1. Introduction

Pumped-storage hydropower plants (PSHP) are the most widely-used energy storage technology for large-scale energy storage levels, as it has the characteristics of being rapid, effective, economical, and reliable [1,2]. In recent years, along with the rapid growth of intermittent renewable energy sources, demands for power supply quality and reliability have become stricter. As large-capacity, reversible, pump-turbine manufacturing technology, and high-power converter technology, advance, adjustable-speed pumped-storage technology has become the optimal scheme for pumped-storage power plants. The adjustable-speed, pumped-storage technology has more benefits than constant-speed pumped storage power stations, such as faster grid support in the generating mode and power/frequency regulating ability in the pumping mode. Generally, the installed capacity of pumped-storage plants can reach hundreds of megawatts. Simultaneously, the AC excitation converter is about 20% of the motor capacity and can reach tens of megawatts. Currently, the thyristor based cycloconverter is the most widely-used converter topology of doubly-fed adjustable-speed pumped storage plants, due to the development of the power electronic devices, control strategy, etc. [3–5]. The cycloconverter-based adjustable speed pumped-storage hydropower plants consist of a three-phase breaker, doubly-fed induction machine (DFIM), stator and rotor transformers, and cycloconverter. The DFIM's stator side is connected directly to the stator transformer's secondary

winding via the three-phase breaker. In addition, the DFIM's rotor side is connected to the rotor transformer's secondary winding via the cycloconverter. Furthermore, the three-phase grid voltage connects the DFIM's stator winding in order to build an AC magnetic field, synchronized with the grid frequency, which is constant under a balanced, three-phase system. Therefore, the rotor's mechanical rotating frequency can be adjusted by means of controlling the slip frequency. Meanwhile, the adjustable-speed, pumped-storage hydropower plant can operate in a certain range of variable speeds while maintaining the synchronized operation of grid voltage. The configuration of the cycloconverter-based adjustable-speed pumped-storage hydropower plant is shown in Figure 1.

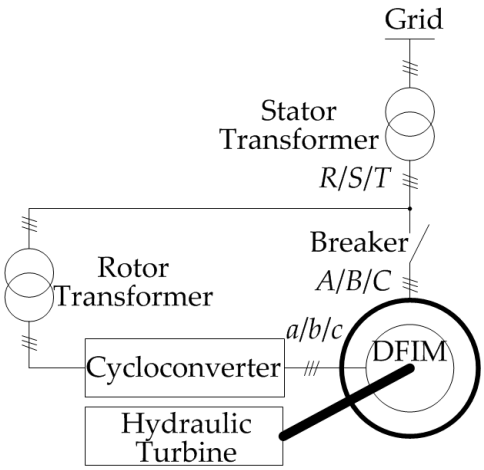

Figure 1. Schematic diagram of the adjustable-speed, pumped-storage hydropower plant.

Phase-locked loops (PLLs) are the most widely-used synchronization technique in the field of grid-connected power converters [6–12]. PLLs are typically composed of a phase detector (PD), loop filter (LF), and a voltage-controlled oscillator (VCO) [13]. A major challenge of PLLs is how to quickly and accurately estimate the phase angle and frequency when the grid voltage is distorted. To overcome this challenge, combining filtering techniques into the structure of PLLs has been proposed in the literature [13–24]. Reference [14] used a double, or more synchronous reference frame (DSRF/MSRF), to realize the decoupling between the fundamental negative sequence and the positive sequence components, and then locking the phase angle by extracting the fundamental positive sequence component, which can realize a fast and dynamic response. However, this scheme suffers from a high computational burden under harmonically-distorted grid conditions. The delayed signal cancellation (DSC) based PLL can obtain good, steady-state performance, but it is difficult to balance the contradiction between dynamic performance and the amount of calculations [15]. The second-order generalized integral (SOGI) based PLL has a strong, steady-state performance and a fast and dynamic response, but the digital implementation is complex [16,17]. The first-order comb filter (CF) is a linear-phase, finite-impulse-response (FIR) filter that can realize the ideal low-pass filter (LPF) characteristic, and is a widely-used technique in PLLs due to its simple digital realization and low computational burden [18–25]; furthermore, the first-order CF is equivalent to a moving average filter (MAF). In Reference [22], small-signal modeling of an SRF-PLL with an MAF-based prefiltering was introduced so as to compensate for the phase and amplitude errors of MAF-PLL in the presence of frequency drifts. However, this scheme results in a complicated design procedure and a high digital implementation cost. As indicated in Reference [24], the frequency-dependent attenuation characteristic is a practical challenge of MAFs, and some possible solutions to overcome this challenge were mentioned; however, frequency adaptive digital realization and hardware implementation were not considered in Reference [24].

This paper presents a CF transfer function and schematic diagram for CF-PLL in Section 2; the major problem associated with CF-PLL is the slow dynamic response characteristic. Section 3

proposes a modified comb filter (MCF) based PLL and its parameter setting method, based on the discrete model of MCF-PLL. Then, FAMCF-PLL and its digital implementation scheme are proposed in order to enhance the disturbance resistibility when the power grid's frequency changes. The adjustable-speed, pumped-storage power plant's excitation control system, based on the VME bus, and experimental results, are presented in Section 4 to validate the theoretical studies. Conclusions are drawn in the final section.

2. CF-PLL

The CF transfer function can be described as [18]:

$$G_{\mathrm{CF}}(s) = \frac{1 - e^{-T_w s}}{T_w s} \tag{1}$$

where T_w is the window length of CF.

The transfer function (Equation (1)) indicates that the CF's transient response time is equal to its window length. Assuming that the window length of the CF contains N samples of its input signal, and $N = T_w/T_s$, T_s is the control system's sampling time. The transfer function and the pole-zero expression of CF in the z-domain can be obtained as:

$$G_{\mathrm{CF}}(z) = \frac{1}{N}\frac{1 - z^{-N}}{1 - z^{-1}} = \frac{1}{N}\prod_{k=1}^{N}\frac{z - z_k}{z - p_1} \tag{2}$$

By substituting $z = e^{j\omega}$ into Equation (2)

$$G_{\mathrm{CF}}(e^{j\omega}) = \frac{1}{N}\prod_{k=1}^{N}\frac{e^{j\omega} - e^{j(2\pi\cdot k/N\cdot T_s)}}{e^{j\omega} - e^{j(2\pi/N\cdot T_s)}} \tag{3}$$

A schematic diagram of CF-PLL is shown in Figure 2. The PD is composed of a Clarke transformation and park transformation, converting the three-phase grid voltage, u_a, u_b, u_c, into DC component u_d and u_q under the synchronous rotating reference frame. In addition, u_d contains the input voltage's amplitude, and u_q contains the input voltage's phase angle error. Then, CF extracts the DC components of u_d and u_q, blocking the sinusoidal disturbances of integer multiples of the disturbance frequency. Following that, u_q is changed into a per-unit value and is transferred to the LF. The estimated angular frequency consists of the grid voltage's angular frequency and the estimate angular frequency error (proportional integral regulator output). Furthermore, the estimated phase angle is obtained by integrating the estimated angular frequency by means of the VCO. Finally, the estimated phase angle is sent to the park transformation as a rotation transform angle.

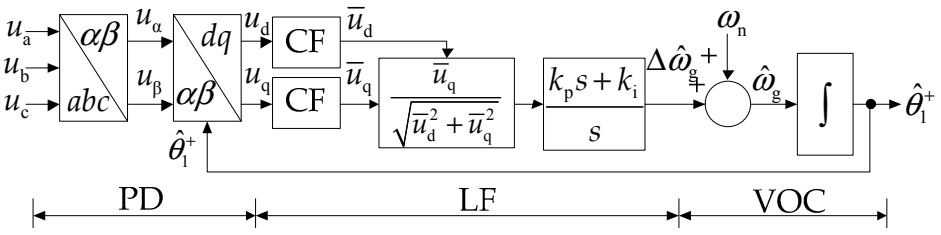

Figure 2. Schematic diagram of CF-PLL.

Generally, the disturbance frequency of CF is equal to twice that of the fundamental grid voltage's frequency (T_w = 0.01 s). At the same time, assuming that the sampling frequency of the control system is 10 kHz (T_s = 0.0001 s), then, selection of the parameters of the PI regulator is done according to the symmetrical optimum method [23]: k_p = 83.3 and k_i = 2893.5. The bode plot of the open-loop transfer

function of the CF-PLL is shown in Figure 3. It can be seen that the CF-PLL has a unity gain at zero frequency and zero gain, at the notch frequencies 100 m (m = 1, 2, 3, ...) Hz. Therefore, CF-PLL can pass a DC component and completely block the notch frequency components. In other words, CF-PLL can block the sinusoidal disturbances of integer multiples of the disturbance frequency $1/T_w$. In addition, Figure 3 shows that CF-PLL has a phase margin (PM) of 43.3° and a gain margin (GM) of 14.1 dB, ensuring the stability of CF-PLL. The cut-off frequency of CF-PLL is $2\pi \cdot 13.8$ rad/s, which indicates that the dynamic response is slow, which is the drawback of CF-PLL.

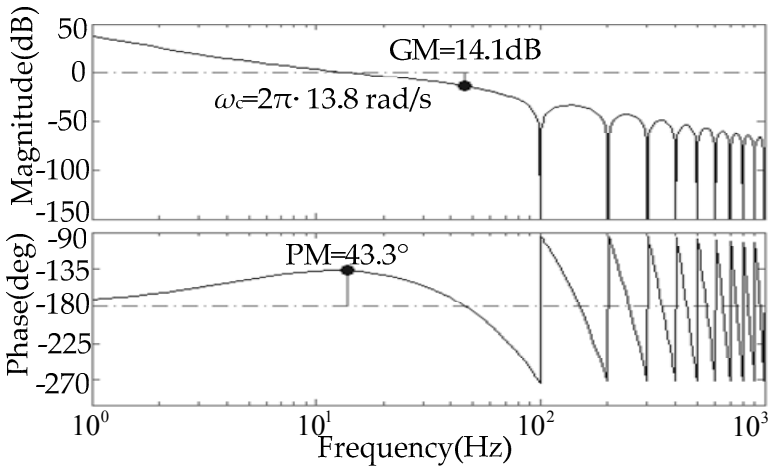

Figure 3. Bode plot of the open-loop transfer function of CF-PLL; N = 100.

3. FAMCF-PLL

3.1. MCF-PLL

In order to improve the dynamic response of CF-PLL, this paper proposes MCF-PLL by introducing N poles and one zero when the sampling order of CF is N. The transfer function and pole-zero expression of MCF in the z-domain are

$$G_{\mathrm{MCF}}(z) = \frac{K}{N}\frac{1-z^{-N}}{1-z^{-1}}\frac{1-\alpha\cdot z^{-1}}{1-(\alpha\cdot z^{-1})^{N}} = \frac{K}{N}\prod_{k=1}^{N+1}\frac{z-z_k}{z-p_k} \tag{4}$$

where α is attenuation factor, $0 < \alpha < 1$. K is the gain factor, $K = (1-\alpha^N)/(1-\alpha)$.

By substituting $z = e^{j\omega}$ into Equation (4)

$$G_{\mathrm{MCF}}(e^{j\omega}) = \frac{K}{N}\prod_{k=1}^{N+1}\frac{e^{j\omega}-z_k}{e^{j\omega}-p_k} = \frac{K}{N}\prod_{k=1}^{N+1}\frac{e^{j\omega}-e^{j[2\pi\cdot k/(N+1)\cdot T_s]}}{e^{j\omega}-\alpha\cdot e^{j[2\pi\cdot k/(N+1)\cdot T_s]}} \tag{5}$$

When the frequency is ω_m (m = 1, 2, ..., N + 1), $e^{j\omega m} = z_m = p_m$. MCF has N + 1 zeros and N + 1 poles when the sampling order is N. Moreover, MCF has a unity gain at zero frequency, $N-1$ zeros, and $N-1$ poles at notch frequency. Selecting N = 10, the pole-zero pattern of MCF is shown in Figure 4 when α = 0.9, 0.95, and 0.99. It can be seen that CF has 10 zeros and 1 pole. On the other hand, MCF has 11 poles and 11 zeros by introducing 10 poles and 1 zero at the CF frequency. The distance between the pole-zero pattern of CF and MCF becomes smaller as the attenuation factor increases. If α = 1, MCF turns into an all-pass filter. A bode plot of the open-loop transfer function of MCF-PLL, when selecting different α values, is shown in Figure 5. The phase and gain margins of MCF-PLL become larger as the attenuation factor increases. This paper selects α = 0.99, and MCF-PLL has a phase margin of 45°, gain margin of 17.3 dB, and a cutoff frequency of $2\pi \cdot 36$ rad/s. Compared with CF-PLL, MCF-PLL improves the dynamic response on the premise of maintaining stability.

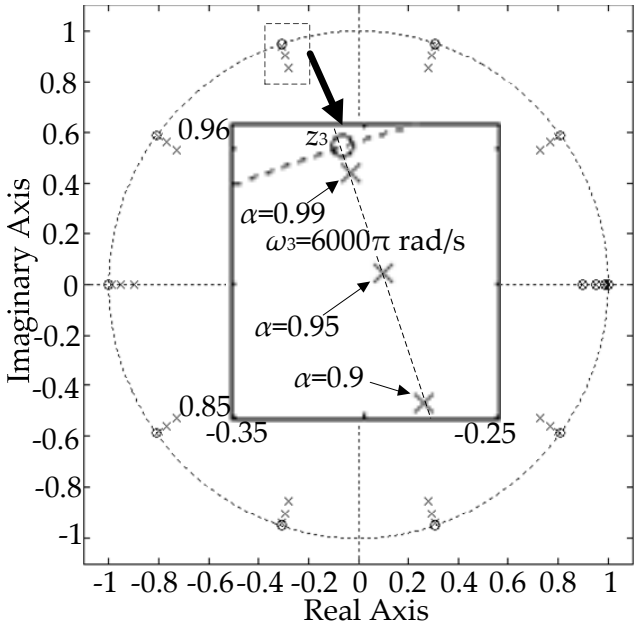

Figure 4. The z-plane, pole-zero pattern of MCF, with N = 10.

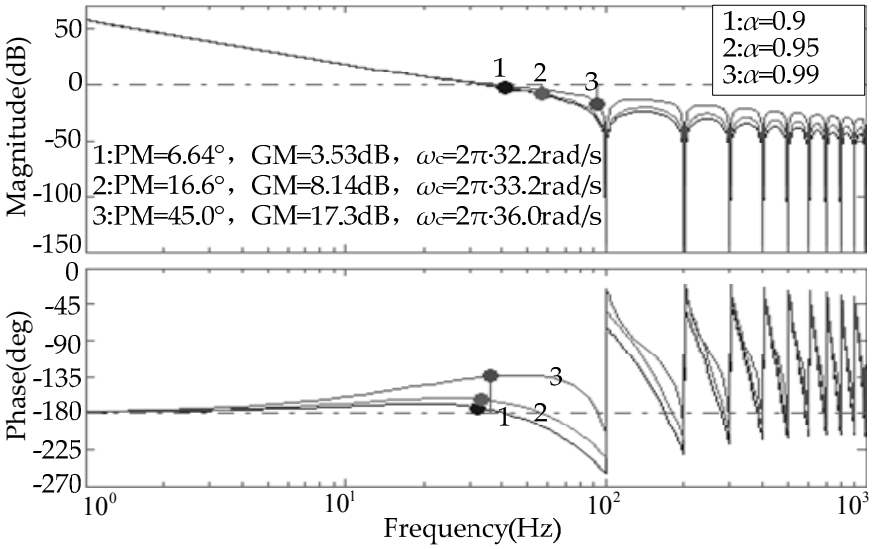

Figure 5. Bode plot of the open-loop transfer function of MCF-PLL, with N = 100.

3.2. Discrete Model of FAMCF-PLL

Assuming the three-phase grid voltage

$$\begin{cases} u_a = \sum\limits_{i=1,5,7,\ldots} \left[U_i^+ \cos\left(\theta_i^+\right) + U_i^- \cos\left(\theta_i^-\right)\right] \\ u_b = \sum\limits_{i=1,5,7,\ldots} \left[U_i^+ \cos\left(\theta_i^+ - \frac{2\pi}{3}\right) + U_i^- \cos\left(\theta_i^- + \frac{2\pi}{3}\right)\right] \\ u_c = \sum\limits_{i=1,5,7,\ldots} \left[U_i^+ \cos\left(\theta_i^+ + \frac{2\pi}{3}\right) + U_i^- \cos\left(\theta_i^- - \frac{2\pi}{3}\right)\right] \end{cases} \tag{6}$$

where U_i^+ and U_i^- represent the positive and negative sequence amplitudes of the grid voltage's k order harmonic, respectively. θ_i^+ and θ_i^- represent the positive and negative sequence phase angles of the grid voltage's k order harmonic, respectively.

Equation (6) can be rewritten in the $\alpha\beta$ reference frame using the Clarke transformation

$$\begin{cases} u_\alpha = \sum\limits_{i=1,5,7,\ldots} \left[U_i^+ \cos\left(\theta_i^+\right) + U_i^- \cos\left(\theta_i^-\right)\right] \\ u_\beta = \sum\limits_{i=1,5,7,\ldots} \left[U_i^+ \sin\left(\theta_i^+\right) - U_i^- \sin\left(\theta_i^-\right)\right] \end{cases} \tag{7}$$

Equation (7) can be rewritten in the dq reference frame by using the park transformation

$$\begin{cases} u_d = \sum\limits_{i=1,5,7,\ldots} \left[U_i^+ \cos\left(\theta_i^+ - \hat{\theta}_1^+\right) + U_i^- \cos\left(\theta_i^- + \hat{\theta}_1^+\right)\right] \\ u_q = \sum\limits_{i=1,5,7,\ldots} \left[U_i^+ \sin\left(\theta_i^+ - \hat{\theta}_1^+\right) - U_i^- \sin\left(\theta_i^- + \hat{\theta}_1^+\right)\right] \end{cases} \tag{8}$$

When FAMCF-PLL completes the grid voltage phase locked, the phase error ($\delta = \omega t + \theta_1^+ - \theta_u \approx 0$, Equation (8)) can be simplified as:

$$\begin{cases} u_d = U_1^+ \cos\delta + f_d\left(2\omega_g, 4\omega_g, 6\omega_g, \ldots\right) \\ u_q = U_1^+ \sin\delta + f_q\left(2\omega_g, 4\omega_g, 6\omega_g, \ldots\right) \end{cases} \tag{9}$$

The disturbance frequency of FAMCF is equal to twice that of the fundamental grid voltage's frequency, T_w = 0.01 s. The grid voltages in the d_q reference frame are obtained

$$\begin{cases} \overline{u}_d = U_1^+ \cos\delta \\ \overline{u}_q = U_1^+ \sin\delta \end{cases} \tag{10}$$

Then, converting the grid voltages' q axis component into per-unit value expression

$$\overline{u}_q^* = \frac{\overline{u}_q}{\sqrt{\overline{u}_d^2 + \overline{u}_q^2}} = \sin\delta \approx \delta \tag{11}$$

The schematic diagram of the MCF-PLL discrete model is shown in Figure 6. The transfer function of MCF in the z-domain is given by Equation (4). The transfer function of the PI controller in the z-domain is:

$$G_{\mathrm{PI}}(z) = k_p + \frac{k_i \cdot T_s}{z-1} \tag{12}$$

where k_p is the proportionality coefficient of the PI controller and k_i is the integral coefficient of the PI controller.

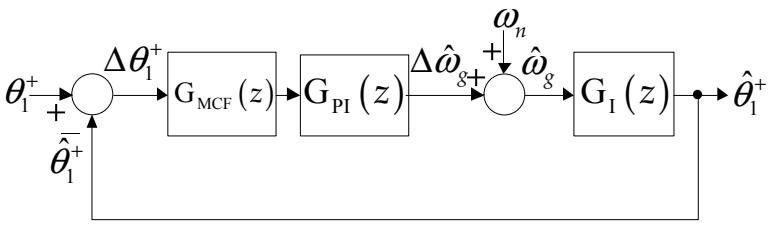

Figure 6. Schematic diagram of MCF-PLL discrete model.

The transfer function of the integrator in the z-domain is:

$$G_{\mathrm{I}}(z) = \frac{T_s}{z-1} \tag{13}$$

Selecting a phase margin within the range of 30°~60°, to guarantee the stability of the control system, is recommended. This paper selected PM = 45°, $\omega_c = 2\pi \cdot 36$ rad/s. The discrete model of MCF-PLL is set up in MATLAB/Simulink (MathWorks, Natick, MA, USA), based on the Equations (4), (12), and (13). Then, the values of the phase margin and the cut-off frequency in the

proportional integral derivative (PID) Tuner were set. The parameters of the proportional integral (PI) regulator are obtained: k_p = 194.15, k_i = 28,008.07.

3.3. FAMCF-PLL Realization

The MCF-PLL cannot completely block the disturbance components if the grid voltage frequency changes [23–25]. In such cases, MCF-PLL needs to adjust the sampling order, according to the variations in the grid voltage's frequency. Then, the MCF sampling order, N, is given by means of the nearest integer approach

$$N = \text{round}(T_w/T_s) = \text{round}\left(\pi f_s/\hat{\omega}_g\right) \tag{14}$$

where T_s is the control system's sampling period. $\hat{\omega}_g$ is the estimated angular frequency of MCF-PLL.

Figure 7 shows the digital implementation schematic diagram of FAMCF-PLL. It can be seen that FAMCF-PLL can be easily implemented. Equation (15) presents the digital implementation method of FAMCF-PLL

$$\begin{cases} y(k) = \frac{1}{N}\left[\sum\limits_{i=0}^{k-1} x(k-i) - \sum\limits_{i=N}^{k-1} x(k-i)\right] \\ \overline{x}(k) = K\left[\sum\limits_{i=0}^{k-N} \alpha^N \cdot y(k-i) - \sum\limits_{i=0}^{k-N-1} \alpha \cdot y(k-i)\right] \end{cases} \tag{15}$$

where $x(k)$ is the input variable of FAMCF-PLL at k sample time. $y(k)$ is the output variable of FAMCF-PLL at k sample time.

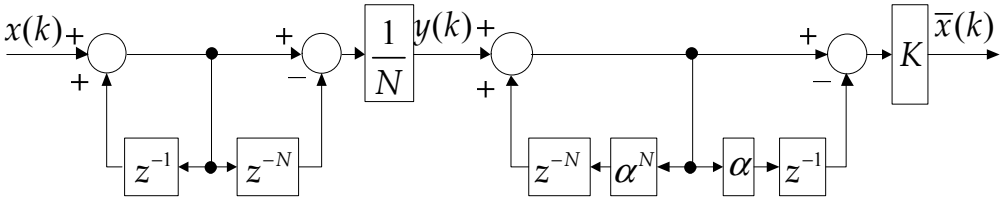

Figure 7. Digital implementation schematic diagram of FAMCF-PLL.

The FAMCF-PLL digital implementation scheme in this paper consists of four steps:

(1) At sample time k, adding the grid voltages' q axis component, x (k), to A ($i-1$); then saving the result to array A (i).
(2) Computing sample order N using Equation (14), $y(k) = [A(k) - A(k-N)]/N$.
(3) Adding y (k) to $\alpha^N \cdot B(k-N)$, then saving the result to array B (i).
(4) $\overline{x}(k) = [B(k) - \alpha \cdot B(k-1)]/K$.

4. Experimental Results

The proposed FAMCF-PLL scheme for doubly-fed adjustable-speed pumped storage plants was carried out on the VME bus based control system (RX7i PAC Systems, General Electric Company, Fairfield, CT, USA). The control system consisted of a CPU board (VMIVME-7807, General Electric Company), an encoder signal board, an analog output board (VMIVME-4140, General Electric Company) and three current control boards. The current control board was implemented on a DSP (TMS320F28335, Texas Instruments Company, Dallas, TX, USA) and a FPGA (EPF10K30A, Altera Company, San Jose, CA, USA). The current control board algorithms completed the current close loop control, linear trigger, AD samplings, and generated the firing pulses. The virtual distorted grid conditions, FAMCF-PLL, the Clarke transformation, park transformation, and power calculation algorithms were developed in IOWorks using the programming unit. Furthermore, the control algorithms were downloaded to the CPU board using an Ethernet connector. All results were obtained under 10-kHz sampling frequency experimental conditions. Finally, the internal variables

were exported by the analog output board and were monitored using an oscilloscope (DPO4034B, Tektronix Company, Beaverton, OR, USA). Figure 8 shows images of the experimental platform and the control diagram of the system. The DFIM's parameters are shown in the Appendix A.

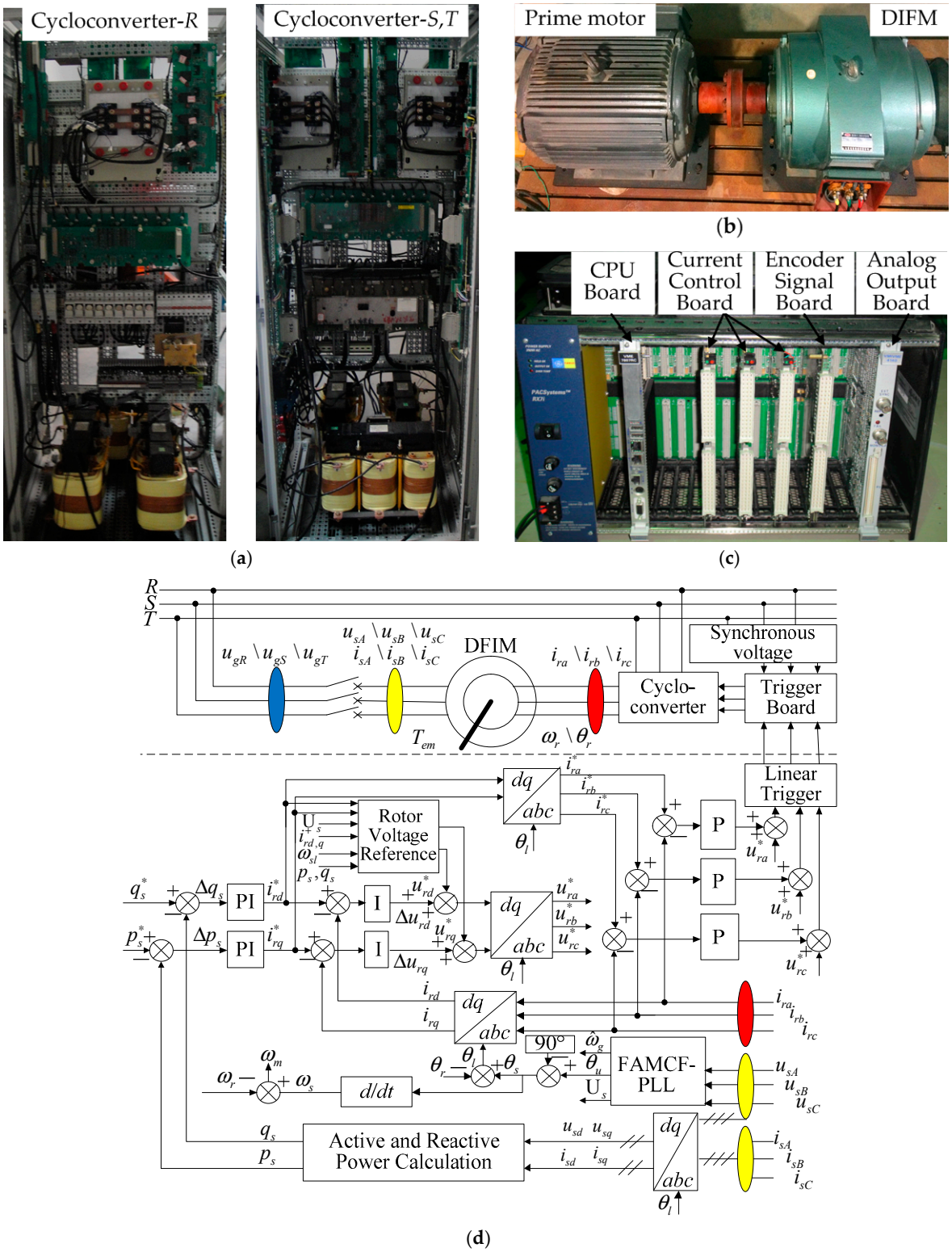

Figure 8. Images of the experimental platform. (**a**) Cycloconverter power cabinet; (**b**) DIFM and prime motor; (**c**) Control system; (**d**) Control diagram of the doubly-fed, adjustable-speed, pumped storage hydropower plant.

The paper selects CF-PLL and MCF-PLL as the control groups to verify the steady-state and dynamic performances of the proposed FAMCF-PLL under the following conditions:

- Condition 1: 40 ms, the grid voltage undergoes a frequency step change of +5 Hz.
- Condition 2: 40 ms, the grid voltage undergoes a phase angle jump of +40°.
- Condition 3: 40 ms, the grid voltage undergoes a harmonics injection of 20% fifth and 10% seventh harmonic components. At 100 ms, the grid voltage undergoes a frequency step change of +5 Hz.
- Condition 4: 40 ms, the voltage amplitude of phase *A* sags by 50% and the voltage amplitude of phase *B* sags by 30%. At 100 ms, the grid voltage undergoes a frequency step change of +5 Hz.
- Condition 5: 40 ms, the frequency step change, phase angle jump, harmonics injection, and voltage sag occur at the same time.

Figure 9a shows the experimental result when the grid voltage underwent a frequency step change of +5 Hz. It can be seen that the CF-PLL suffered from a slow transient response. However, the steady-state characteristics of the MCF-PLL and FAMCF-PLL were as good as those achieved by CF-PLL. Moreover, the proposed FAMCF-PLL could obtain better steady-state performance and a faster transient response than CF-PLL and MCF-PLL. Figure 9b shows the experimental results when the grid voltage underwent a phase angle jump of +40°. It can be observed that the transient response of MCF-PLL and FAMCF-PLL were much faster than that of CF-PLL, which was similar to the experimental results in Figure 9a. Detail analyses results are shown in Table 1.

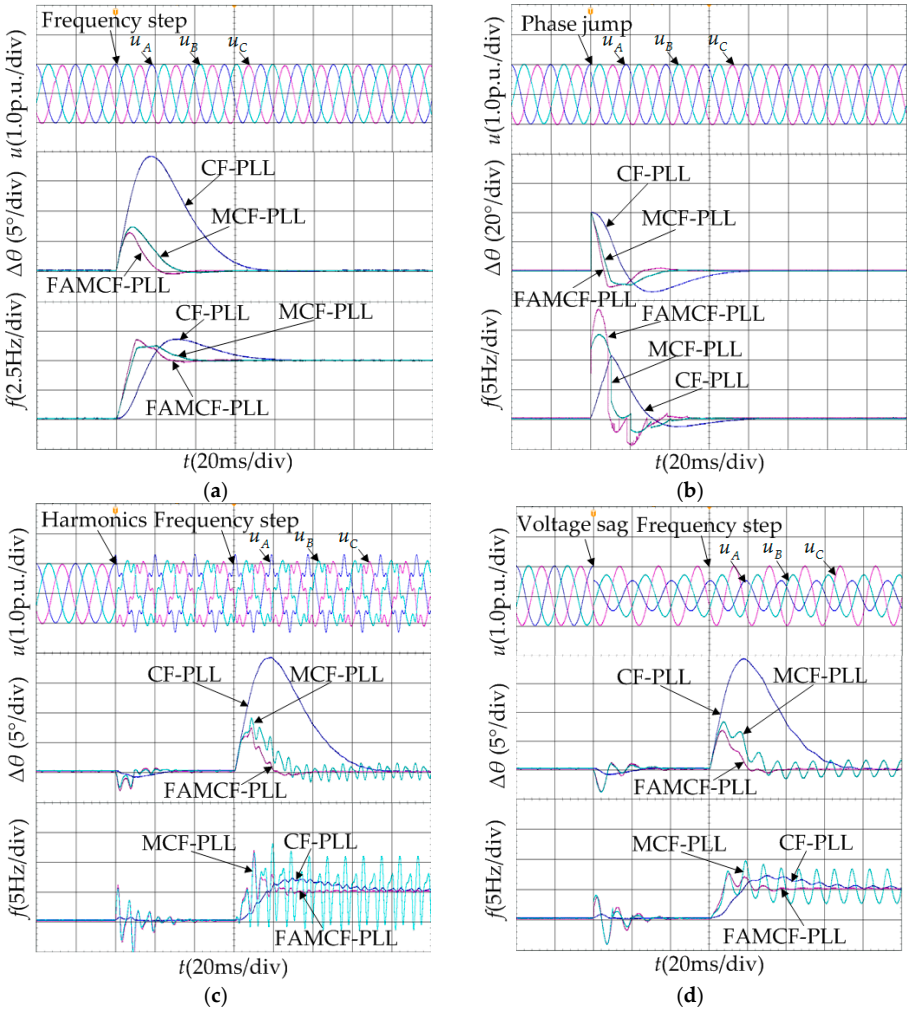

Figure 8. *Cont.*

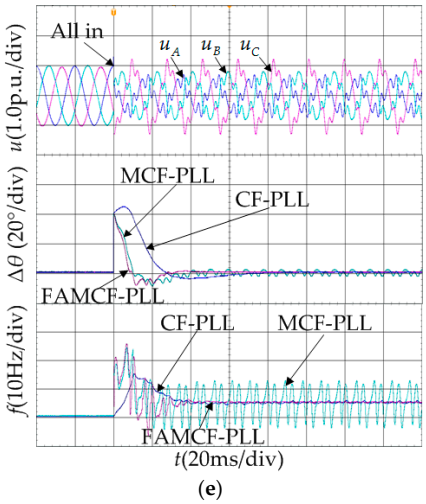

Figure 9. Experimental results of PLLs under distorted grid conditions. (**a**) Condition 1; (**b**) Condition 2; (**c**) Condition 3; (**d**) Condition 4; (**e**) Condition 5.

Table 1. Detailed experimental results of the PLLs.

Condition		CF-PLL	MCF-PLL	FAMCF-PLL
1	frequency 5% setting time/ms	66.8	33.4	24.0
	frequency overshoot/%	38.1	28.0	33.8
	peak phase error/deg	19.3	7.7	6.3
2	phase 5% setting time/ms	64.6	32.6	23.6
	phase overshoot/%	34.8	23.0	27.8
	peak frequency error/Hz	10.9	14.3	18.3
3	peak-to-peak phase error/deg	0.100	3.10	0
	peak-to-peak frequency error/Hz	1.00	12.0	0.500
4	peak-to-peak phase error/deg	0.6	3.60	0
	peak-to-peak frequency error/Hz	0.800	6.70	0.200
5	peak-to-peak phase error/deg	0.800	5.00	0
	peak-to-peak frequency error/Hz	1.20	17.2	0.700

In order to analyze the effects of the FAMCF-PLL's grid voltage's frequency variation rejection capability, the experimental results of the PLLs under comprehensive distorted grid conditions are shown in Figure 9c–e. Figure 9c shows that MCF-PLL and FAMCF-PLL had faster transient responses than CF-PLL under the distorted grid voltage, with fifth- and seventh-order harmonic components set at 20% and 10%, respectively. At 100 ms, CF-PLL and FAMCF-PLL obtained a much better disturbance rejection capability than MCF-PLL in experimental operations when the grid voltage's frequency changed. As a result, it can be observed that, both the phase errors and the frequency deviations of CF-PLL and FAMCF-PLL were much smaller than those of MCF-PLL. Figure 9d shows that both the phase errors and the frequency deviations of CF-PLL and FAMCF-PLL were much smaller than those of MCF-PLL under the unbalanced grid voltage amplitude sags and frequency changes, which was similar to the experimental results of Figure 9c. In addition, the transient response of MCF-PLL and FAMCF-PLL was much faster than that of CF-PLL. Figure 9e demonstrates that the transient response of CF-PLL was too slow to realize the phase lock. Meanwhile, MCF-PLL showed an excellent filtering capability when the grid voltage's frequency was at its nominal value. However, the phase errors and frequency deviations increased if the grid voltage's frequency changed from its nominal value. FAMCF-PLL could obtain good steady-state performance and disturbance rejection capability,

even when the grid voltage's frequency changed, owing to adaptive frequency realization. The detailed results can be found in Table 1.

Figure 10 shows the experimental results of the doubly-fed, adjustable-speed, pumped storage hydropower experimental platform under normal grid conditions. During the process of rotor acceleration, from 1425 rpm (0.9 5p.u.) to 1575 rpm (1.05 p.u.), and rotor deceleration, from 1575 rpm (1.05 p.u.) to 1425 rpm (0.95 p.u.), the proposed strategy obtained smooth rotor currents and phase sequence changes during the entire dynamic process, as shown in Figure 10a,b, respectively. In a word, the result showed that the doubly-fed, adjustable-speed system had a good performance, both under sub-synchronous, and super-synchronous, states using FAMCF-PLL.

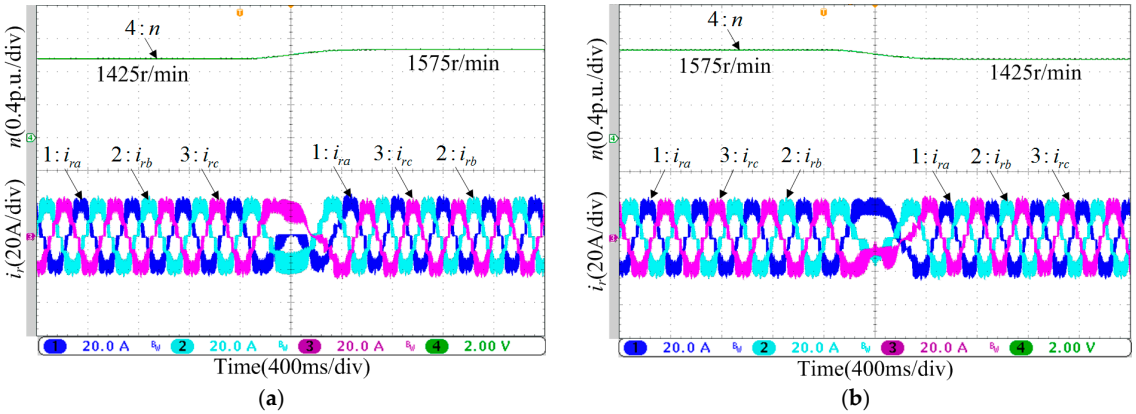

Figure 10. Experimental results of the doubly-fed, adjustable-speed, pumped storage hydropower experimental platform. (**a**) Sub-synchronous to super-synchronous; (**b**) Super-synchronous to sub-synchronous.

5. Conclusions

This paper proposed a FAMCF-PLL for doubly-fed adjustable-speed pumped storage plants, especially when grid voltage is not ideal. The proposed scheme obtained excellent disturbance rejection ability, by blocking the sinusoidal disturbances of integer multiples of the disturbance frequency, even when the grid voltage was adverse. Compared with CF-PLL and MCF-PLL, FAMCF-PLL improved the disturbance-rejection ability when the frequency of the grid voltage changed. Finally, the control system of adjustable-speed, pumped-storage power plants was built, based on the VME bus, and the experimental results validated the feasibility and effectiveness of the proposed algorithms.

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Appendix A

DFIM: S_n = 110 kVA, $U_s = U_r$ = 380 V, f = 50 Hz, n_p = 2 pole pairs, R_s = 0.0728 Ω, R_r = 0.0345 Ω, L_s = 6.57 mH, L_r = 3.27 mH, L_m = 43.93 mH.

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