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A Modified Partial Power structure for Quasi Z-Source Converter to Improve Voltage Gain and Power Rating

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Abstract: Employing partial power processing (PPP) technique for quasi Z-source converter (QZSC) a new structure of the converter is presented. Using PPP technique although eliminates electrical insolation, but permits reducing voltage and current stress at the semiconductors, if compared with full power proposals. In this work, two PPP structures are discussed: A first one, similar to the basic topology, where the output voltage of the power converter is in series with the input voltage; and a second one, where the output is in series with the capacitor of the QZSC. This minor modification, which requires no extra elements, improves the power rating, voltage gain, and requires a lower transformation ratio. An experimental prototype of the proposed converter has been tested and the results are compared with other implementations, permitting to validate the theoretical analysis as well as the advantages that this proposal provides.

Keywords: partial power processing; quasi Z-source converters; high step up converters

1. Introduction

As one of the main backbones of the power electronics industry an uncountable number of research works have been devoted to the study and design of high efficiency, low power rating, and low cost DC/DC converters for different applications such as: PV, electrical equipment, electrical vehicles, energy storage, and communication systems. Furthermore, many researches have been made to improve the performance of conventional converters. One recent technique that is giving rise to good results is based on partial power processing (PPP) [1,2]. The basic principle of this technique is based on providing part of the input power directly to the output, meanwhile the rest is processed by the converter [1–13]. The main advantage of this technique is to level down the power rating of the elements as less power is handled by the converter. This is achieved without requiring to add or remove any element.

The main feature of the PPP technique is found in the connection between the source and the load [1]. The layout available in Figure 1 shows the two main topologies. The first type (Figure 1a), which is appropriate for boosting, has an output voltage equals to the sum of the source voltage and the output voltage of the converter [1,3–7]. The second one, shown in Figure 1b, is appropriate for buck application, and builds the output voltage taking the difference between system and converter input voltages [8,9].

Isolation is a big challenge in PPP applications [1,2,10]. However non-isolated converters can be considered in some cases [3–5]. For instance, in [11] a simple and commercially available non-isolated

partial power (PP) boost converter for PV systems was integrated. Based on [12], the performance of this converter does not follow the PP method and acts like a full power converter (FPC). As described in [1,3,4], if the average current passing through the direct power path is zero, the system's performance is similar to a full power processing converter. A dual input non-isolated partial power converter (PPC) was introduced in [13–15], which employs two similar PPC.

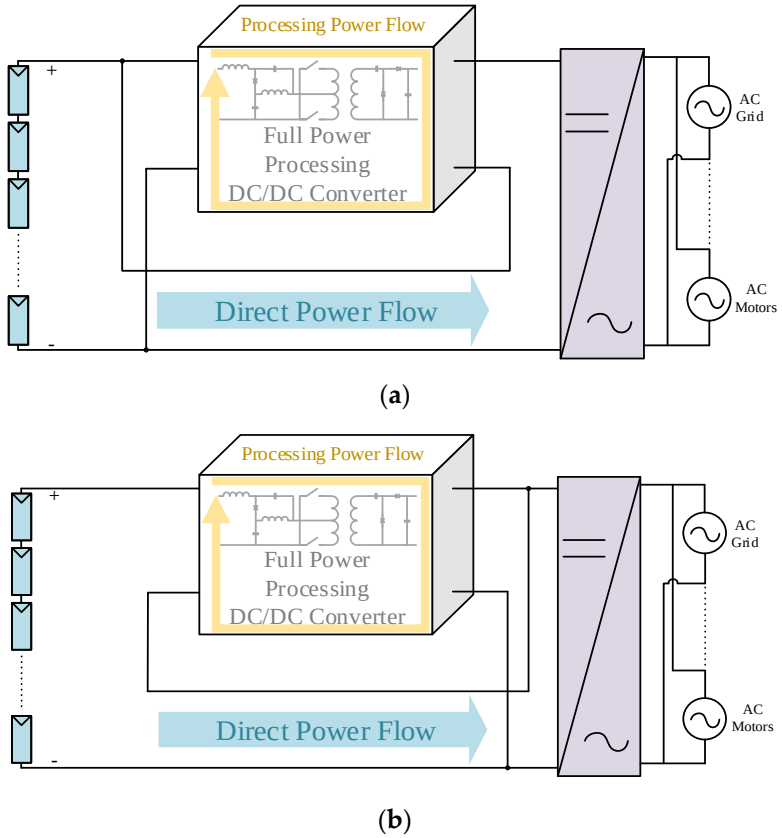


Figure 1. Basic structure of partial power processing (PPP system): (**a**) Input parallel output series, (**b**) Input series output parallel.

On the other hand, impedance network converters are widely investigated for low voltage renewable energy source applications. The main advantage of these converters lays on the fact that they can provide a high voltage step up; and the other merit is short circuit immunity [16–25]. The PPP technique can be applied to these types of converters in order to improve their performance. Z-source converter (ZSC) which is the first proposed structure of impedance network converters, includes an inductor and a capacitor that handle the charge and discharge cycles to provide the maximum power conversion ability during the shoot through time interval [19]. However, quasi ZSC (QZSC) which has been chosen in this paper, provides some advantages compared to ZSC, including continuous input current and wider boosting range [20,25].

After defining the topology different types of switching methods can be implemented such as: Using only one switch to shoot through switching, using two or three leg H-Bridge switching topology, and push-pull switching topology [21] (Figure 2). In this case reducing the number of switches and implementing a simple control using push-pull switching, have been prioritized in the selection of the proposed converter [22].

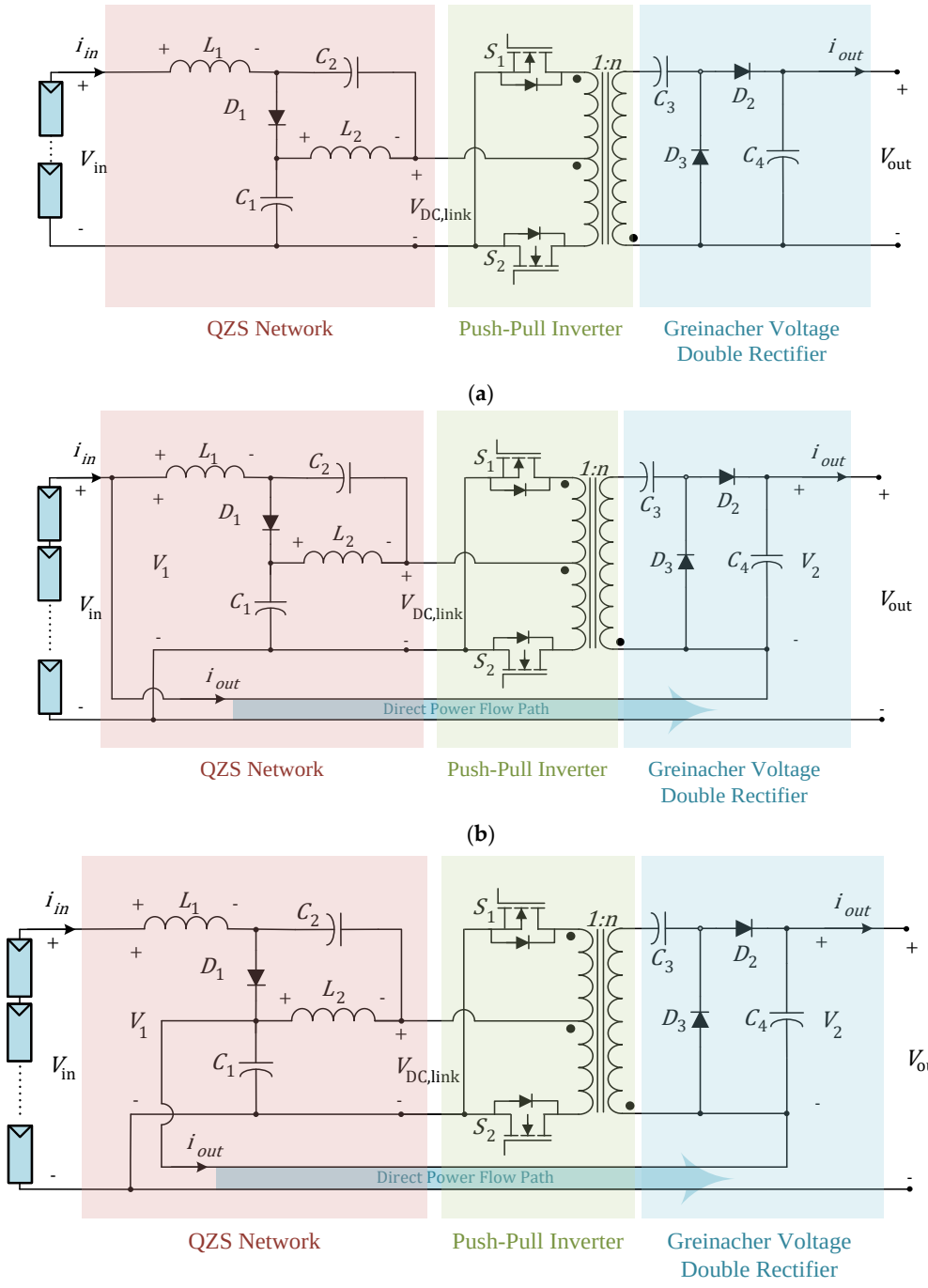


Figure 2. Equivalent circuits of the converters: (**a**) Full power quasi Z-source converter (QZSC), (**b**) Basic PPP QZSC, (**c**) Proposed PPP QZSC.

In this paper the isolated QZSC has been used with push pull switching method in the middle, as shown in Figure 2a. Two structures of PPC for this converter are presented: PP-QZSC (Figure 2b) and modified PP-QZSC (Figure 2c). The first type is based on the basic structure of PPP technique (as depicted in Figure 1a), while the structure is revised in the second one and this provides reduced voltage stress and higher voltage gain.

One of the main contributions of this paper is the use of the PPP technique for improving the voltage gain of the full power QZSC (FP-QZSC). The proposed method permits achieving a voltage gain 20% higher than basic PPP system.

In order to evaluate the performance of the modified PP-QZSC, its performance will be compared to traditional FP-QZSC and basic PP-QZSC in terms of efficiency, voltage and current stress, and voltage gain in continuous conduction mode (CCM) of operation.

2. Operation Principles and Topology Analysis of the Proposed Converter

The modified PP-QZSC in Figure 2c follows the switching sequence shown in Figure 3.

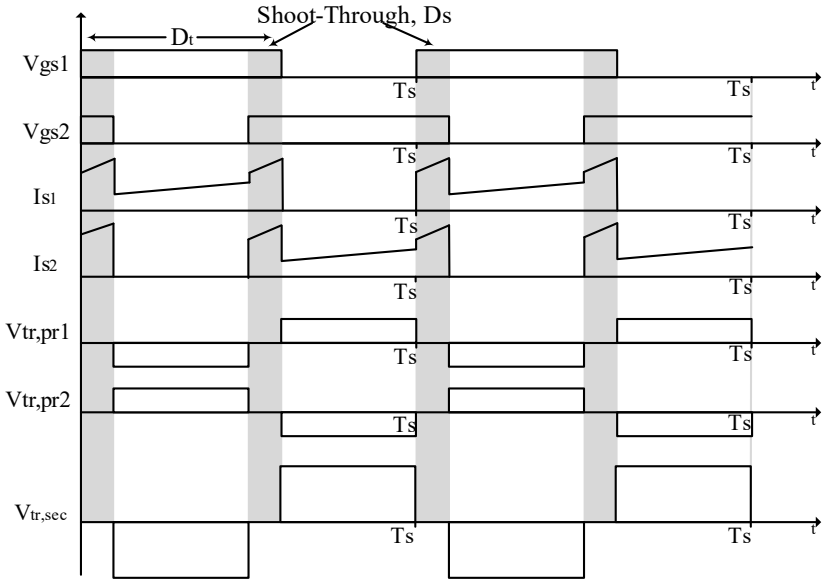


Figure 3. Equivalent circuits of the converters: (**a**) Full power QZSC, (**b**) Basic PPP QZSC, (**c**) Proposed PPP QZSC.

It should point out that in order to guarantee a good operation of the proposed converter, the duty cycle D_t should be within 50% < D_t< 75% and hence the shoot-through duty cycle D_s is $D_s = 2D_t - 1$. As by short circuiting the transformer magnetically the shoot through situation happens, the transformer design should be very accurate [22]. In this study the transformer magnetizing inductance L_M, is neglected.

Considering the sequence described in the figure, three modes of operation can be defined for modified PP-QZSC (Figure 2c). The equivalent circuits corresponding to these modes are shown in Figure 4. In the proposed converter the output voltage is the sum of the voltages at C_1 and C_4. Therefore, the output voltage can be determined as follows:

$$V_{out} = V_{C_1} + V_{C_4} \tag{1}$$

$$V_{C_1} = \frac{1 - D_s}{1 - 2D_s} V_{in} \tag{2}$$

$$V_{C_4} = \frac{2n}{1 - 2D_s} V_{in} \tag{3}$$

where, V_{out} and V_{in} is the output and input voltages and D_s stands for shoot through duty cycle. Substituting (1) and (2) into (3) and based on D_t or D_s, the converter voltage gain can be expressed as:

$$\frac{V_{out}}{V_{in}} = \frac{2n + 1 - D_s}{1 - 2D_s} = \frac{2(n + 1 - D_t)}{3 - 4D_t} \tag{4}$$

where, n is the transformer turns ratio and D_t is the duty cycle of switches. The same analysis can be considered for basic PP-QZSC and FP- QZSC which is given by (5) and (6) respectively.

$$\frac{V_{out}}{V_{in}} = \frac{2n + 3 - 4D_t}{3 - 4D_t} \tag{5}$$

$$\frac{V_{out}}{V_{in}} = \frac{2n}{3 - 4D_t} \tag{6}$$

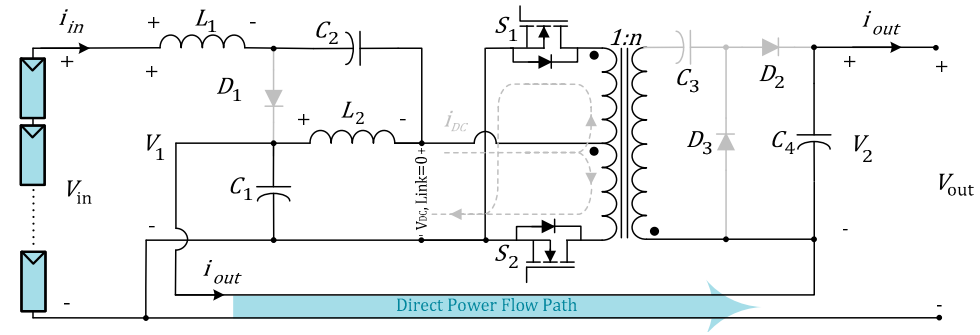
Figure 5 shows the voltage gain versus duty cycle for similar transformer turn ratio, n = 1. As it can be realized, the proposed converter with a slight difference, provides a higher voltage gain. This is translated into a lower voltage stress for all the elements, specifically for the voltage stress in the semiconductors. Moreover, the proposed converter is compared to other PP topologies such as: Boost, Full Bridge, and Flyback PPC. This figure shows the merit of PPP technique for impedance network converters.

The QZS network part of the circuit only processes two modes of operation: Shoot-through mode and non-Shoot-through mode. So, the inductor currents in steady state can be derived based on the following two modes of operation:

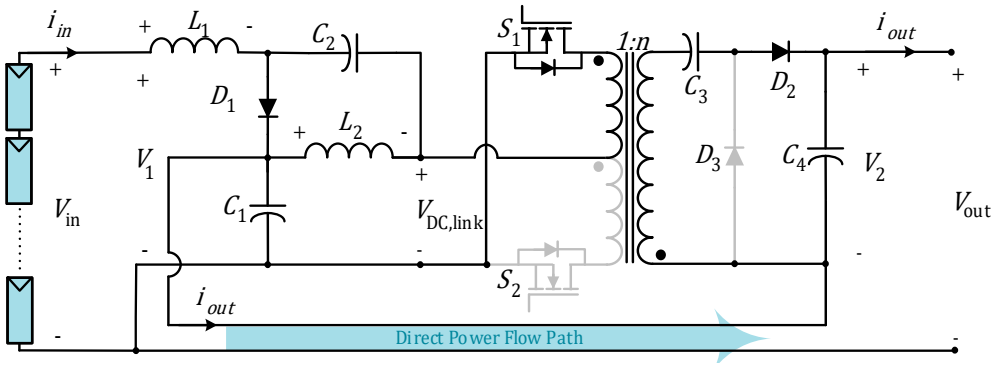
Shoot-through mode: In this stage the diode D_1 is turned off and the DC link terminals are magnetically short circuited, therefore the following equations referring to Figure 4a can be written:

$$\begin{aligned} i_{C1} &= -i_{L2} - i_{out} \\ i_{C2} &= -i_{L1} = -i_{in} \end{aligned} \tag{7}$$

where i_{in}, i_{out}, i_C, and i_L are input, output, capacitor, and inductor currents respectively.



(**a**)



(**b**)

Figure 4. *Cont.*

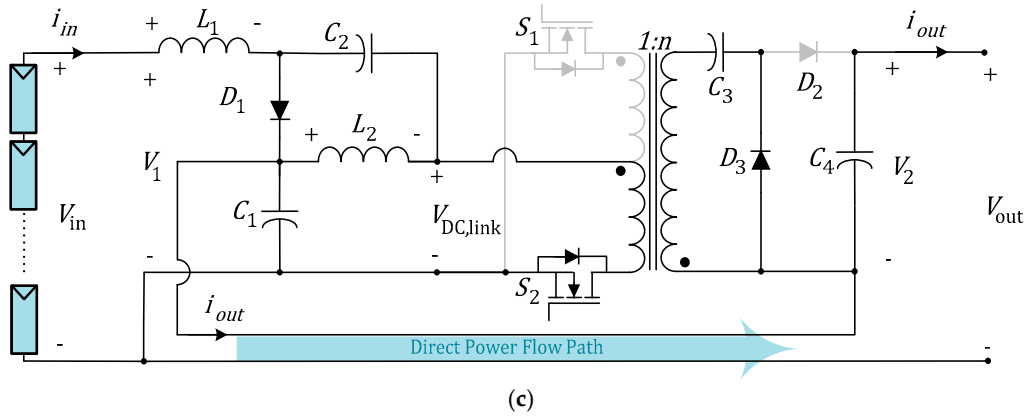


Figure 4. Operation modes of the proposed PPP QZSC: (**a**) Shoot-through mode, (**b**) Non-shoot-through and S_1 is ON, S_2 is off, (**c**) Non-shoot-through and S_2 is ON, S_1 is off.

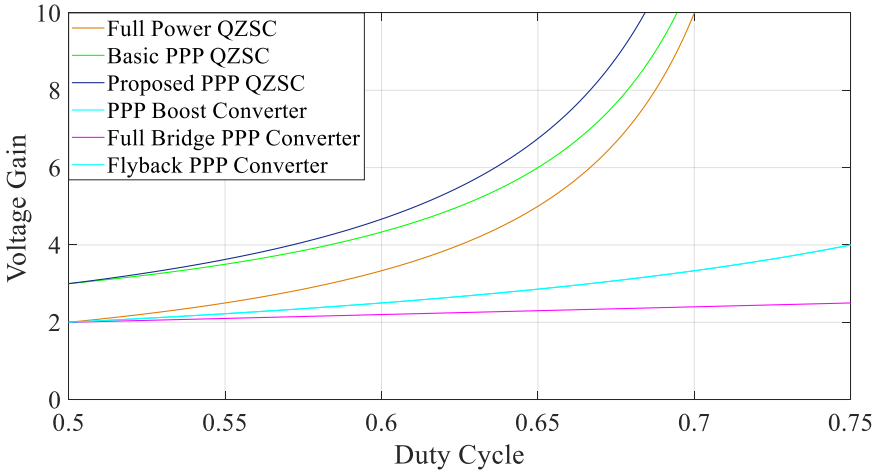


Figure 5. Voltage gain versus duty cycle for three discussed converters and PPP structures of Flyback, H-bridge, and Boost converters (Flyback and Boost have similar waveform).

Non-shoot-through mode: Based on Figure 4b or Figure 4c, the diode D_1 is turned on and inductors currents are induced to DC link terminals, so;

$$\begin{cases} i_{C_1} = i_{D_1} - i_{L_2} - i_{out} \\ i_{C_2} = i_{D_1} - i_{in} \end{cases} \tag{8}$$

where i_{D_1} is the D_1 current. According to the capacitor Amp-second balance law and shoot through duty cycle, the inductor's steady state current can be calculated as:

$$\begin{cases} I_{L_1} = I_{in} = \frac{2n+1-D_s}{1-2D_s} \cdot \frac{V_{out}}{R_{out}} = \frac{2(n+1-D_t)}{3-4D_t} \cdot \frac{V_{out}}{R_{out}} \\ I_{L_2} = I_{in} - I_{out} = \frac{2n+D_s}{1-2D_s} \cdot \frac{V_{out}}{R_{out}} = \frac{2n+2D_t-1}{3-4D_t} \cdot \frac{V_{out}}{R_{out}} \end{cases} \tag{9}$$

3. Comparison and Evaluation of Topologies

In the following, three discussed converters are compared regarding several criteria in steady state operation. The averaged model of QZSC and PP-QZSC is discussed in [26].

3.1. Voltage and Current Stress Analysis

The voltage and current stress of the semiconductor devices are shown in Table 1. Current stress equations of the converters are identically except for D_1 current stress, so overall the modified

PP-QZSC has lower current stress compared to others. Also the voltage stress of the modified PP-QZSC is reduced compared to FP-QZSC and basic PP-QZSC. Both the basic and the modified PP-QZSC have less current and voltage stresses compared to FP-QZSC. Figure 6 illustrates a comparison of the switch's voltage stress as a ratio of input voltage based on the converter voltage gain. From this figure it can be concluded that having less voltage stress in the switches results in lower switch built in conducting resistance. Also, the voltage stress of other elements such as diodes are reduced. Lower voltage stress results in lower power rating of the elements, for instance low power rated passive element like capacitor. Generally, reduced voltage and current stress of the elements, specifically active elements, can be effective for enhancing the converter's cost.

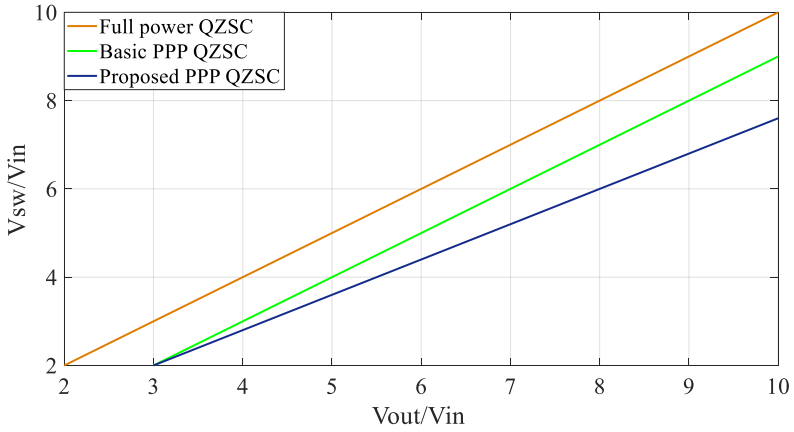


Figure 6. MOSFET voltage stress/input voltage versus voltage gain for FP-QZSC, basic PP-QZSC, and modified PP-QZSC (Transformer turn ratio = 1).

3.2. Element Design

The full bridge, half bridge, and push-pull switching topologies help the voltage and current stress to be reduced compared to single switching topologies [21]. The steady state analysis of inductors current ripples and capacitors voltage ripples indicates the size of passive elements of the converters, therefore;

$$\begin{cases} L_1 = \frac{2(2D_t-1)(1-D_t)}{4nf_s} \cdot \frac{V_{out}}{\Delta I_{L1}} \\ L_2 = \frac{2(2D_t-1)(1-D_t)}{4nf_s} \cdot \frac{V_{out}}{\Delta I_{L_2}} \end{cases} \tag{10}$$

$$\begin{cases} C_1 = \frac{(n+1-D_t)(2D_t-1)}{(3-4D_t)f_sR_{out}} \cdot \frac{V_{out}}{\Delta V_{C_1}} \\ C_2 = \frac{(n+1-D_t)(2D_t-1)}{(3-4D_t)f_sR_{out}} \cdot \frac{V_{out}}{\Delta V_{C_2}} \\ C_3 = \frac{4n+1}{2nf_sR_{out}} \cdot \frac{V_{out}}{\Delta V_{C_3}} \\ C_4 = \frac{D_t}{2f_sR_{out}} \cdot \frac{V_{out}}{\Delta V_{C_4}} \end{cases} \tag{11}$$

where, Δi_L is the inductor current ripple, ΔV_C is the capacitor voltage ripple and f_s is the switching frequency. The output voltage ripple for FP-QZSC and basic PP-QZSC are ΔV_{C_4} but for the modified PP-QZSC is the summation of ΔV_{C_1} and ΔV_{C_4}.

Table 1. Voltage and current stress comparison.

Converter		Voltage Stress	Current Stress
Switches	Full Power QZSC [22]	$\frac{1}{n} \cdot V_{out}$	$\frac{2n}{1-2D_s} \cdot \frac{V_{out}}{R_{out}}$
	Basic PPP QZSC	$\frac{2}{2n-1-2D_{s_1}} V_{out}$	$\frac{2n}{1-2D_{s_1}} \cdot \frac{V_{out}}{R_{out}}$
	Proposed PPP QZSC	$\frac{2}{2n+1-D_{s_2}} V_{out}$	$\frac{4n+1}{2\left(1-D_{s_2}\right)} \cdot \frac{V_{out}}{R_{out}}$
Diode D_1	Full Power QZSC	$\frac{1}{2n} \cdot V_{out}$	$\frac{2nV_{out}}{(1-2D_s)(1-D_s)R_{out}}$
	Basic PPP QZSC	$\frac{1}{2n+1-2D_{s_1}} V_{out}$	$\frac{2nV_{out}}{(1-2D_{s_1})\left(1-D_{s_1}\right)R_{out}}$
	Proposed PPP QZSC	$\frac{1}{2n+1-D_{s_1}} V_{out}$	$\frac{(2n+1-D_{s_2})V_{out}}{(1-2D_{s_2})\left(1-D_{s_2}\right)R_{out}}$
Diode D_2 & D_3	Full Power QZSC	V_{out}	$\frac{2}{1-2D_s} \cdot \frac{V_{out}}{R_{out}}$
	Basic PPP QZSC	$\frac{2n}{2n+2-2D_{s_1}} V_{out}$	$\frac{2}{1-2D_{s_1}} \cdot \frac{V_{out}}{R_{out}}$
	Proposed PPP QZSC	$\frac{2n}{2n+1-D_{s_2}} V_{out}$	$\frac{2n+D_{s_2}}{n\left(1-2D_{s_2}\right)} \cdot \frac{V_{out}}{R_{out}}$
Converter		**Inductor L_1**	**Inductor L_2**
Current Stress	Full Power QZSC	$\frac{2}{1-2D_s} \cdot \frac{V_{out}}{R_{out}}$	$\frac{2}{1-2D_s} \cdot \frac{V_{out}}{R_{out}}$
	Basic PPP QZSC	$\frac{2}{1-2D_{s1}} \cdot \frac{V_{out}}{R_{out}}$	$\frac{2}{1-2D_{s_1}} \cdot \frac{V_{out}}{R_{out}}$
	Proposed PPP QZSC	$\frac{2n+1-D_{s2}}{1-2D_{s_2}} \cdot \frac{V_{out}}{R_{out}}$	$\frac{2n+D_{s_2}}{1-2D_{s_2}} \cdot \frac{V_{out}}{R_{out}}$

3.3. Comparison

In terms of comparison, some parameters have been considered such as voltage gain, voltage and current stress, voltage ripple of capacitors, current ripple of inductors, power losses, transformer turn ratio, number of used elements, and efficiency. Therefore, some non-idealities of elements such as: Inductor resistance, transformer resistance, switch built in conducting resistance, and diode conducting voltage drop are considered. Also, converter no-load power loss which is caused by transformer or inductor core loss has been considered as a constant factor of output power. Other non-idealities such as capacitor equivalent series resistance (ESR) or diode resistance are neglected. Table 2 shows the converters specifications and the amount of non-ideal elements which has been considered in terms of simulation comparison.

Table 2. Prototype and Simulation parameters.

Parameters	Symbols	Value/Part no.
Output Voltage	V_{out}	90 V
Input Voltage	V_{in}	20 V
Switching Frequency	f_s	40 kHz
Duty Cycle	D_t	0.6
Transformer turn ratio	n	1:1:1
Primary and secondary resistance	R_{wp}, R_{ws}	0.01 Ω
Inductance	L_1, L_2	200 µH
Inductor resistance	R_{L_1}, R_{L_2}	0.01 Ω
Diode Forward Voltage	V_d	0.98 V
capacitance	C_1, C_2, C_3, C_4	100 µF
Switch on resistance	R_{on}	0.18 Ω
Switch	S_1, S_2	IRF640N

3.4. Voltage Gain Comparison

The effect of non-idealities is translated into power losses increase and reduction of the output voltage that results in higher duty cycle for a determined value of input and output voltage. Figure 7 illustrates the output voltage comparison versus duty cycle while the input voltage is the same. As

it can be seen, the required duty cycle for the proposed PPP converter at a specific output voltage is lower than in other converters.

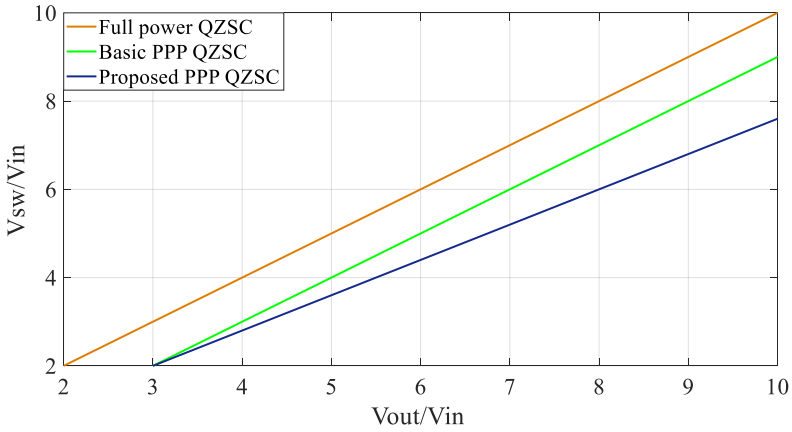


Figure 7. The effect of non-idealities on output voltage waveform versus duty cycle for the three discussed converters.

3.5. Losses Comparison

Figure 8 shows the conducting dissipation power comparison between FP-QZSC, basic PP-QZSC, and the modified PP-QZSC. Both presented PPCs have lower power losses compared to FP-QZSC.

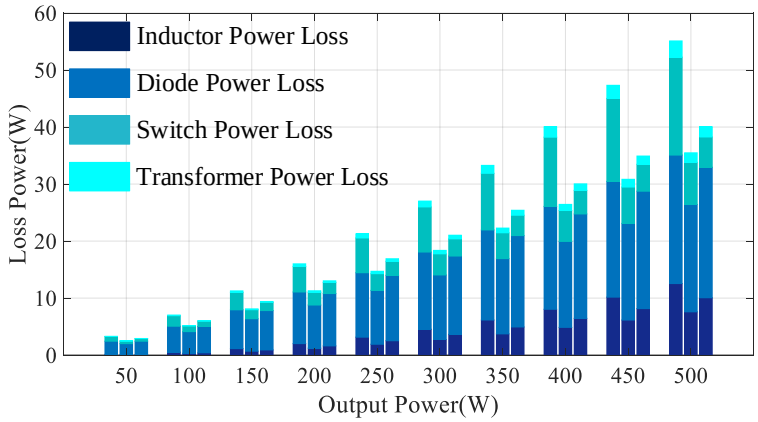


Figure 8. Power Loss Comparison: Left bar) Full power QZSC, Middle bar) Basic PPP QZSC, Right bar) Proposed PPP QZSC.

The efficiency difference between the basic and the proposed PP structures is related to current difference passing through L_1. The power losses difference between the basic PP-QZSC and the modified PP-QZSC, where the basic converter dissipates less power, as this parameter is highly dependent on the value of L_1 and D_1. These two parameters are the structural difference between the presented converters. In the QZSC network of the modified PP-QZSC, L_1 and D_1 currents are equal to I_{in} but in the basic PP-QZSC this value is lower, being I_{in}-I_{out} the overall current that go through the circuit. Other elements performances are almost similar in the basic PP-QZSC and the modified PP-QZSC, because they handle I_{in}-I_{out} which give rise to similar power losses. Therefore, in proposed model these elements process the whole input power which in this case causes higher losses than in the basic converter. In terms of power losses, the switching losses are also considered. Based on parasitic elements, which are mentioned before and referring to Tables 1 and 2, the power losses of the inductors, diodes, switches, and transformer are given by (12), (13), (14), and(15) respectively. These equations are calculated based on switching duty cycle, D_t. In order to compute the losses, RMS values of each current are calculated. With a small approximation, diodes, switches, and transformer current ripples

are considered to be inductor current ripple. The inductors power losses value is based on their RMS current, which is calculated as follows,

$$\begin{cases} P_L = R_{L_1} {I_{L_1,rms}}^2 + R_{L_2} {I_{L_2,rms}}^2 \\ I_{L_1,rms} = I_{L_1,avg} \sqrt{1 + \frac{1}{3}\left(\frac{\Delta i}{2I_{L_1,avg}}\right)} \\ I_{L_2,rms} = I_{L_2,avg} \sqrt{1 + \frac{1}{3}\left(\frac{\Delta i}{2I_{L_2,avg}}\right)} \end{cases} \tag{12}$$

where P_L, $I_{L_1,rms}$, $I_{L_2,rms}$, and Δi are the overall inductor's losses, L_1 and L_2 the average current and current ripple which can be obtained in (14), respectively. Also, diodes and switches power losses are calculated based their current RMS values, so

$$P_D = \left(I_{D_1,avg} + I_{D_2,avg} + I_{D_3,avg}\right) V_d \tag{13}$$

P_D is the sum of diodes conduction loss and is calculated based on the average current. Also, $I_{D_1,rms}$, $I_{D_2,rms}$, and $I_{D_3,rms}$ are:

$$\begin{cases} I_{D_1,avg} = \frac{2n+1-D_s}{1-2D_s} \cdot \frac{V_{out}}{R_{out}} \\ I_{D_2,avg} = I_{D_3,avg} \frac{(1-D_s)(2n+D_s)}{2n(1-2D_s)} \cdot \frac{V_{out}}{R_{out}} \end{cases} \tag{14}$$

$P_{S(cond)}$ are the conduction losses in the switches (S_1 and S_2). $I_{S,rms(Cond)}$ is the RMS value of the current at the switch and is calculated as:

$$\begin{cases} P_{S_1(Cond)} = P_{S_2(Cond)} = \frac{1}{2} P_{S(cond)} \\ P_{S(cond)} = 2R_{on} {I_{S,rms(Cond)}}^2 \end{cases} \tag{15}$$

$P_{S(cond)}$ are the conduction losses of the switches (S_1 and S_2). Likewise, $I_{S,rms}$ is the RMS value of the current at the switch and it can be calculated as:

$$I_{s,rms} = \sqrt{\frac{11 - 2D_t}{24} \Delta i^2 + (2D_t - 1) {I_1}^2 + (1 - D_t) {I_2}^2}, \tag{16}$$

where I_1 and I_2 are the $D_s T_s$ and $(D_t - D_s)T_s$ time intervals average currents, as it can be concluded from Figure 3. The transformer's primary and secondary windings losses are determined according to the switches and diode D_2 and D_3 currents, respectively. According to Figure 4a,b the transformer primary windings conduction is based on switches turn on time interval, $D_t T_s$ and the secondary winding is calculated in $(1 - D_s)T_s$. Therefore;

$$\begin{cases} P_{winding} = P_{wind,pri1} + P_{wind,pri2} + P_{wind,\text{sec}} \\ P_{wind,pri1} = P_{wind,pri2} = R_w {I_{S,rms,(Cond)}}^2 \\ P_{wind,\text{sec}} = R_w {I_{D2,rms}}^2 \end{cases} \tag{17}$$

$P_{winding}$ is the sum of the transformer primary and secondary power losses. The switching power loss ($P_{S(switching)}$) due to non-ideal turn-on and turn-off is illustrated by (18).

$$\begin{cases} P_{S(switching)} = 2(\alpha_{on} + \alpha_{off})(V_{sw} I_{sw}) f_{sw} \\ \alpha_{on} = \alpha_{off} = 0.5(\tau_{rise} + \tau_{fall}) \end{cases} \tag{18}$$

α_{on} and α_{off} are turn on and turn off switching times respectively which can be found in the datasheet. Also V_{sw} and I_{sw} are the average voltage and current stress of the switches, which can be obtained from Table 1. Figure 9 shows the MOSFET switches power loss comparison based on (17) and (18), which the proposed converter has less switch power dissipation.

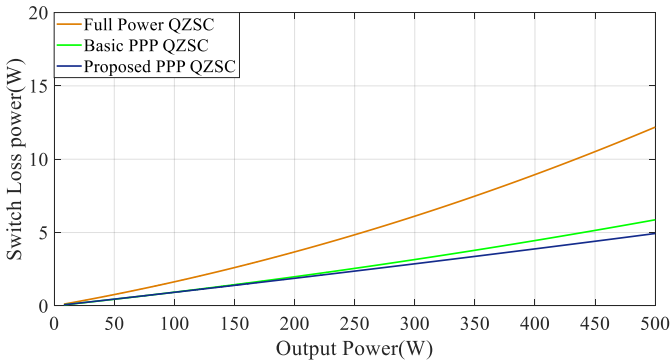


Figure 9. Switch power loss versus output power for the three discussed converters.

3.6. Efficiency Comparison

Integrating PPP technique into any converter does not necessarily mean an improvement in the efficiency [1]. In this case integrating PPP technique improved both basic proposed models compared to full power converter. However, the proposed converter efficiency is lower than basic structure. The structural difference between basic and proposed converters has been mentioned which results in efficiency difference as well. Efficiency of the proposed model highly depends on operating points and transformer turn ratio, which in some cases the modified PP-QZSC efficiency can be improved compared to the basic model. The relationship between these three converters efficiencies which have been listed in Table 3. Since the QZSC efficiency η_{Q1} is always smaller than one, the overall efficiencies of the basic PP-QZSC and the modified PP-QZSC are higher than the FP-QZSC. If the individual converter efficiencies are similar, the relation of converters efficiencies are $\eta_{S3} > \eta_{S2} > \eta_{S1}$ which is shown in Figure 10. Moreover, the full power converter duty cycle is higher than the other two converters. Also, V_{out}/V_{C4} ratio in the modified PP-QZSC is limited to a range between 1.25 and 1.5 because of switching duty cycle which is a range between 50% to 75%. Individual system efficiency of the proposed PPP system, η_{Q3} is dependent on this ratio. If V_{out}/V_{C4} gets larger, η_{Q3} gets lower, therefore η_{S3} is always lower than one. Figure 11 shows the efficiency comparison based on the output power.

Table 3. Efficiency comparison of Full power, basic PPP, and proposed PPP QZSC.

Converter	Individual Converter Output Voltage	Individual Converter Efficiency	System Efficiency
Full power QZSC	V_{out}	η_{Q_1}	$\eta_{S_1} = \eta_{Q_1}$
Basic PPP QZSC	$V_{out} - V_{in}$	η_{Q_1}	$\eta_{S_2} = \frac{V_{out}}{V_{C_4} + \eta_{Q_2} \cdot V_{in}} \cdot \eta_{Q_2}$
Proposed PPP QZSC	$V_{out} - V_{C_1}$	η_{Q_3}	$\eta_{S_3} = \frac{V_{out}}{V_{C_4}} \cdot \eta_{Q_3}$

It should be noticed that, the experimental efficiency curve in 22, shows that maximum efficiency of FP-QZSC can go beyond 97% which is different from our measurement. The efficiency curve of two converters may be compared only if all the conditions are the same. The parameters which affect the converter efficiency are: MOSFET conduction resistance and switching loss, diode forward voltage, winding resistance, and converter operation points. In two prototypes of the converter, these values may differ and therefore different efficiency values can be calculated.

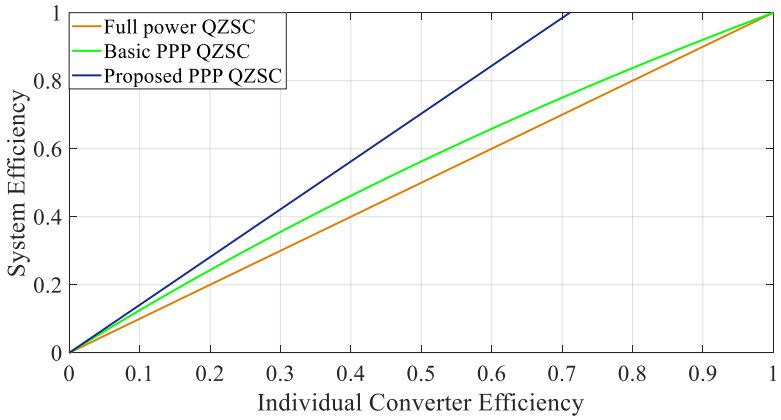


Figure 10. System efficiency versus individual converter efficiency.

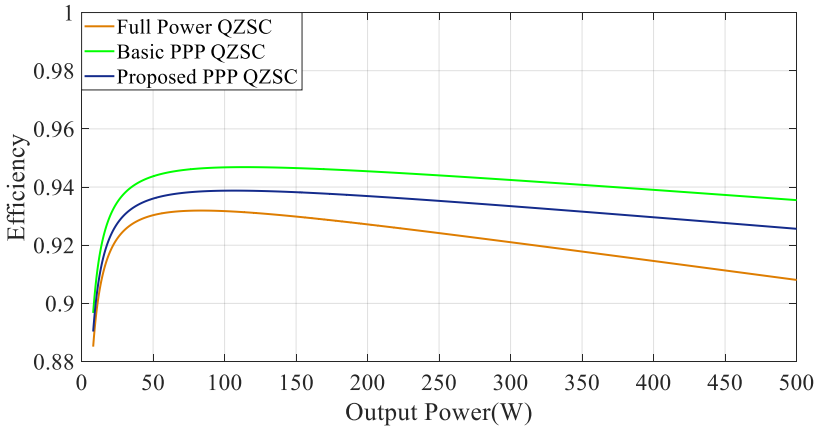


Figure 11. Efficiency versus output power for the three discussed converters.

4. Simulation and Experimental Results and Discussion

The laboratory low power 200 W prototype of the proposed converter, shown in Figure 12, has been built to validate the theoretical analysis and simulation results. The prototype component values are shown in Table 2. In this section the simulation results and experimental results are shown and compared.

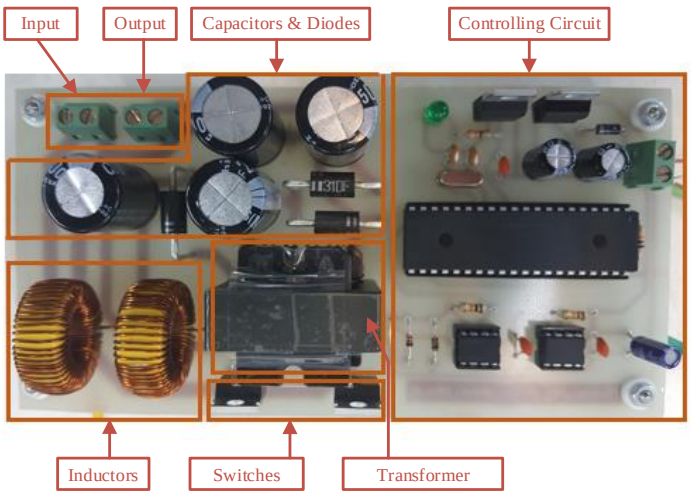


Figure 12. Laboratory prototype of the proposed converter.

The switching gate signals for two switches are shown in Figure 13. In order to generate the desired output voltage, the switching and shoot though duty cycles are adjusted to $D_t = 0.6$ and $D_s = 0.2$ (according to (4)). The switching frequency is 40 kHz. All the experimental tests were conducted under CCM operation of the converter, as DCM does not represent a representative operating point. Comparing simulation and experimental results it can be seen that both match quite well. On the other hand, considering two separate shoot through time intervals (equals to $0.1T_s$) during a switching cycle, the voltage ripple of C_1, and C_2 have a frequency equals to $2fs$ (Figure 14c,d). The frequency voltage ripple of C_3 and C_4 are the same as f_s (Figure 14e,f). The experimental output voltage waveform is also shown in Figure 14a. As mentioned before, the output voltage ripple is the sum of C_1 and C_4 voltage ripples, which can be seen in Figure 14b.

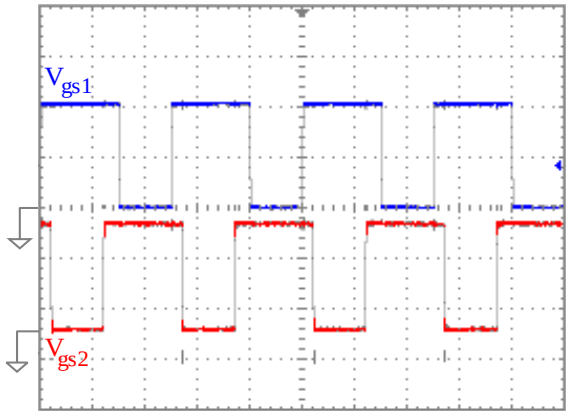
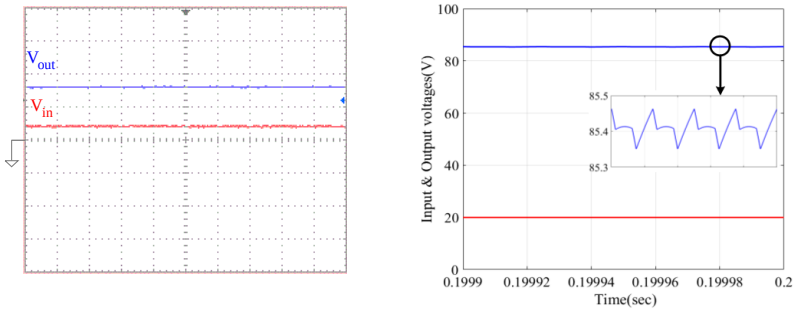


Figure 13. Switch gate signals S_1 and S_2 (Volt/div = 5 V, Time/div = 10 µs). D_t = 0.6 and D_s = 0.2.

The waveforms of I_{L_1} and I_{L_2} are shown in Figure 15. The small current ripples insure the CCM operation of the converter. The only difference between the two current waveforms is that the I_{L_2} is less than inductor I_{L_1} as $I_{L_2} = I_{L_1} - I_{out}$. The experimental and simulation results for transformer primary and secondary voltages are shown in Figure 16. The primary and secondary voltage during shoot through mode is zero which shows the magnetically short circuit of the transformer. In order to compare the performance of the three discussed converters, three converters are made and several tests are done in different operating modes.



(**a**) (**b**)

Figure 14. *Cont.*

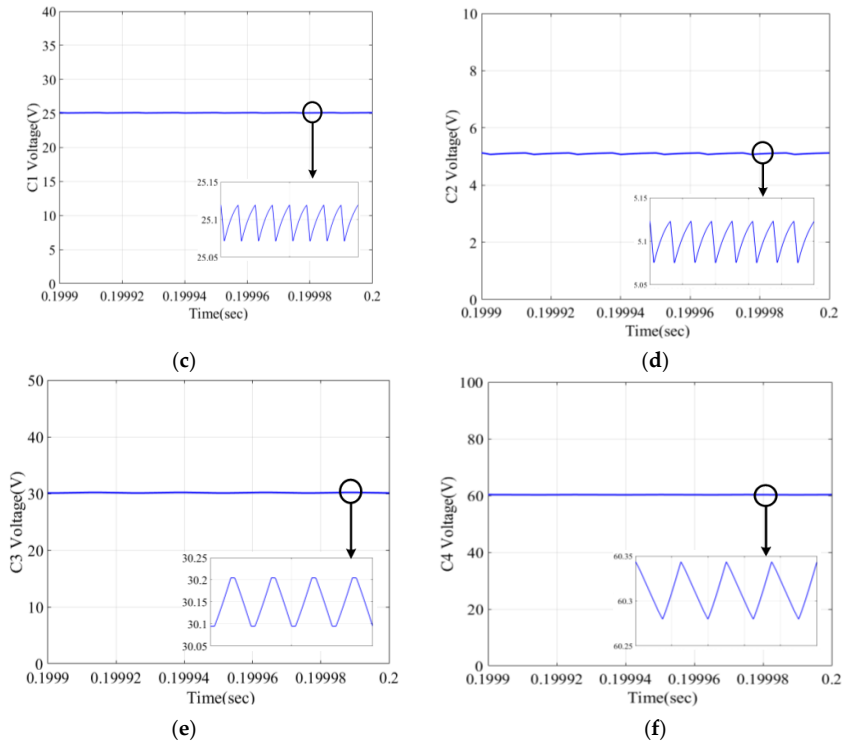


Figure 14. Experimental and simulation result waveforms: (**a**) Input and output voltage (Volt/div = 50 V, Time/div = 10 µs), (**b**) Input and output voltage (**c**) Capacitor C_1 voltage, (**d**) Capacitor C_2 voltage, (**e**) Capacitor C_3 voltage and (**f**) Capacitor C_4 voltage.

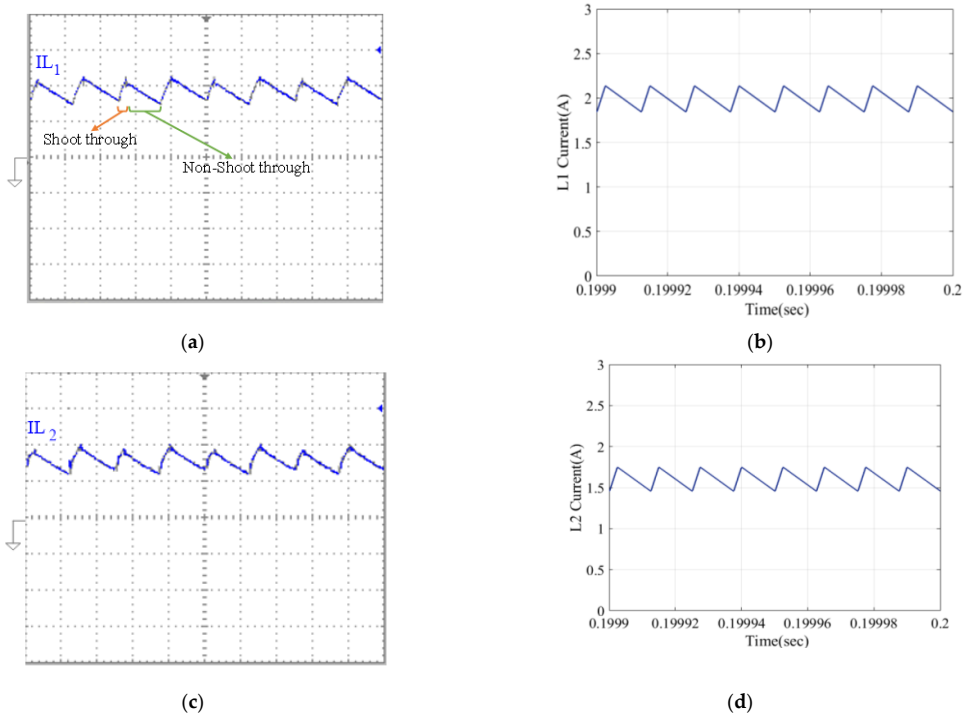


Figure 15. Simulation and experimental results for inductor currents: (**a**) experimental results for I_{L_1} (Amp/div = 1 A, Time/div = 10 µs), (**b**) simulation results for I_{L_1}, (**c**) experimental results for I_{L_2} (Amp/div = 1 A, Time/div = 10 µs) and (**d**) simulation results for I_{L_2}.

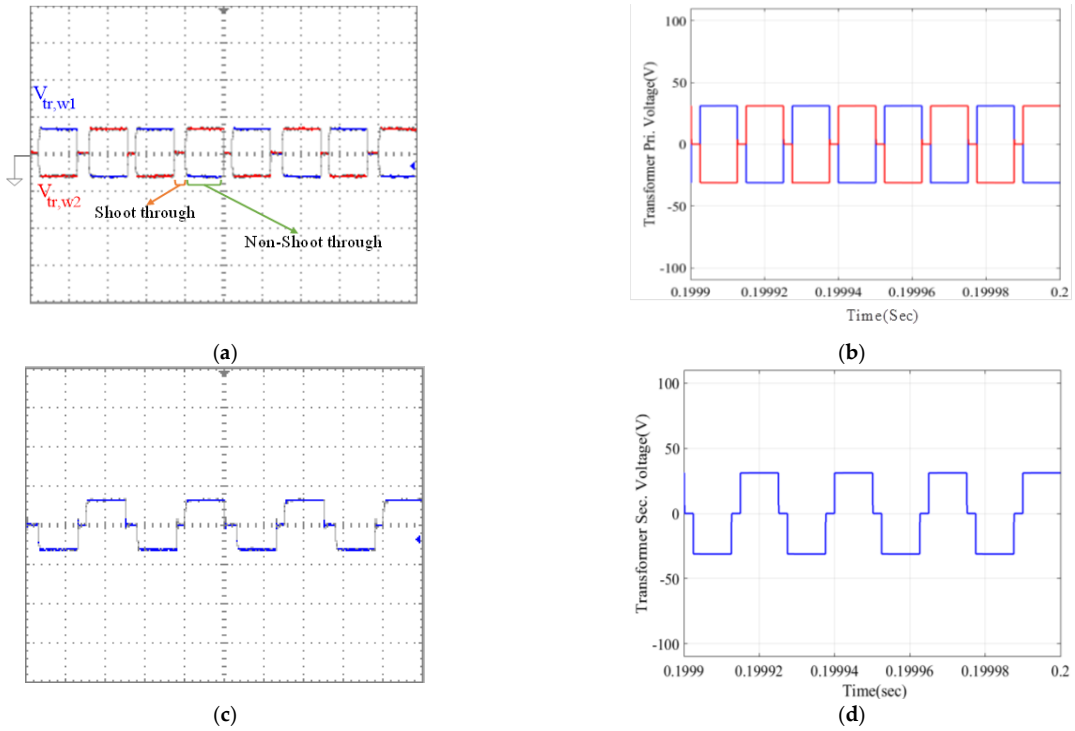


Figure 16. Simulation and experimental results for inductor currents: (**a**) experimental results for I_{L_1} (Amp/div = 1 A, Time/div = 10 µs), (**b**) simulation results for I_{L_1}, (**c**) experimental results for I_{L_2} (Amp/div = 1 A, Time/div = 10 µs) and (**d**) simulation results for I_{L_2}.

In Figure 17, the efficiency of the converters for different input voltages with constant switching duty cycle of 0.6 are sketched also compared with simulation resulted efficiency. The result shows higher efficiency of the basic PP-QZSC as predicted in Section 3. As discussed before, the semiconductor loss is lower which result in a smaller cooling system and improves the reliability of the system.

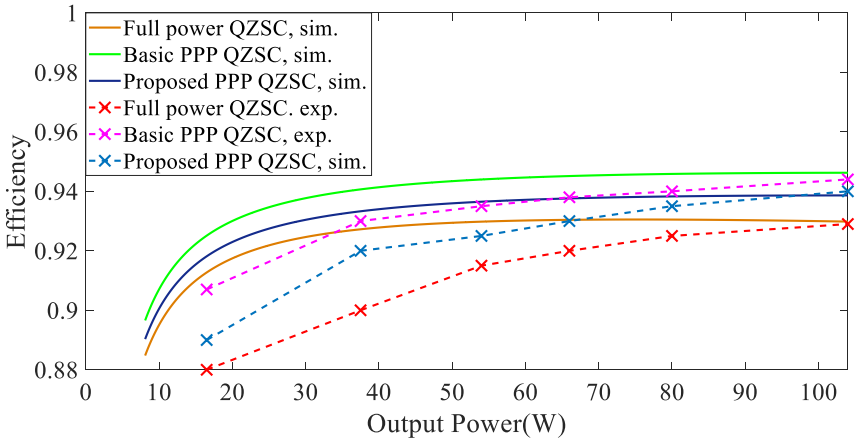


Figure 17. Experimental result for efficiency comparison of the three discussed converters.

5. Conclusions

This paper presents a modified QZSC using PPP technique. Compared to full power converter, partial power converter shows higher efficiency and lower voltage and current stress. Although the modified PP-QZSC had a rather lower efficiency by 1%, but the voltage stress of the switches decrease by 25%. High boost capability, lower voltage and current stress, improved efficiency and lower cost considering small duty cycle, and small turn ratio of the transformer are the proposed and

basic PPP converters features. Higher boosting mode and reduced voltage stress are the proposed PPP QZSC advantages compared to basic PPP structure. The operating performance of the proposed converter was simulated and experimentally tested to validate the theoretical analysis. Due to lower power handled by the PPP converters, which is a remarkable feature, and considering the results and performance obtained, the proposed converter is promising to be used in PV systems, as a partial power inverter would give rise to a lower cost and size of the power processing stage.

Author Contributions: All persons who meet authorship criteria are listed as authors, and all authors certify that they have participated sufficiently in the work to take public responsibility for the content, including participation in the concept, design, analysis, writing, or revision of the manuscript. Furthermore, each author certifies that this material or similar material has not been and will not be submitted to or published in any other publication before its appearance in the Applied Sciences, MDPI. All in all, the contribution of all authors is almost equal.

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