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Modelling of Dynamic Properties of Silicon Carbide Junction Field-Effect Transistors (JFETs)

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Abstract: The paper deals with the problem of modelling and analyzing the dynamic properties of a Junction Field Effect Transistor (JFET) made of silicon carbide. An examination of the usefulness of the built-in JFET Simulation Program with Integrated Circuit Emphasis (SPICE) model was performed. A modified model of silicon carbide JFET was proposed to increase modelling accuracy. An evaluation of the accuracy of the modified model was performed by comparison of the measured and calculated capacitance–voltage characteristics as well as the switching characteristics of JFETs.

Keywords: C–V characteristics; JFET; modelling; silicon carbide

1. Introduction

Nowadays, the dynamic development of high-power electronic systems requires modern electronic components and devices that are characterized by improved electrical and thermal properties [1–4]. A new generation of junction field-effect transistors made of silicon carbide (SiC-JFETs) has appeared on the market as a result of technological progress in the construction of semiconductor devices [1,3,5]. SiC-JFETs are characterized by better static properties, i.e., higher values of absolute maximum ratings of operating currents, terminal voltages and dissipated power as well as dynamic properties related to short switching times [5–7].

The dynamic properties of a JFET depend on, among others, the values of diffusion and junction capacitances of the internal gate-source and gate-drain p–n junctions of the transistor [8–10]. Both capacitances are functions of the terminal voltage applied and play an important role in the forward and the reverse polarization of the device. On the other hand, the dynamic properties of JFETs are characterized by parasitic capacitances resulting from the non-zero size of the transistor structure [8–11].

In the design and analysis of power electronic devices and circuits, an appropriate computer tool containing reliable models of semiconductor devices is needed. One of the most popular computer programs used for the modeling and analysis of electronic devices and circuits is the Simulation Program with Integrated Circuit Emphasis (SPICE) [12]. SPICE contains a large number of passive and active device models. The accuracy of SPICE models for various semiconductor devices, such as MOSFET, BJT, SJT and IGBT transistors, has already been studied [13–18].

In the case of JFET characteristics modelling, a Shichman–Hodges (S–H) model is used [12]. Recently, a successful attempt at modeling the static characteristics and parameters of SiC-JFETs using the S–H model have been reported [19,20]. On the other hand, selected aspects of modelling dynamic characteristics of JFETs were presented in [8–10,21–24].

The paper deals with the problem of modelling capacitance–voltage (C–V) as well as switching characteristics of SiC-JFETs. Appropriate modifications of the Shichman–Hodges model were proposed in order to improving its accuracy. The modified model was experimentally verified by comparison of

the measured and calculated C–V characteristics of the transistor. Moreover, the results of measurements and calculations of the switching characteristics of the transistor were compared.

2. The Shichman–Hodges Model Form

A network form of the built-in in SPICE Shichman–Hodges model of JFET is presented in Figure 1 [12].

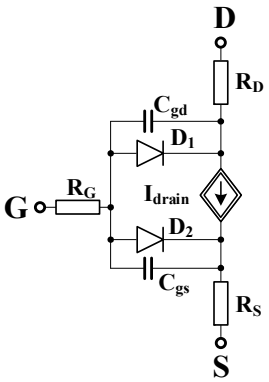


Figure 1. Network form of the Shichman–Hodges (S–H) model of the junction field-effect transistor (JFET) in Simulation Program with Integrated Circuit Emphasis (SPICE).

The main element of the presented model is the controlled source I_{drain} modeling static drain current of the transistor for three operational regions, according to the equations [12,19]:

- in the cut-off region (for $V_{GS}-V_{TO}(T) < 0$):

$$I_{drain} = 0 \tag{1}$$

- in the linear region (for $V_{DS} \leq V_{GS}-V_{TO}(T)$):

$$I_{drain} = BETA(T) \cdot (1 + LAMBDA \cdot V_{DS}) \cdot V_{DS} \cdot (2 \cdot (V_{GS} - V_{TO}(T)) - V_{DS}) \tag{2}$$

- in the saturation region (for $0 < V_{GS}-V_{TO}(T) < V_{DS}$):

$$I_{drain} = BETA(T) \cdot (1 + LAMBDA \cdot V_{DS}) \cdot (V_{GS} - V_{TO}(T))^2 \tag{3}$$

where: V_{GS}—gate-source voltage, V_{DS}—drain-source voltage, LAMBDA—channel-length modulation coefficient, BETA(T)—temperature dependence of transconductance coefficient, $V_{TO}(T)$—temperature dependence of the threshold voltage.

Resistors R_G, R_D and R_S (Figure 1) represent series resistances of the gate, the drain and the source of the transistor. Diodes D_1 and D_2 describe currents of the gate–source and the gate–drain p–n junctions, respectively. An extended description of the static S–H model is given for instance in [20] or is available in the SPICE user manual [12].

Capacitors C_{gs} and C_{gd} (Figure 1) represent nonlinear junction capacitances of p–n junctions, according to equations [3,8]:

- for $V_{gs} \leq FC \cdot PB$

$$C_{gs} = CGS \cdot \left(1 - \frac{V_{gs}}{PB}\right)^{-M} \tag{4}$$

- for $V_{gs} > FC \cdot PB$

$$C_{gs} = CGS \cdot (1 - FC)^{-(1+M)} \cdot \left(1 - FC \cdot (1 + M) + M \cdot \frac{V_{gs}}{PB}\right) \quad (5)$$

- for $V_{gd} \leq FC \cdot PB$

$$C_{gd} = CGD \cdot \left(1 - \frac{V_{gd}}{PB}\right)^{-M} \quad (6)$$

- for $V_{gd} > FC \cdot PB$

$$C_{gd} = CGS \cdot (1 - FC)^{-(1+M)} \cdot \left(1 - FC \cdot (1 + M) + M \cdot \frac{V_{gd}}{PB}\right) \quad (7)$$

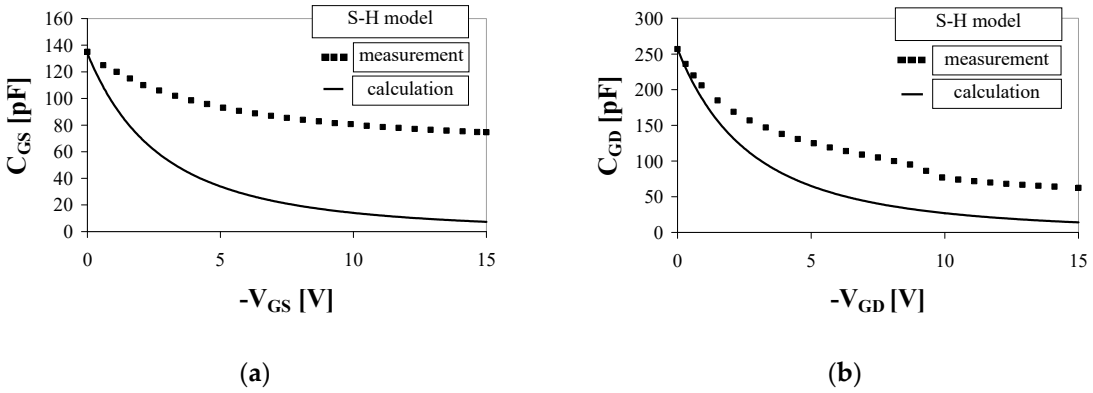
where: FC—forward-bias depletion capacitance coefficient, PB—gate p–n potential, CGS, CGD—zero-bias gate–source and gate–drain junction capacitances, M—gate p–n grading coefficient.

3. Results of Simulations of the Shichman–Hodges Model

A normally-OFF trench silicon carbide power Junction Field-Effect Transistor of absolute maximum drain-source voltage equal to 1700 V (SJEP170R550) fabricated by SemiSouth [25] was chosen for investigations. Measurements of capacitance characteristics were performed using the measuring source Keithley 2602. The JFET model parameters were calculated using an estimation method described in [26]. Values of static model parameters for the considered transistor are: BETA = 2.308 A/V^2, LAMBDA = 0.0538 V^{-1}, IS = $1 \cdot 10^{-16}$ A, ISR = $4.51 \cdot 10^{-9}$ A, M = 0.0164, N = 3.152, NR = 9.62, PB = 6.832 V, R_D = 0.4113 Ω, R_S = 0.0346 Ω, V_{TO} = 0.8576 V, XTI = 2, BETATCE =−0.0994 %/°C, $V_{TOTC} = 6.1494 \cdot 10^{-4}$ V/°C.

In addition, values of parameters describing the capacitance of the considered transistor model are as follows: CGD = $2.57 \cdot 10^{-10}$ F, CGS = $1.34 \cdot 10^{-10}$ F, FC = 0.5.

Results of measurements and calculations of C–V characteristics using S–H model are presented in Figure 2. Points and solid lines in Figure 2 denote the results of measurements and calculations, respectively.



(**a**) (**b**)

Figure 2. (**a**,**b**) Measured and calculated (S–H model) capacitance–voltage characteristics of the SiC JFET.

As seen, for small V_{GS} and V_{GD} bias voltages of around 1 V a good agreement between the simulation and measurement results can be observed. However, quantitative and qualitative discrepancies reaching even one order of magnitude are observed in the case of $C_{GS}(V)$ and $C_{GD}(V)$ characteristics (Figure 2a,b) for voltages greater than 1 V.

The manufacturers of the JFET transistors present in datasheets [25] the characteristics of capacitances C_{iss}, C_{oss} and C_{rss} as a function of specified terminal voltages. These capacitances constitute an appropriate combination of transistor junction capacitances. Capacitances C_{iss}, C_{oss} and C_{rss} are expressed with the following formulas [10]:

$$C_{iss} = C_{gs} + C_{gd} \tag{8}$$

$$C_{oss} = C_{ds} + C_{gd} \tag{9}$$

$$C_{rss} = C_{gd} \tag{10}$$

where C_{gs}—gate–source capacitance, C_{gd}—gate–drain capacitance, and C_{ds}—drain–source capacitance.

Calculations of C–V characteristics of the transistor can be realized using specialized SPICE simulation circuits [10]. The network forms of C_{iss} and C_{rss} measurement fixtures are presented in Figures 3 and 4, respectively.

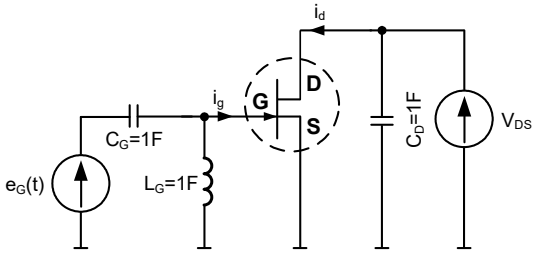


Figure 3. C_{iss} measurement fixture.

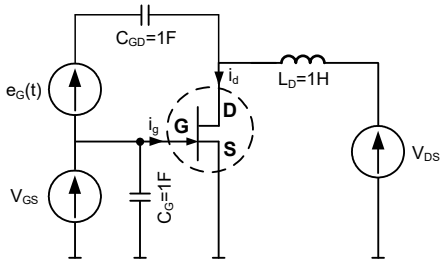


Figure 4. C_{rss} measurement fixture.

Capacitances C_G, C_D, C_{GD} and inductances L_G, L_D from Figures 3 and 4 with non-physical large values are used to separate appropriate currents and voltages in the fixtures. Voltage sources V_{GS} and V_{DS} determine the operating point of the transistor. The voltage source $e_G(t)$ generates a sinusoidal signal with an amplitude U_M = 10 mV and a frequency f = 1 MHz. Capacitance values at a defined operating point are determined by performing a transient analysis and are calculated according to equations [10]:

$$C_{iss} = \frac{i_g}{V_{gs} \cdot 2 \cdot \pi \cdot f} \tag{11}$$

$$C_{oss} = \frac{i_d}{V_{ds} \cdot 2 \cdot \pi \cdot f} \tag{12}$$

$$C_{rss} = \frac{i_g}{V_{gd} \cdot 2 \cdot \pi \cdot f} \tag{13}$$

where: i_g, i_d, V_{gs}, V_{gd}, V_{ds}—amplitude of alternating currents and voltages marked in Figures 3 and 4.

Calculated and measured characteristics C_{iss} and C_{rss} versus drain–source voltage are presented in Figure 5. Points and solid lines in Figure 5 denote the results of measurements and calculations, respectively.

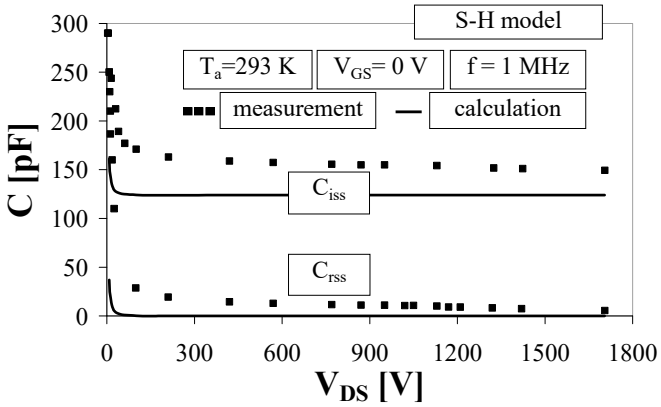


Figure 5. Measured and calculated (S–H model) $C_{iss}(V_{DS})$ and $C_{rss}(V_{DS})$ characteristics of the JFET.

As seen from Figure 5, there are discrepancies between the measurements and the calculations. For example, the calculated values of capacitance C_{iss} for the drain–source voltage up to 500 V are smaller than the values obtained from measurement by about 40%. In the range of relatively small values of drain-source voltage V_{DS}, capacitance values decrease rapidly with the increase of the voltage V_{DS}. However, in the range of drain-source voltage above 100 V capacitance changes are barely noticeable.

Qualitative discrepancies between the measurements and S–H model simulations observed in Figures 2 and 5 are a sufficient reason to introduce appropriate model modifications.

4. Modifications of the Shichman–Hodges Model

The original Shichman–Hodges model assumes [12] that the gate–source and the gate–drain junctions appearing in the transistor structure are identical in terms of physical properties and electrical parameters. Therefore, the model parameters such as M, PB and FC are used to describe properties of the junctions in common (see Equations (4)–(7)). This means that an attempt to determine the values of these parameters in order to achieve a good agreement between simulation and measurement results of the gate–drain junction automatically changes the shape of calculated gate-source junction characteristics.

On the other hand, the structure of a real JFET contains p–n junctions of different electrical properties [21], so a separate set of M, PB and FC parameters has to be used. In the proposed model, independent descriptions of each junction were introduced to increase the modelling accuracy, according to equations:

- for $V_{GS} \leq FC1 \cdot PBCGS$

$$C_{GS} = CGS \cdot \left(1 - \frac{V_{GS}}{PBCGS}\right)^{-MGS} \tag{14}$$

- for $V_{GS} > FC1 \cdot PBCGS$

$$C_{GS} = CGS \cdot (1 - FC1)^{-(1+MGS)} \cdot \left(1 - FC1 \cdot (1 + MGS) + MGS \cdot \frac{V_{GS}}{PBCGS}\right) \tag{15}$$

- for $V_{GD} \leq FC2 \cdot PBCGD$

$$C_{GD} = CGS \cdot \left(1 - \frac{V_{GD}}{PBCGD}\right)^{-MGD} \tag{16}$$

- for $Vgd > FC2 \cdot PBCGD$

$$C_{GD} = CGS \cdot (1 - FC2)^{-(1+MGD)} \cdot \left(1 - FC2 \cdot (1 + MGD) + MGD \cdot \frac{V_{GD}}{PBCGD}\right) \tag{17}$$

where: FC1, PBCGS, MGS, FC2, PBCGD, MGD represent a new set of model parameters.

The modified model was implemented to SPICE as a subcircuit with the use of the ABM (Analog Behavioral Modeling) option (using controlled sources). The network form of the proposed model is presented in Figure 6. Controlled-current sources G_{CGD} and G_{CGS} represent currents flowing through C_{GD} and C_{GS} capacitances. An additional parameter estimation procedure was carried out. New values of the model parameters describing the gate–source and the gate–drain junction are as follows: FC1 = 0.975, PBCGS = 2.764 V, MGS = 0.305, FC2 = 0.826, PBCGD = 2.654 V, MGD = 0.679.

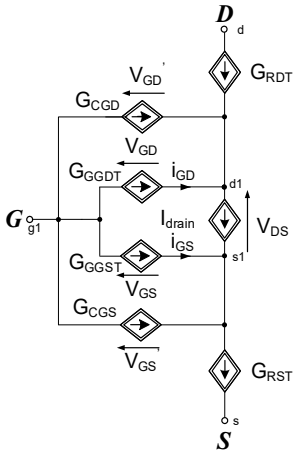


Figure 6. Network form of the modified model of the JFET.

The results of the experimental verification of the modified model are presented in Figures 7 and 8. Points and solid lines in Figures 7 and 8 denote the results of measurements and calculations, respectively.

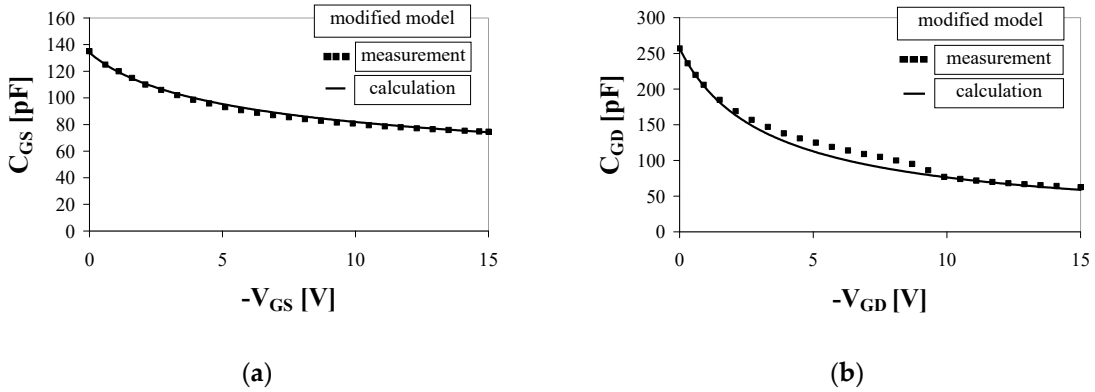


Figure 7. (**a**,**b**) Measured and calculated (modified model) C–V characteristics of the JFET.

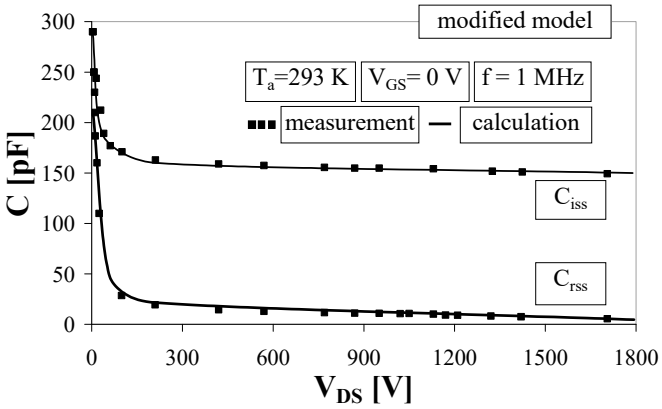


Figure 8. Measured and calculated (modified model) $C_{iss}(V_{DS})$ and $C_{rss}(V_{DS})$ characteristics of the JFET.

As seen, the results of modeling using the modified model provide much greater modelling accuracy than the original S–H model.

5. Simulation Results of Dynamic Characteristics of JFET

Measurements and calculations of the dynamic characteristics of the transistor were carried out in order to check the suitability of the modified JFET model. For this purpose, the simplest measurement system was chosen—a switching circuit presented in Figure 9.

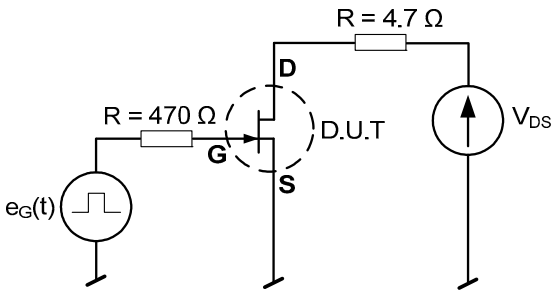


Figure 9. Switching circuit of the transistor.

In the switching circuit, the source V_{DS} is responsible for determining the operating point of the transistor, whereas the source $e_G(t)$ with an amplitude equal to 2.5 V and frequency of 10 kHz forces stimulation on the transistor gate.

Measurement and calculation results of $V_{GS}(t)$ and $V_{DS}(t)$ waveforms of the JFET are presented in Figure 10. Points and solid lines in Figure 10 denote the results of measurements and calculations, respectively.

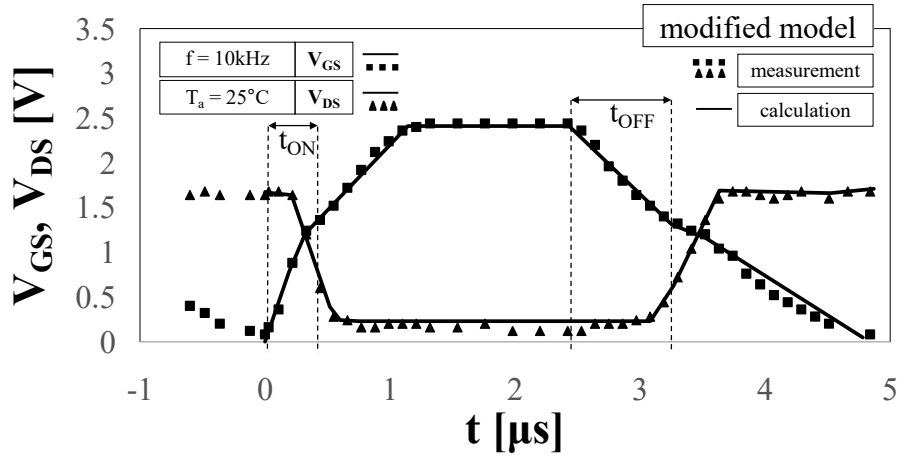


Figure 10. Calculated and measured time waveforms of the gate–source and drain–source voltage of the JFET in the switching circuit.

A good agreement between the results of measurements and calculations of waveforms $V_{GS}(t)$ and $V_{DS}(t)$ is observed, which confirms the correctness of the modified model. The turn-on (t_{ON}) and turn-off (t_{OFF}) delay times of the transistor are equal to about 0.3 and 0.8 µs, respectively.

6. Conclusions

In this paper, the usefulness of the Shichman–Hodges model of the JFET built-in in SPICE is examined. The SJEP170R550 transistor offered by SemiSouth Inc. is considered in detail. Owing to the observed discrepancies between the device's simulated and measured characteristics some modifications of the model to improve its accuracy are proposed. The modifications concern a change

in the description of the capacitances of the transistor's p–n junctions. A significant increase in the modeling accuracy of SiC JFET characteristics is observed, which confirms the validity of the modified model. The proposed model can be used for modelling other types of JFETs made of silicon carbide, where performing an estimation procedure of transistor model parameters is only required.

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