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# Voltage-Balancing Strategy for Three-Level Neutral-Point-Clamped Cascade Converter under Sequence Smooth Modulation

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**Abstract:** Three-level neutral-point clamped cascaded converters (3LNPC-CC) are widely used in high power nigh-voltage applications. This paper mainly discusses the open-circuit fault in DC-side of the 3LNPC-CC. Optimized by the sequence pulse modulation, a sequence smooth modulation (SSM) is proposed to keep the DC-side voltage balance while the 3LNPC-CC suffers open-circuit fault from DC-side. The SSM found efficient switch-state path through a 3-D cube model and simplified the path from thousands of switch state. The SSM avoids the complex calculation in the voltage-balancing modulation, while the dynamic character of it was less influenced. At the same time, the modulation changes the voltage level smoothly and balances the fault DC-side voltage effectively. The characters of the proposed modulation are verified by the simulation and the experiment.

**Keywords:** 3LNPC-CC; voltage-balancing; sequence smooth modulation open-circuit fault

## 1. Introduction

The traction power supply system is one of the four core systems of a railway and the only source of train power [1]. In addition, the traction power supply system is also an important load of the three-phase power system [2,3]. Because the transformer production technology is mature and simple relatively, the railway mainly power supply is three-phase to single-phase. In the traction power supply system, the power realized the conversion of three-phase 110 kV to single-phase 27.5 kV. However, with the development of industrialization and the full use of renewable energy, many disadvantages of this power supply mode have gradually emerged. Therefore, the traction power supply method based on the application of multilevel converters was widely researched and applied [4,5].

An inverter is the core piece of equipment in the multilevel converter [2]. In this topology, photovoltaic and wind-generator energy is connected to the system through the inverter to provide energy for traction power supply and railway load. The cascaded multilevel inverter is a typical inverter, which was proposed in 1981 [6]. The advantages of the multilevel inverter include:

(1) High-voltage and high-power output can be realized by low-voltage power-switching devices;
(2) The switching frequency of a single power-switching device is low;
(3) Low loss of power-switching devices;
(4) The filter device is physically small in size.

H-bridge topology, the neutral-point clamped (NPC) topology and modular multilevel converters (MMC) topology are the most widely used structures in multilevel converters. The H-bridge topology is simple in structure, but weak in voltage-bearing capacity, while the MMC topology is strong in

voltage-bearing capacity, but complex in structure. In this way, the H-bridge topology and the MMC topologies are not applicable to the railway power supply system due to their limitations. The NPC cascaded converter has been widely used due to its simple structure relatively and high voltage-bearing capacity [7]. The NPC topology consists of several IGBT and clamp diodes. However, with the increase of the number of output levels, the topology of the converter is relatively complex, and a large number of sensors is needed to control the converter. Once charging and discharging time of the supporting capacitor is inconsistent, the voltage of the series capacitor will be unbalanced [8]. In addition, when the DC-side capacitance or internal switching devices of the cascaded multilevel inverter develop an open-circuit fault, the control performance of the system will be lost and even seriously affect the operation of the system. Therefore, the study in DC-side open-circuit fault of the cascaded inverter has become an urgent problem in academic and industry [9].

For the direct current-side (DC-side) open-circuit fault of the system, the direct measurement method of voltage sensor is adopted. However, the measurement method of the voltage sensor is limited by the DC-side support capacitance, which reduces the open-circuit-fault diagnosis accuracy and greatly increases the open-circuit-fault diagnosis time. In [10], the control strategy used the proportional-integral controller (PI) controller is adjusted. In this paper, the equivalent duty cycle is adjusted by PI controller and the power flow of each module is changed to realize the DC-side voltage balanced. However, the DC-side voltage balanced stability with the PI controller has a contradiction between the mean voltage velocity and stability. In addition, the regulation speed of the DC-side voltage is slow.

In contrast, a modulation voltage-balancing strategy could change the turn-on and turn-off sequence of the switches directly, so the fault tolerance effect is stronger—and the speed is faster. In [11], the redundant vector-selection modulation strategy is used to realize the stability control after DC-side voltage unbalanced of each module in cascaded H-bridge converter (CHBC). The DC-side voltage control is integrated into the modulation strategy in this strategy, which can achieve a more rapid, wide range of fault tolerance effects. The strategy proposed in [12] indicates that the opposite vectors could be a fantastic way to ensure the stability of the DC-side voltage, which has been demonstrated by a large number of simulations and experiments in this paper. This method can greatly widen the stable range of the fault tolerance strategy. However, there is no intermediate transition vector when the opposite vector is inserted, it will lead to the sudden change of port voltage level, which will lead to the increase of switching frequency, switching loss. In order to solve the above problems, a smooth voltage-balancing strategy is proposed in [13]. By sacrificing parts of the dynamic response capabilities, this strategy selects the redundancy and smooth voltage vector to control the DC-side voltage after open-circuit fault, which eliminates the mutation of port voltage level. In [14], a sequence pulse modulation (SPM) is proposed, which has strong fault tolerance capability and smooth change of voltage level. However, it is complicated to calculate the switching state. Generally speaking, the [12–14] could balance the DC-link voltage under modulation index among 0.8. However, [12] balances the voltage with the price of switch state jump, [14] works with drastic fluctuation, the calculation of [13] was too complex to become engineered. A fault reconfiguration strategy with strong control ability and good performance need to be studied [15–17]. Additionally, the voltage-balancing capability is difficult to realize the quantification [18,19]. In [20,21], the range of voltage-balancing capability is described by energy flow between DC-side and AC-side. Among these strategies, the DC-link voltage could remain balance while the modulation index is at least below 0.8. However, a qualitative description is not suitable for different voltage level systems and has some inevitable errors [22–25]. Thus, a precise voltage-balancing capability mathematical model is of great importance to establish for different 3LNPC-CC systems.

In this paper, an SSM strategy is proposed for the 3LNPC-CC system. The rest of this paper is organized as follows: Section 2 presents the 3LNPC-CC and its control system. Then, the proposed strategy is discussed in detail in Section 3. Section 4 verifies the theoretical analysis by simulation and experimental results, respectively.

## 2. The Configuration and Control Strategy of 3LNPC-CC

### *2.1. The Configuration of the Multimodule 3LNPC-CC*

The basic structure of 3LNPC-CC applied in the hybrid AC–DC–AC smart grid is shown in Figure 1. The nigh-voltage input is connected with the distributed network. The module voltage input is a bidirectional port connecting with the battery group, super capacitor or flywheel energy-storage system. The low-voltage output provides three-phase 380-V AC-voltage for industry applications, urban lighting and residential electrical equipment. Additionally, the 3LNPC-CC plays an important role in the realization of high and low-voltage power conversion. The transformer is mainly used for electrical isolation while the filter is applied to improve power quality. The output of this system is used for the daily life.

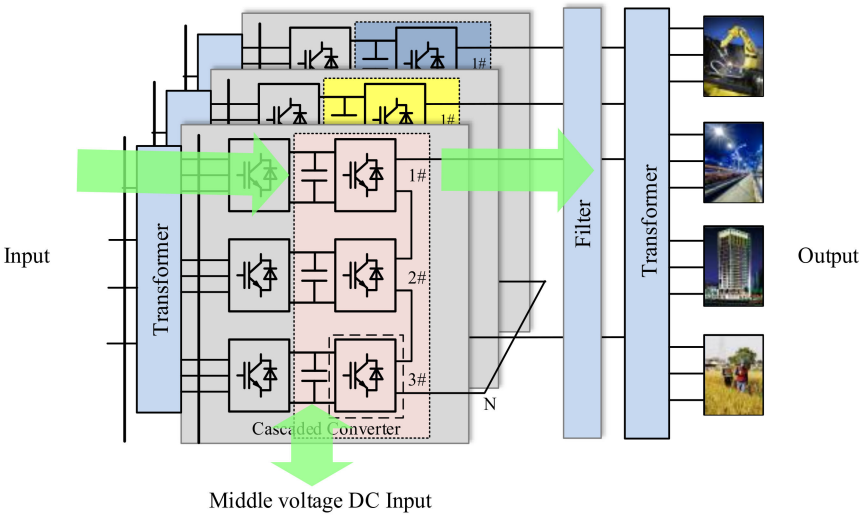



**Figure 1.** Basic structure of the hybrid AC–DC–AC smart grid.

As is shown in Figure 2, the topology of 3LNPC-CC is composed of a DC side, several NPC modules and an AC side. In each NPC module, there are one isolated switch, two series capacitors, eight IGBTs and four diodes. Each module is cascaded to establish one phase's voltage; the other two phases have similar topologies. Thus, the input of 3LNPC-CC is composed of 3n DC ports, while the output of 3LNPC-CC is three-phase AC port and one neutral point.

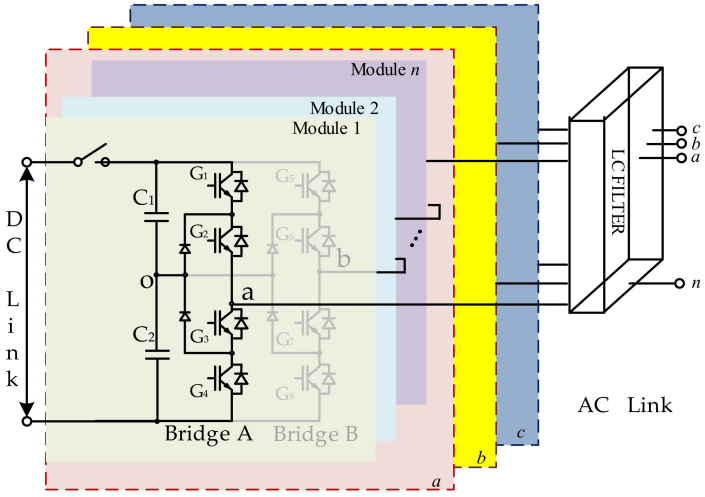



**Figure 2.** Topology of 3LNPC-CC.

### 2.2. The Control Strategy of the Multimodule 3LNPC-CC

In multimodule 3LNPC-CC, a voltage–current closed loop control is applied to regulate the output voltage and current, respectively. The control strategy aims to provide the AC voltage according to the reference value and improve the power quality. The control strategy is mainly composed of a voltage loop and a current loop based on the PI controller. The voltage and current are decoupled with the active component $d$ and passive component $q$. Once the output AC voltage develops fluctuation, the control variable $v_d$ and $v_q$ will be regulated under the $d$–$q$ axis to maintain the output voltage. Moreover, once the output AC current contains a reactive component, the control variable $i_d$ and $i_q$ will be regulated to maintain the unit power factor. Thus, the mathematical model of the double closed loop control strategy can be defined as Formulas (1) and (2).

$$\begin{cases} u_d^* = k_{ip}(i_d^* - i_d) + k_{ii}\int(i_d^* - i_d)dt + \omega L i_q \\ u_q^* = k_{ip}(i_q^* - i_q) + k_{ii}\int(i_q^* - i_q)dt + \omega L i_d \end{cases} \tag{1}$$

$$\begin{cases} i_d^* = i_{Ld} + k_{vp}(v_d^* - v_d) + k_{vi}\int(v_d^* - v_d)dt + \omega C v_{Lq} \\ i_q^* = i_{Lq} + k_{vp}(v_q^* - v_q) + k_{vi}\int(v_q^* - v_q)dt + \omega C v_{Ld} \end{cases} \tag{2}$$

where $u_d$, $u_q$, $i_d$, $i_q$ are control variables under the $d$–$q$ axis while the $u^*_d$, $u^*_q$, $i^*_d$, $i^*_q$ are reference values under the $d$–$q$ axis. The PI controller has two pairs parameters which are $k_{vp}$, $k_{vi}$, $k_{ip}$ and $k_{ii}$. Moreover, the $L$ is the filter value of the inductor, the $C$ is the filter value of capacitor and $\omega$ is the frequency of 3LNPC-CC. According to the mathematical model, the control scheme of 3LNPC-CC can be illustrated in Figure 3. $v_{an}$, $v_{bn}$ and $v_{cn}$ are the three phase voltage. 1 is the normalized reference value of $v_d$. 0 is the normalized zero value of $v_q$. $i_{La}$, $i_{Lb}$ and $i_{Lc}$ are the three phase current. $\omega$ is the angle of the three phase current, which is locked by PLL (phase-locked loop). The voltage signal sampled from voltage sensor is the input of the voltage loop, which can produce the reference of $d$–$q$ current. Similarly, the current signal from current sensor is transformed to current loop to produce the reference of $d$–$q$ voltage. Thus, the $d$–$q$ voltage can be decoupled with the three-phase voltage signal as the output signal of the control strategy. In Figure 3, the modulation strategy and the proposed voltage-balancing strategy are illustrated, which are thoroughly introduced in Sections 3 and 4. The final control results in Figure 3 will be transferred as IGBT signal ($G_1$,$G_2$,$G_3$ … $G_n$), for controlling the gate of IGBT in Figure 2.

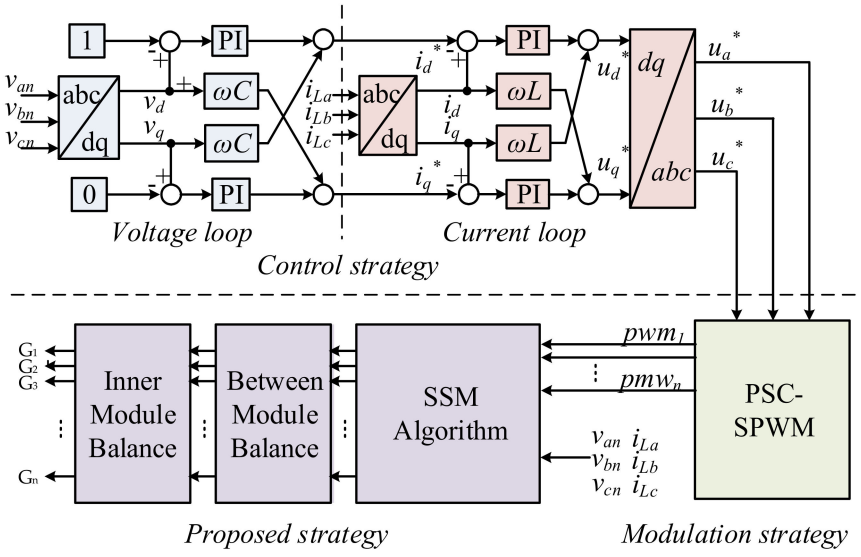



**Figure 3.** Control scheme of 3LNPC-CC.

## 3. The Proposed Strategy of 3LNPC-CC

### *3.1. The Proposed Strategy*

A three-module 3LNPC-CC is used to illustrate the theory of voltage balancing. In the DC voltage $V_{dc1}$, $V_{dc2}$ and $V_{dc3}$ of Module 1, Module 2 and Module 3 are sampled, respectively. While one module suffers from the open-circuit fault of DC-side, the DC-side voltage of the module will drop drastically. In fact, the function of voltage-balancing strategy is to stop the DC-side voltage dropping and bring DC-side voltage to normal. When the output current is positive, the open-circuit fault module should try it best to synthesize −2, −1 and 0 voltage level, so that the voltage level could balance the DC-side voltage by charging the DC-side capacitor. Similarly, When the output current is negative, the fault module should try its best to synthesize 2, 1 and 0 voltage levels.

To achieve the voltage-balancing strategy, [13] proposed an SPM as shown in Table 1—in which all modules synthesize the voltage level based on table according to the voltage level. The relationship DC-side voltage of Module $S_1$, Module $S_2$ and Module $S_3$ are $V_{dc1} > V_{dc2} > V_{dc3}$. However, as it is shown in Table 1, when the total voltage-level changes from 2 to 1, at the same time, the rank number of the DC-side voltage changes as $V_{dc1} > V_{dc3} > V_{dc2}$, the voltage level of cell 2 will change from 2 to −2, namely the voltage-level jump appears. The voltage-level jump will lead an equivalent increase in switching frequency. If the voltage-level jump needs to be avoided, the rank of the DC-side voltage could change while the modulation level $M$ equals 6, 0, −6. However, the limitation will cause dynamic performance loss. In addition—to keep the voltage-level change smooth—the −2 voltage level is banned while $M = 1$, as does $M = 2$ while $M = -1$. Therefore, the voltage-balancing capability of SPM could still be increasing.

**Table 1.** Voltage level allocation.

| $M$ | $S_{1st}$ | $S_{2nd}$ | $S_{3th}$ |
|---|---|---|---|
| 6 | 2 | 2 | 2 |
| 5 | 2 | 2 | 1 |
| 4 | 2 | 2 | 0 |
| 3 | 2 | 2 | −1 |
| 2 | 2 | 2 | −2 |
| 1 | 1 | 1 | −1 |
| 0 | 0 | 0 | 0 |
| −1 | −1 | −1 | 1 |
| −2 | −2 | −2 | 2 |
| −3 | −2 | −2 | 1 |
| −4 | −2 | −2 | 0 |
| −5 | −2 | −2 | −1 |
| −6 | −2 | −2 | −2 |

An ideal 3-D cube model voltage-balancing strategy is shown in Figure 4, three-module consist of $5^3 = 125$ switch states, which makes up the number of total voltage levels is 13. Each module is shown on an axis in Figure 4, a cube appears. Each color represents one kind of the total voltage level. The full line shows the path when the total voltage-level changes. For example, when the total voltage level is 13, which is on the point of (2,2,2), the red line shows the path of the total voltage between 13 and 12, the point changes from (2,2,2) to (2,2,1), (2,1,2) or (1,2,2). Thus, the voltage-level changes smoothly. To realize this strategy, the modulation needs to calculate voltage level of each module which is related to its DC-side voltage and the initial switch state. However, this also means that once a bug occurs in the calculation, all following calculations will error in succession.

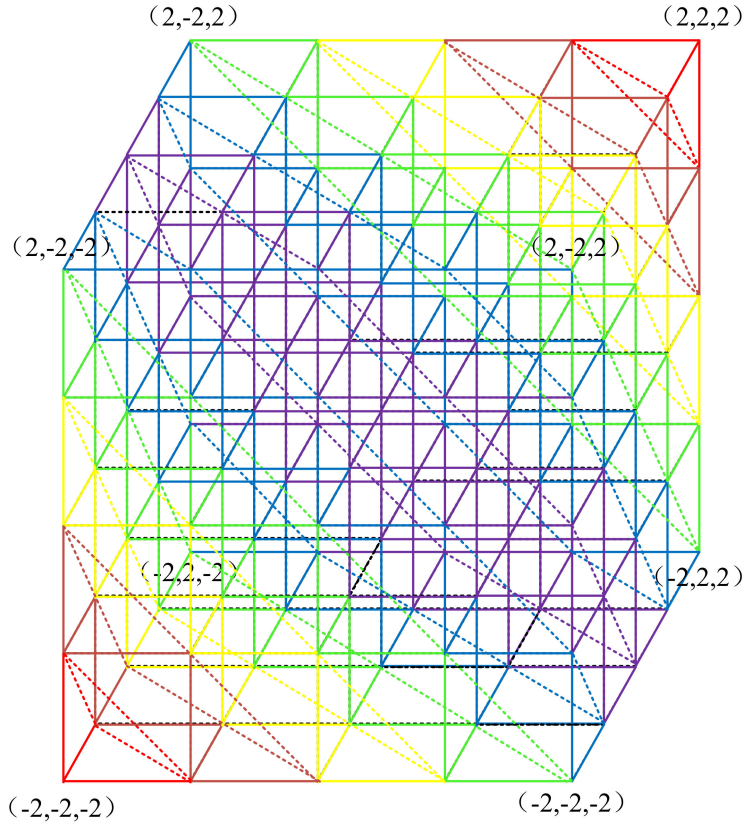



**Figure 4.** 3-D cube model voltage-balancing strategy.

Considering the advantage and disadvantages of the SPM and the calculation modulation above, the proposed SSM combines the advantage of them. The basic frame of the SSM is to calculate all the possibility of the switch-state changes, then list the changes in Table 1. Thus, a 3 Module 3LNPC-CC has 125 kinds of switch state and 6 kinds of the DC-side voltage rank. Each switch state has 2 kinds of voltage-level change tail, which is the voltage level plus and voltage level minus. Thus, the number of the total switch-state changes is about 1500. The 1500 kinds of switch states could be classified as follows:

(a) DC-side voltage rank: $V_{dc1} > V_{dc2} > V_{dc3}$, voltage level: positive plus, the number of module which the switch state is 2:0, initial example: (1,1,1), result example (2,1,1);

In this situation, the switch state of the module (Module 1) which DC-side voltage rank is the highest of all has rising space, thus the switch state of Module 1 increases from 1 to 2.

(b) DC-side voltage rank: $V_{dc3} > V_{dc2} > V_{dc1}$, voltage level: positive plus, the switch state of Module 3 is 2, initial example:(1,1,2), result example (1,2,2);

In this situation, the switch state of the module (Module 3) which DC-side voltage rank is the highest of all, but it has no rising space, thus the switch state of Module 2 increases from 1 to 2, which has the second-highest of the DC-side voltage rank.

(c) DC- side voltage rank: $V_{dc2} > V_{dc3} > V_{dc1}$, voltage level: positive plus, the switch state of Module 3 is 2 and the switch state of Module 2 is 2, initial example:(−1,2,2), result example (0,2,2);

In this situation, the switch state of the module (Module 2) which DC- side voltage rank is the highest of all, but it has no rising space, neither does Module 3, thus the switch state of Module 1 increases from −1 to 0, which has the second-highest of the DC-side voltage rank.

(d) DC- side voltage rank: $V_{dc1} > V_{dc2} > V_{dc3}$, voltage level: positive minus, the number of module which the switch state is −2:0, initial example:(1,1,1), result example (1,1,0);

In this situation, the switch state of the module (Module 3) which DC- side voltage rank is the lowest of all has falling space, thus the switch state of Module 3 decreases from 1 to 0.

(e) DC- side voltage rank: $V_{dc3} > V_{dc2} > V_{dc1}$, voltage level: positive minus, the switch state of Module 1 is −2, initial example:(1,2, −2), result example (1,1, −2);

In this situation, the switch state of the module (Module 3) which DC- side voltage rank is the lowest of all, but it has no falling space, thus the switch state of Module 2 increases from 2 to 1, which has the second-highest of the DC-side voltage rank.

(f) DC- side voltage rank: $V_{dc1} > V_{dc2} > V_{dc3}$, voltage level: negative plus, the number of module which the switch state is 2:0, initial example:( −1, −1, −1), result example (−1, −1,0);

In this situation, the switch state of the module (Module 3) which DC- side voltage rank is the lowest of all has rising space, thus the switch state of Module 3 increases from −1 to 0.

(g) DC- side voltage rank: $V_{dc3} > V_{dc2} > V_{dc1}$, voltage level: negative plus, the switch state of Module 1 is 2, initial example:( −1, −1, −2), result example (−1,0, −2);

In this situation, the switch state of the module (Module 1) which DC- side voltage rank is the lowest of all, but it has no rising space, thus the switch state of Module 2 increases from −1 to 0, which has the second-highest of the DC-side voltage rank.

(h) DC- side voltage rank: $V_{dc1} > V_{dc2} > V_{dc3}$, voltage level: negative minus, the number of module which the switch state is -2:0, initial example:( −1, −1, −1), result example (−1, −1, −2);

In this situation, the switch state of the module (Module 3) which DC- side voltage rank is the highest of all has rising space, thus the switch state of Module 3 decreases from 1 to 0.

(i) DC- side voltage rank: $V_{dc3} > V_{dc2} > V_{dc1}$, voltage level: negative minus, the switch state of Module 1 is −2, initial example: −2, −1, −1), result example (−2, −2, −1);

In this situation, the switch state of the module (Module 3) which DC- side voltage rank is the highest of all, but it has no falling space, thus the switch state of Module 2 increases from −1 to −2, which has the second-highest of the DC-side voltage rank.

(j) DC- side voltage rank: $V_{dc2} > V_{dc3} > V_{dc1}$, voltage level: negative minus, the switch state of Module 3 and Module 3 are −2, initial example:(−2, −2,1), result example (−2, −2,0);

In this situation, the switch state of the module (Module 2) which DC- side voltage rank is the highest of all, but it has no falling space, neither does Module 3, thus the switch state of Module 1 decreases from 1 to 0, which has the second-highest of the DC-side voltage rank.

(k) The special situation; (2,2,2) cannot be added anymore, and the (−2, −2, −2) cannot be reduced any more.

The changes of switch states are calculated and ranked, to make a list and saved in the controller. Then the modulation will work as the list arranging. In addition, the result of the modulation will operate like Figure 4 shows. First, the SSM chooses the proper switch state to balance the voltage smoothly. Second, the SSM could choose the off-line switch state—the final result of the switch state could be generated as a table, avoiding the complex calculations while 3LNPC-CC is working. Finally, the SSM is easy to extend as the off-line calculating. Compared to traditional strategies, the proposed SSM is optimized, simplified and extendable. Although the expression of the SSM is complex, the calculation while the SSM working is much easier than that of [13] and [20].

### *3.2. The Balance Range of the Proposed Strategy*

Although the proposed voltage-balancing strategy provides a strong balance capability for 3LNPC-CC, the balance range has its limits. In order to find the boundary of the balance capability, the mathematical model of balance capability is established in this section, based on the conservation of energy theorem.

First, the balance index $\zeta$ must be defined in Equation (3), which can quantitatively measure the degree of voltage imbalance. In the traditional voltage-balancing algorithm, the definition of balance index is always dependent on power. However, it is difficult for traditional definitions to maintain uniformity at different power levels. Thus, based on the normalization technique, the balance index $\zeta$ is defined by DC-side voltage reference and DC-side voltage difference. If all DC-side inputs are equal to the rated voltage, the balance index $\zeta$ is equal to zero. Similarly, if one module develops an open-circuit fault of DC side, the balance index $\zeta$ is equal to 0. Thus, full range of load can be represented regardless of the power level of system:

$$\zeta = \frac{n \cdot (v_{dc.\max} - v_{dc.\min})}{\sum v_{dc}} \tag{3}$$

Second, the relationship between the balance index $\zeta$ and energy flow can be established in Equation (4). Due to the structure of 3LNPC-CC, all modules are cascaded with a similar current flow even if one module is faulty. Thus, the balanced index is proportional to DC-voltage, DC-power and energy flow of each module. In Equation (4), the $\Delta v_{dc}$, $\Delta W$ and $\Delta E$ are different from DC-voltage, power and energy flow between faulty modules and other normal modules. Moreover, $k_1$ and $k_2$ are the proportional factor in the process, which have no dimensions:

$$\zeta = \frac{\Delta v_{dc}}{\sum v_{dc}} = k_1 \frac{\Delta W}{\sum W} = k_2 \frac{\Delta E}{\sum E} \tag{4}$$

Next, the mathematical model of the proposed voltage-balancing strategy is established in Equation (5). According to Equation (5), it indicates that the range of voltage-balancing is determined by the difference in energy flow, including input energy and output energy. The input energy can be changed by the value of DC-side voltage while the output energy can be controlled by the proposed voltage-balancing strategy. Thus, in Equation (5), the energy flow difference can be described where $PWM_{fault}(m,\omega t)$ is the voltage level of the faulty module at the moment of $t$ and $\omega$ is the angular frequency of 3LNPC-CC. $v_{dc}$ and $i_s$ is the DC-side voltage and AC-side current of 3LNPC-CC, respectively:

$$\zeta = \Delta v_{dc} / \sum v_{dc} = \Delta W / \sum W = \frac{\int_0^{2\pi} v_{dc} i_s PWM_{fault}(m, \omega t) dt}{\int_0^{2\pi} v_{dc} i_s \sin \omega t dt} \tag{5}$$

Finally, the relationship between balance index $\zeta$, modulation index $m$, and module number $n$ can be illustrated in Figure 5. In respect to the fixed module number, the boundary of voltage-balancing is composed of two parts. Taken the 3 modules system as an example, when modulation index is lower than 0.82, the voltage-balancing can be acquired no matter how serious the input situation is. However, when modulation index is higher than 0.82, the voltage-balancing capability is deceased. Voltage-balancing can only be achieved under specific load conditions. When modulation index is close to 1, the voltage-balancing capability hardly exists. Additionally, with the increasing of module numbers, the voltage-balancing capability is stronger. However, in consideration of the engineering requirements, the module number needs to be as little as possible. Thus, one compromise must be made between voltage-balancing capability and module number. The calculation result is shown in Figure 5.

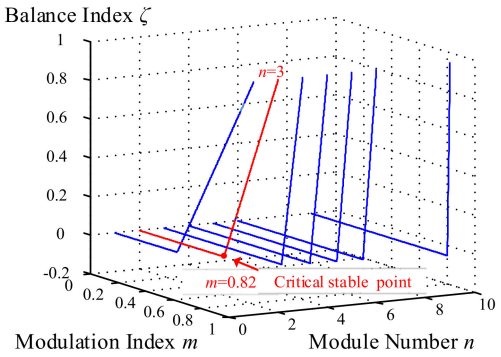



**Figure 5.** Balance boundary of 3LNPC-CC.

## 4. Simulation and Experiment

### *4.1. Simulation*

The simulation of the proposed SSM is built in Matlab/Simulink, a three-Module 3LNPC-CC to verified it. The detailed parameters of the simulation are shown in Table 2, where the DC-side voltage is about 48 V in each module.

In order to verify the unit power factor of the AC-side achieved by the control strategy of 3LNPC-CC, the output voltage and current of the 3LNPC-CC is simulated and shown in Figure 6. In the initial stage, the 3LNPC-CC operates under the modulation index of 0.6, the AC-side voltage and current keep the same phase and the frequency. When the sudden change of modulation index comes at 0.445 s, the amplitude of the AC-side voltage and current changes to 120 V and 2.5 A, respectively and the system enters a new steady-state rapidly. After the sudden change, the 3LNPC-CC operates under the modulation index of 0.8 and still keeps the unit power factor operation.

As shown in Figure 7, the DC-side source of Module 3 develops an open-circuit fault. After the open-circuit fault of the DC side, the whole output port voltage $u_{ab}$ still remain stable and the number of voltage level is eleven under the modulation index of 0.8. The whole output port voltage $u_{ab}$ is shaped like a regular staircase wave, which indicates the good performance of the control strategy. However, the output port voltages of each module are no longer the staircase waves. As is obviously seen in Figure 7, Module 1 and Module 2 transfer their switching frequency to Module 3. Module 1 and Module 2 remain in switching states 2 and −2 most of the time while Module 3 changes its switching states rapidly for the purpose of balancing the DC-side voltage. More important, the voltage level of three modules is changed only 1 or −1 at one time, the short circuit and overvoltage which may happen in bridge arm are prevented. Thus, the voltage level of Module 3 is operated as the strategy needs.

In order to verify the effectiveness of the proposed strategy, the DC-side source of Module 3 is set to have an open-circuit fault before the 3LNPC-CC starts. The DC-side voltages of three modules are shown in Figure 8. In the beginning, $V_{dc1}$ and $V_{dc2}$ remain stable at 48 V and $V_{dc3}$ is 0 because of the open-circuit fault. After the response time of 0.055 s, $V_{dc3}$ increases rapidly to 48 V due to the proposed strategy. When the 3LNPC-CC enters the stable period, DC-side voltages of each module keep the same track at 48 V with a low amplitude ripple. In this way, the validity of the proposed strategy is proved.

With reference to Figure 9a–c, each DC-side voltage with different modulation index is illustrated based on the proposed strategy. The DC-side source of Module 3 is cut off at 0.15 s due to the open-circuit fault in all these three figures. In Figure 9a, the modulation index is 0.78 which is lower than its critical value 0.82, the DC-side voltage-balancing will be maintained after the open-circuit fault. In Figure 9b, the modulation index is the critical value 0.82, $V_{dc3}$ is parallel to $V_{dc1}$ and $V_{dc2}$ and the system is in a critical stable state. However, in Figure 9c, the modulation index is 0.88, and the system works out of the balanced area. Therefore, $V_{dc3}$ cannot be balanced at 48 V, which verifies the correctness of the proposed reconfiguration capability calculation in Section 4.

**Table 2.** Simulation Parameter.

| Parameter Name | Value |
|---|---|
| Number of the modules | 3 |
| DC-side voltage of each module | 48 V |
| Modulation index | 0.8 |
| Carrier wave frequency | 2 kHz |
| Switches | IGBT |
| Filter inductance | 1 mH |
| Filter capacitor | 10 μF |
| DC-side capacitor | 470 μF |
| Load | 50 Ω |

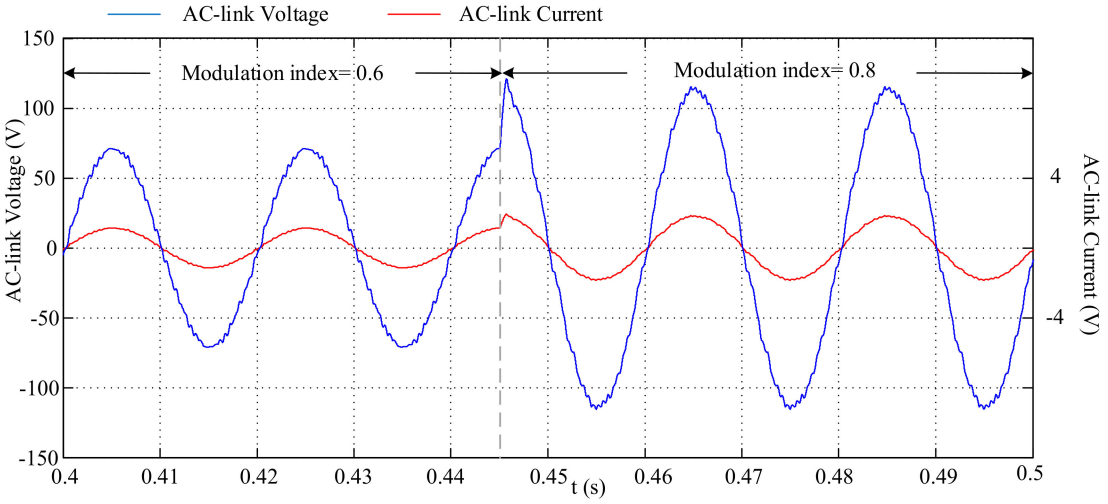



**Figure 6.** AC-side voltage and current for a step in the modulation index.

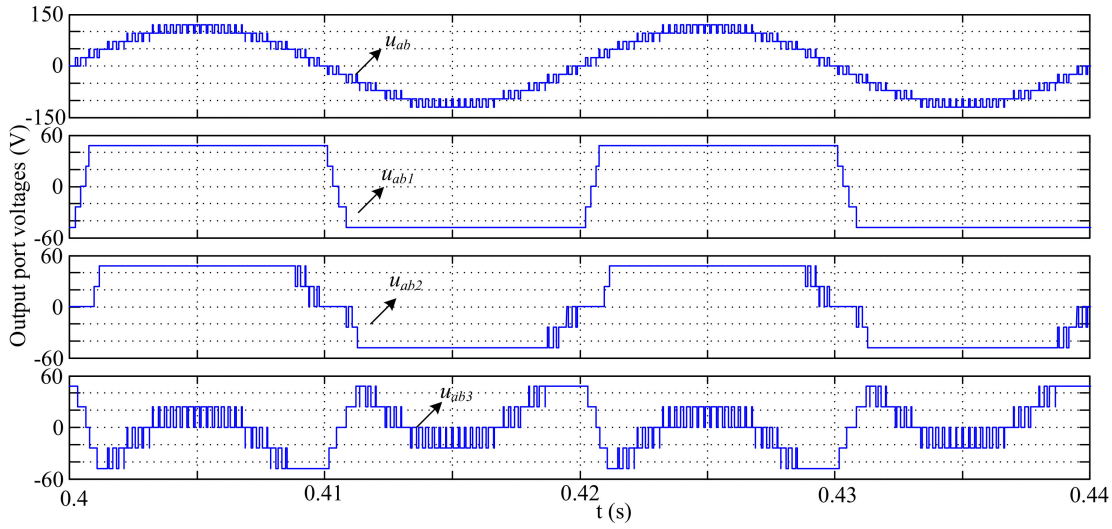



**Figure 7.** Output port voltage of the proposed strategy.

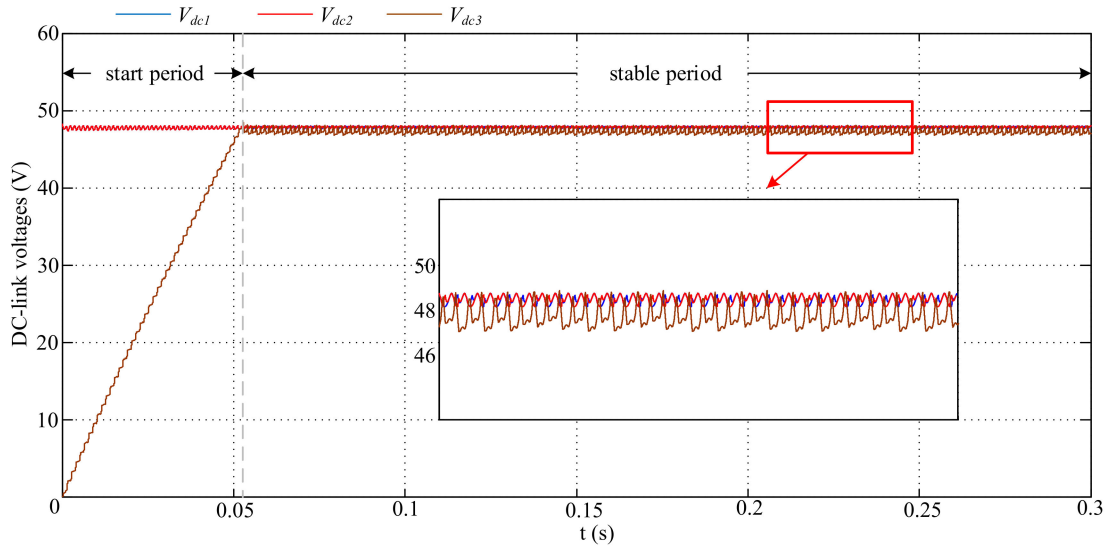
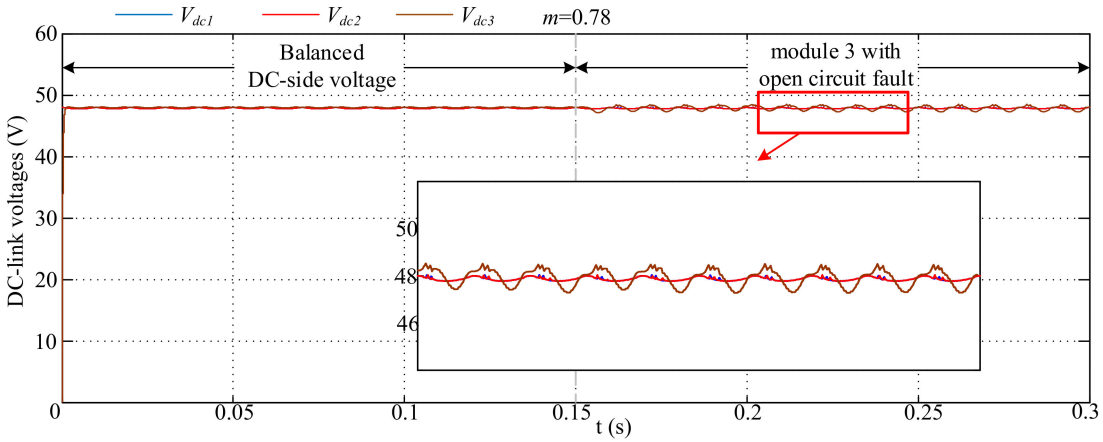
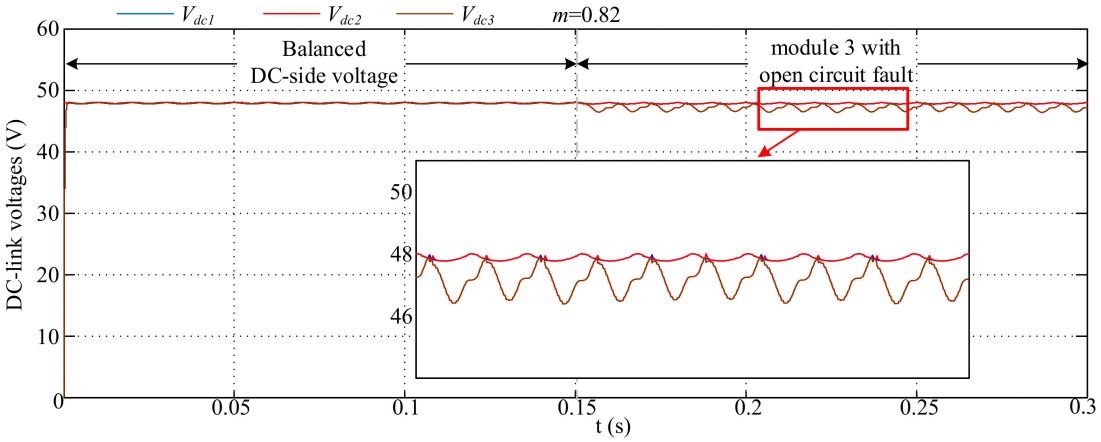



**Figure 8.** DC-side voltages of each module.




(**a**)




(**b**)

**Figure 9.** *Cont.*

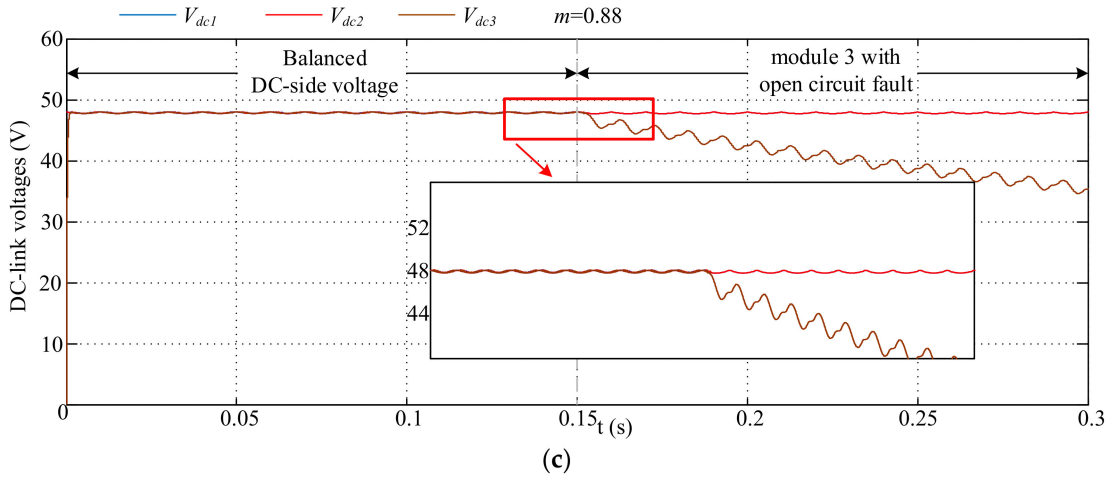



**Figure 9.** DC-side voltages of each module. (**a**) Each DC-side voltage of the proposed strategy ($m$ = 0.78); (**b**) each DC-side voltage of the proposed strategy ($m$ = 0.82); (**c**) each DC-side voltage of the proposed strategy ($m$ = 0.88).

### *4.2. Experiment*

The low power experiment of a three-Module 3LNPC-CC prototype was designed to illustrate the dynamic performance of the proposed strategy. The parameter and the prototype are shown in Table 3 and Figure 10, respectively. A prototype was designed and two experiments are conducted to illustrate the dynamic performance of the proposed strategy. The FPGA EP4CE10F17C8N is used as a core controller, the process of FPGA is mainly made up of PLL, d–q decoupling (dq–abc), d—-q coupling (abc–dq), PI controller, PSC modulation and SSM proposed, as it is shown in Figure 11.

In order to verify the topology and the modulation of the prototype, the experiment of using phase-shift carrier (PSC) modulation and the proposed strategy is completed, the static waveform of the 3LNPC-CC is shown in Figure 12. In Figure 12a, an eleven-level output voltage is synthesized by the PSC-SPWM, while the voltage levels of each module are evenly distributed. Figure 12b shows the static wave of output voltage when the proposed strategy works, while Module 1 is regarded as the one who suffers from open-circuit fault. Based on the proposed strategy, the voltage level of Module 1 changes rapidly, while the voltage level of the other two modules remains at switching state ± 2 for most of the time. Moreover, the total output voltage $U_{ab}$ of the 3LNPC-CC remains normally, although the output voltage of each module is rearranged by the proposed strategy.

Figure 13 shows the start period of the 3LNPC-CC when Module 1 suffering from open-circuit fault. Because of the DC-side voltage loss, the input and output voltage of Module 1 is 0 at the beginning. Figure 13a is the output voltage of the 3 modules. Because of the open-circuit fault of Module 1, the total output voltage $U_{ab}$ deformed during the start period. Gradually, with the DC-side voltage of Module 1 recovering, the $U_{ab}$ become normal. However, due to the proposed strategy, the switching times of the open-circuit fault module increases to keep its DC-side voltage steady. Although the switch states of all modules are rearranged, the total voltage of 3LNPC-CC remains unchanged. Figure 13b illustrates the DC-side voltage of each module and the AC-side current. Similarly, the DC-side voltage of Module 1 is zero at the beginning. After the proposed strategy is activated, the DC-side voltage of Module 1 increases and traces the DC-side voltage of the other two modules within 0.4 s. This means that the SSM could ensure the 3LNPC-CC working while the DC-port of one module of a module is fault while it. Figure 13b also shows the proposed SSM could balance the DC-link voltage under the modulation index among 0.8 while one module of 3LNPC-CC under 0.8, this keeps the average level such as [12–14] and [20].

**Table 3.** Experiment parameters.

| Parameter Name | Value |
|---|---|
| Number of the cascade module | 3 |
| DC-side voltage | 48 V |
| Output voltage | 85 V |
| Controller (FPGA) | EP4CE10F17C8 N |
| Switch (IGBT) | FGA25N120ANTD |
| DC-side capacitance | 470 μF |
| Filter inductance | 1 mH |
| Filter capacitance | 10 μF |
| Load | 50 Ω |
| Carrier wave frequency | 2 kHz |

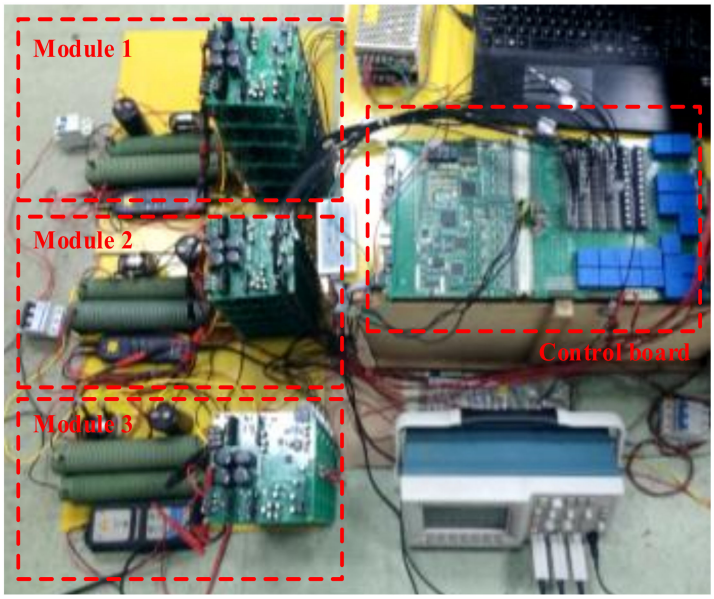



**Figure 10.** Prototype of the three-module 3LNPC-CC.

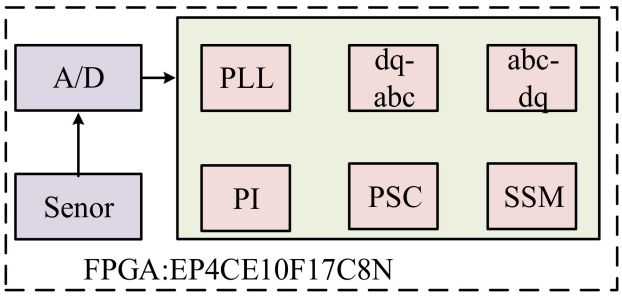
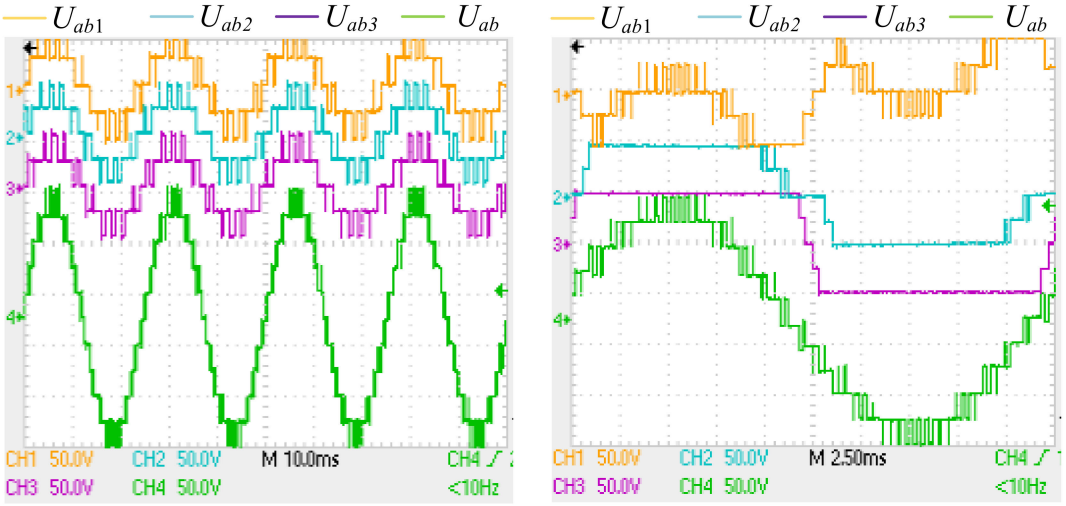
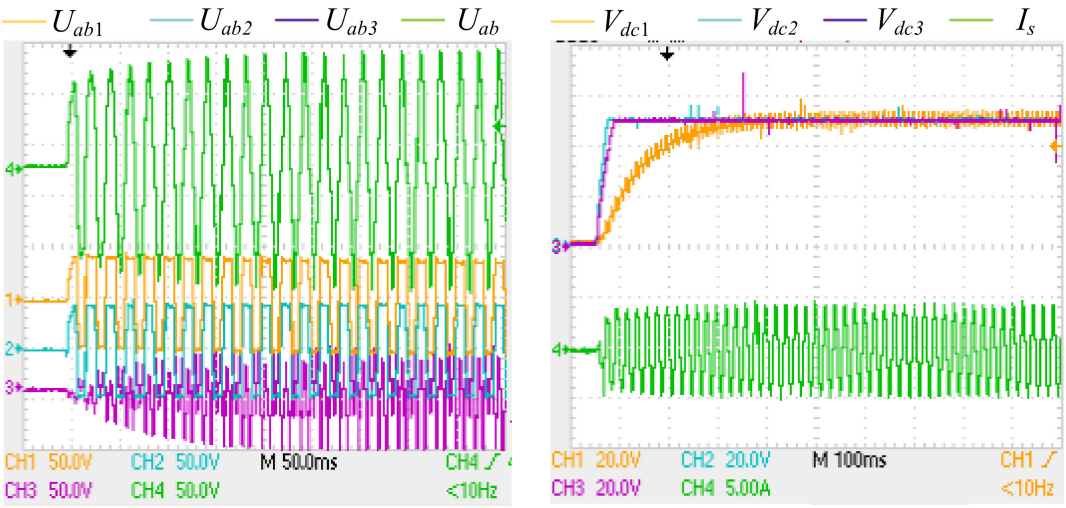



**Figure 11.** Controller.




(**a**) (**b**)

**Figure 12.** The static waveforms of three-module 3LNPC-CC. (**a**) The PSC modulation of 3LNPC-CC; (**b**) proposed strategy of 3LNPC-CC.




(**a**) (**b**)

**Figure 13.** Experiment start with Module 1 suffering from an open-circuit fault. (**a**) Output voltages of 3LNPC-CC; (**b**) DC-side voltages and AC-side current.

Figure 14 shows the DC-side voltages and AC-side current using the proposed strategy of three-module 3LNPC-CC. When the system enters the steady-state operation, the open-circuit fault of DC-side source occurs in Module 1 and the DC-side source is completely cut off. Therefore, the DC-side voltage of Module 1 dropped greatly about 28 V. However, under the influence of the proposed strategy, the DC-side voltage of Module 1 does not drop continuously and increases to 50 V at the end. The process of recovering is less than 0.04 s, which is faster than the start experiment. In this way, the validity of the proposed strategy is proved. Furthermore, the fluctuation is much smaller than [13], similar with others article.

Since the modulation index could have an effect on the voltage-balancing capability, Figure 15 shows the DC-side voltages and AC-side current with different modulation index and the DC-side source of Module 1 is cut off in Figure 15a–c. In Figure 15a, the system works at a limit condition with the modulation index of 0.82 and the DC-side voltage of Module 1 fluctuates in a large range. As shown in Figure 15b,c, the proposed strategy is verified with a modulation index of 0.8 and 0.78. The fluctuation of DC-side voltages of Module 1 decreases and the DC-side voltage of three modules

follow the trails of each other because the applying of the proposed strategy. These experimental results are in accordance with the theoretical and simulation analysis.

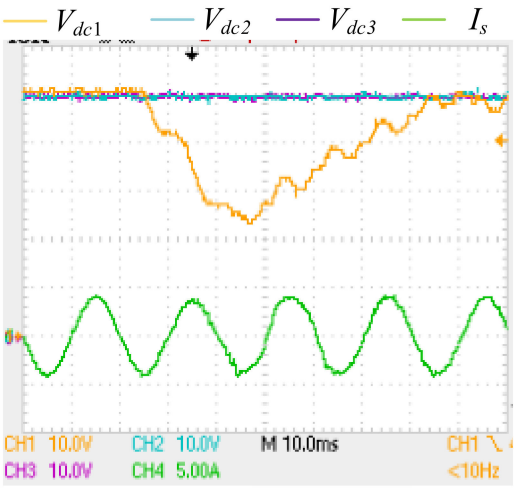



**Figure 14.** DC-side voltages and AC-side current during DC-side source open-circuit fault.

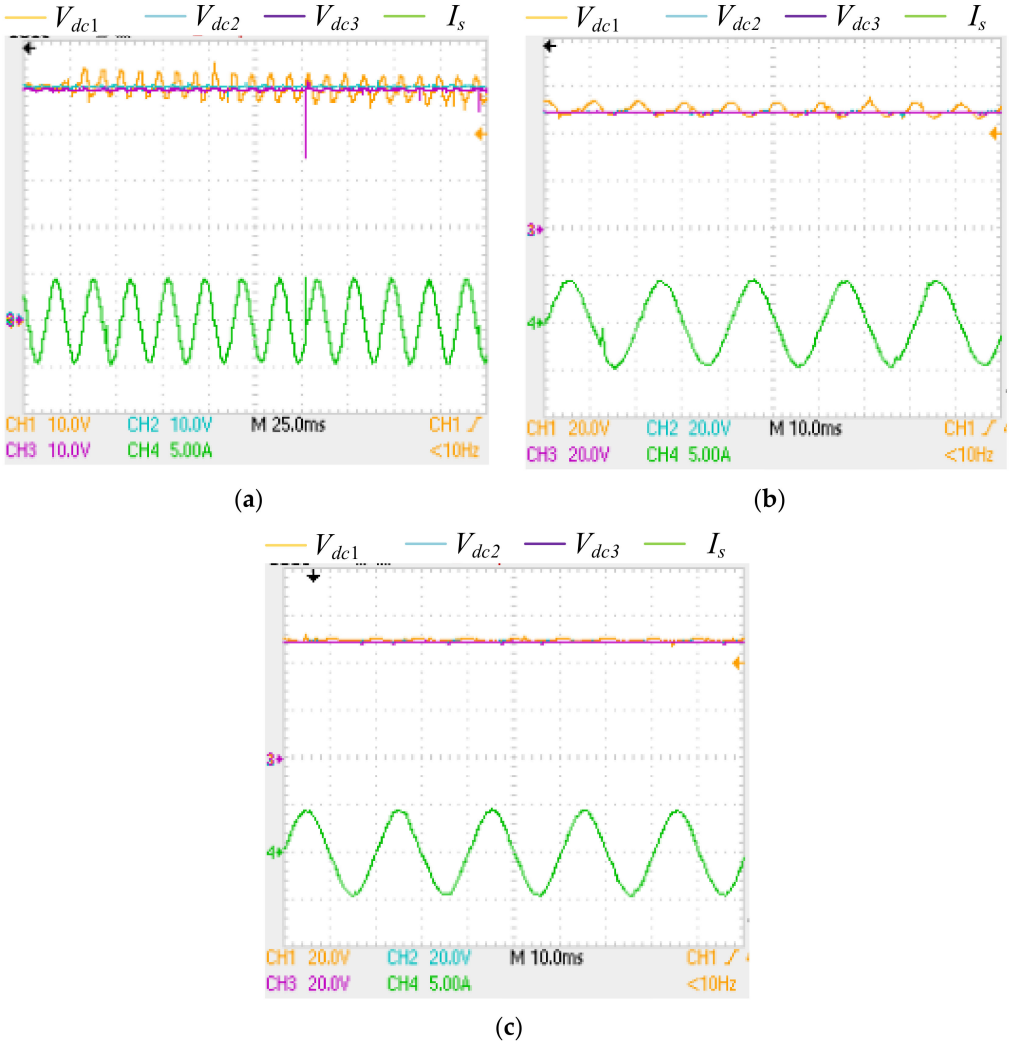



**Figure 15.** DC-side voltages and AC-side current under different modulation index. (**a**) m = 0.82; (**b**) m = 0.8; (**c**) m = 0.78.

## 5. Conclusions

In this paper, a novel voltage-balancing strategy applied in a three-level neutral-point clamped cascaded converter is proposed to improve the balance of DC-side voltage. The basic configuration of 3LNPC-CC was designed, and the normal control strategy is illustrated, which achieved the regulation of AC-side voltage and current. A SSM of voltage-balancing strategy and the optimal path of voltage level transformation is also proposed. The input DC-side voltage can be regulated—even if one module develops an open-circuit fault of DC-side. The voltage level can be changed smoothly in this strategy. The recovery time of the input DC-side source from full power to no power is approximately 0.28 s. The main contributions of this paper are as follows:

(a) An SSM structure of 3LNPC-CC is proposed, which represents the change of different working states. When the input of 3LNPC-CC is unbalanced, the normal path of working states is changed and an improved path of working states is assigned that can recover the balance of DC-side balance. The advantage of the improved path is a smooth switch of voltage level during the whole working cycle;

(b) A coordinated control strategy is designed, which is composed of double-closed loop and sequence smooth modulation, based on AC-side voltage, AC-side current and DC-side voltage. The performance of AC-side and DC-side can be assured at the same time;

(c) An experiment platform is established in this paper. The dynamic performance is illustrated when DC-side input develops an open-circuit fault and must be cut off. The DC-side voltage can be recovered even if the extreme imbalance occurs. The ripple of the DC-side voltage is improved with the decreasing of modulation index. Additionally, the 3LNPC-CC has an excellent dynamic performance.

In conclusion, the advantages of proposed SSM are as follows:

(a) The proposed SSM could balance the DC-link voltage of the DC-port fault module, while the modulation index is under 0.8. The voltage-balancing ability is fairly high-level among voltage-balancing strategies;

(b) The proposed SSM is able to find a proper switch-state path for voltage balancing that is suitable for the voltage balancing strategy. In addition, the proper switch-state path ensures the minimum switch-state changes and minimum frequency;

(c) The proposed SSM takes the advantages from the smooth modulation and SPM by using a calculated table—not only for finding the proper switch state, but also for avoiding complex calculations while the 3LNPC-CC is working.

**Author Contributions:** L.Y. conceived the strategy and the experiments; X.P. performed the experiments; S.G. analyzed the data; C.Z. acquihired the financial support for the project leading to this publication. S.G. contributed experiment prototype and L.Y. wrote the paper. All authors have read and agreed to the published version of the manuscript.

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**Conflicts of Interest:** The authors declare no conflict of interest.

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