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A Single-Voltage-Source Class-D Boost Multi-Level Inverter with Self-Balanced Capacitors

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Abstract: A symmetric single-source 7-level DC-AC converter with voltage gain of 3 and self-voltage balance is presented by combining the Class-D amplifier and the diode-clamped DC-AC converter. There is only one switch is switched for any time in this circuit. As a result, the conversion efficiency can be upgraded significantly as well as the control strategy can be simplified considerably. In the paper, the operation principle and circuit design of this converter are analyzed in detail, and its feasibility and effectiveness are verified by simulation and digital control, respectively.

Keywords: multi-level inverter; diode clamped inverter; self-balanced capacitor; self-voltage balance

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1. Introduction

With the rapid development of technology and power electronics in recent years [1], a large amount of low-frequency harmonic currents, generated by the non-linear loads of power electronics, flow into the power system, resulting in increasingly serious harmonic pollution of the power system. As the generated harmonic is larger or exceeds the tolerance value, it may cause other nearby non-linear load products to mis-activate, mis-measure, degrade efficiency or even burn out. The International Electrotechnical Commission (IEC) in Europe has issued IEC 61000-3-2 Harmonic Specification [2], and the Japanese Specifications have also issued JIS-C-61000-3-2 standard [3] has been promulgated by the Japanese Specifications to formally regulate the harmonics generated by electronic devices.

In order to cope with the AC systems used in the market, DC-AC converters or AC-DC converters combined with DC-AC converters are used to convert the green energy to AC power. Therefore, DC-AC converters are one of the most important technologies used in the industry today. Multi-level DC-AC converters use switching paths to make the output voltage appear in a hierarchical pattern and increase the number of levels or filters to make the output voltage appear like a sine wave. The output voltage of the multistage DC-AC converter is in the form of a stratified output voltage so that the voltage stress on the switch can be clamped. Therefore, the high-voltage AC output can be achieved with the switch with the low-voltage stress. Figure 1 shows the generalized classification of voltage-type multi-stage DC-AC converters, which contain neutral point clamped converters [4], the flywheel capacitor type [5] and the series-connected type [5].

Flying capacitors are DC-AC converters that use multiple capacitors connected to each other to achieve output voltage clamping. However, a large number of capacitors and complex control methods are required to balance the capacitor voltage to achieve a hierarchical output voltage [5].

Although the cascade structure has the characteristics of modular design and floating power supply, it requires multiple independent power inputs to achieve a hierarchical AC output voltage [5].

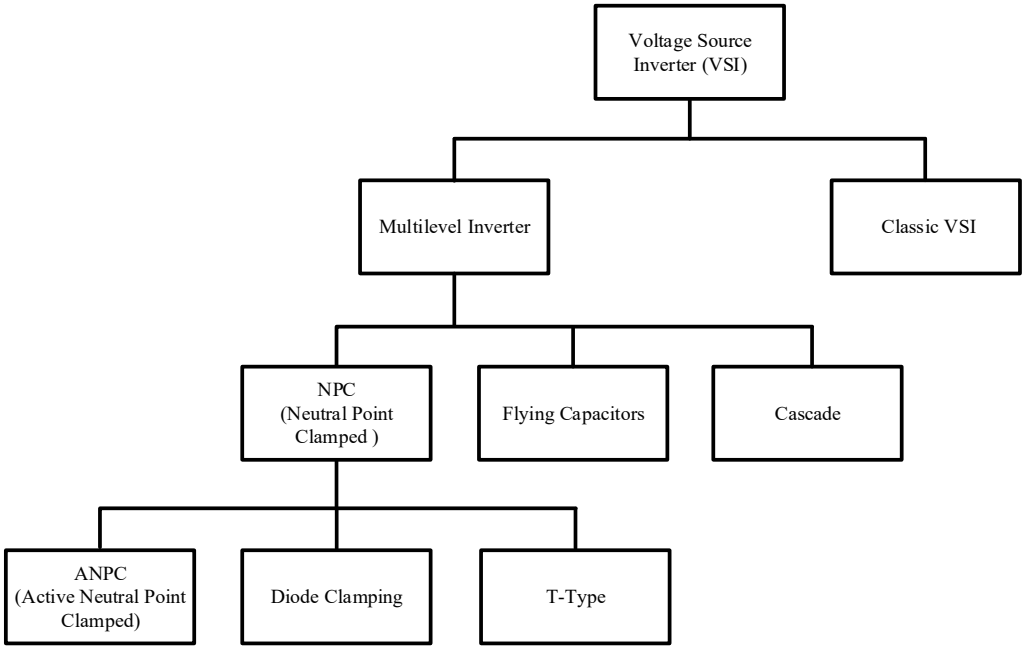

Figure 1. DC-AC converter classification.

The circuit structure presented in [4] uses diodes and switches to create a neutral potential for the output voltage, which has a lower harmonic content than the conventional two-level DC-AC converter. The pulse width modulation (PWM) method proposed in [6] is based on the comparison of sine and triangle waves to generate suitable driving signals to turn on/off switches, which in turn make the output voltage appear in the form of a sine wave.

Studies referenced in [7,8] propose a neutral point clamping circuit. The circuit structure presented in [7] consists of six switches and a floating capacitor to realize a DC-AC converter with a voltage gain of 1 at 5 levels. The circuit structure presented in [8] is similar to that of [7] and adopts nine switches to realize a DC-AC converter with a voltage gain of 1.5 at 7 levels. By adding two additional switches and one floating capacitor, a DC-AC converter with a voltage gain of 1 at 9 levels can be realized with eleven switches, two DC link capacitors, and two floating capacitors. At the same time, with the same number of components, a DC-AC converter with a voltage gain of 2.5 at 11 levels can be realized by only changing the switching sequence. The literature [9] proposes a circuit that can operate in a reactive power condition by combining the concept of diode clamping, flywheel capacitor, and T-type active clamping to design a DC-AC converter with a voltage gain of 0.5 at 5 levels.

In [10], a step-up converter is used to provide the required step voltage for the H-bridge output. This approach not only achieves the purpose of the DC step-up voltage but also uses the inductor of this circuit as the input inductor to reduce the input current ripple. In addition, in [10], a 5-, 7-, and 15-level circuit structure is proposed to realize the high-level AC output and applied to the fuel cell system. In [11,12], floating capacitors are used to increase the number of levels of the DC-AC converter. This circuit structure can be used to increase the voltage gain with a single power input, but the floating capacitor must be self-balanced to output the step voltage. The structure proposed in [11] uses two floating capacitors and two diodes along with the required switching sequence to achieve self-balancing of the capacitors, resulting in a voltage gain of 2 at nine levels. In [12], a circuit with three floating capacitors and three diodes is presented, and the capacitor voltage is one to two times the input voltage, so the number of output levels can reach nine with a voltage gain of 4. However, this method will increase the voltage stress on the switch, so a higher specification switch is required. In [13], a modified pulse width modulation control

method is proposed to combine the active clamping circuit with the H-bridge structure so that the capacitor voltage across the H-bridge can maintain self-balance in each level.

Therefore, based on the Class-D amplifier and the traditional diode clamped DC-AC converter, a single-voltage-source symmetric two-output-port 7-level DC-AC converter along with only one switch is switched for any time in this circuit is presented. As a result, not only the proposed converter can possess a 3-voltage-gain and the adopted capacitors with the inherent capability of self-voltage balance, but also the conversion efficiency can be upgraded significantly as well as the control strategy can be simplified greatly. In addition, due to the symmetric structure, the interchangeability of mass production of this converter can be easily realized. In the paper, the feasibility of the proposed circuit is demonstrated by simulating a 300 W prototype circuit, and the effectiveness of this prototype circuit is confirmed by using a single comparator PWM voltage feedback control [14] based on the field programmable gate array (FPGA).

2. Operating Principles of the Proposed Circuit

Figure 2 shows the proposed single-voltage-source class-D 7-level DC-AC converter. This converter is composed of 12 switches, 8 diodes, and 4 energy-transferring capacitors.

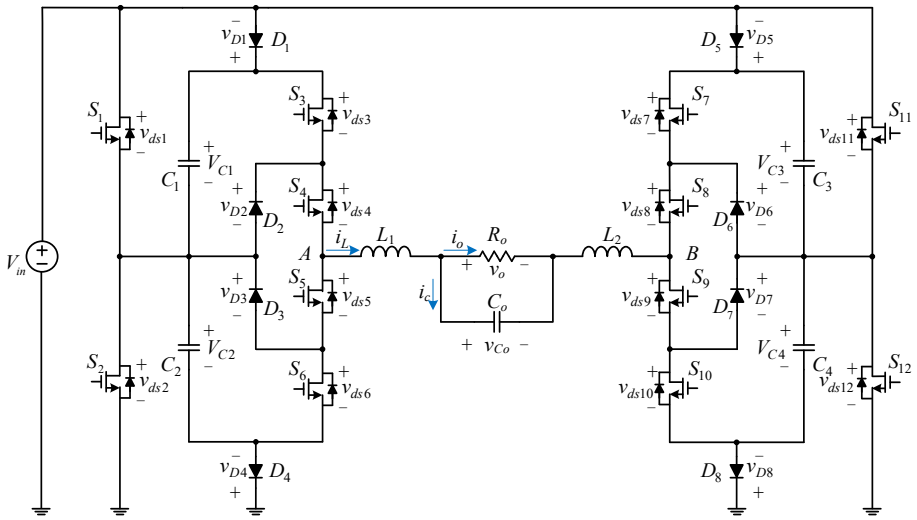

Figure 2. Single-voltage-source Class-D 7-level DC-AC converter.

Before the operating analysis, a brief description of the relevant symbol definitions and required assumptions is given: (1) V_{in} is the input voltage, v_o is the output voltage, and the voltage v_{Co} of the filter capacitor C_o is equal to v_o; (2) S_1 to S_{12} are the switches with the corresponding cross-voltages v_{ds1} to v_{ds12}; (3) D_1 to D_8 are diodes with the corresponding cross-voltages, v_{D1} to v_{D8}; (4) C_1 to C_4 are energy-transferring capacitors with the corresponding currents i_{C1} to i_{C4}; (5) the values of the energy-transferring capacitors are assumed to be large enough that the voltages across them can be considered constant, i.e., $V_{C1} = V_{C2} = V_{C3} = V_{C4}$; (6) i_o is the output current; (7) i_L is the current flowing through inductors L_1 and L_2; and (8) all components are regarded as idea except for the body diodes of the switches.

Figure 3 shows the waveforms of the gate driving signals for switches. Since the gate driving signals are the same at the positive and negative half cycles, only the positive half-cycle is analyzed. The circuit operation behavior has five stages, only one switch will be in PWM switching in each stage, and the other switches are normally on or normally off. Since stage I is equivalent to stage V and stage II is equivalent to stage IV, only stages I, II, and III are analyzed.

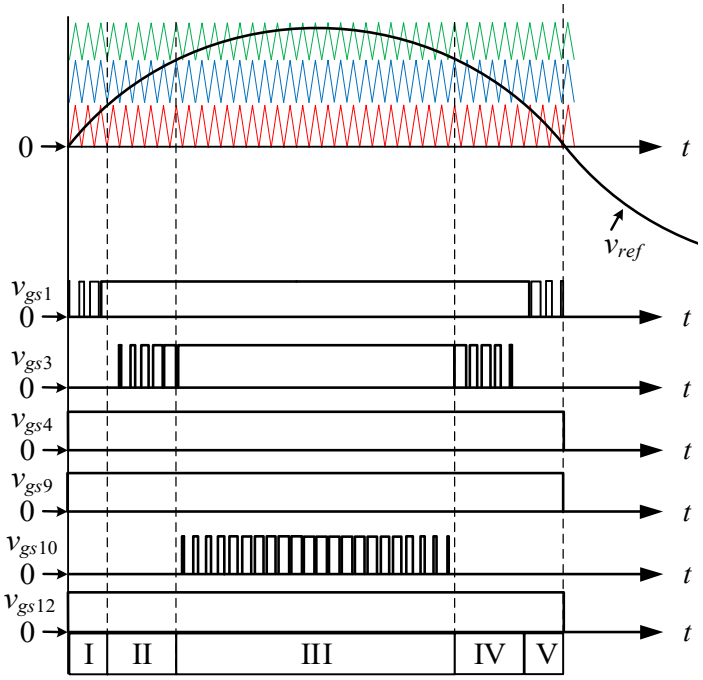

Figure 3. Waveforms of the gate driving signals for switches.

When the output voltage is at the positive half cycle, the switches S_4, S_9, and S_{12} remain on, and the switches S_2, S_5, S_6, S_7, S_8, and S_{11} remain off. The output voltage can be determined by switching S_1, S_3, and S_{10} to determine the circuit operation behavior of stages I, II, and III, respectively. Note that in the following descriptions, only one switch is switched at any time, and the current path is marked to show that the converter satisfies energy conservation and Kirchhoff's voltage and current laws in any stage.

2.1. Stage I

Only the switch S_1 is switched as in Figure 4.

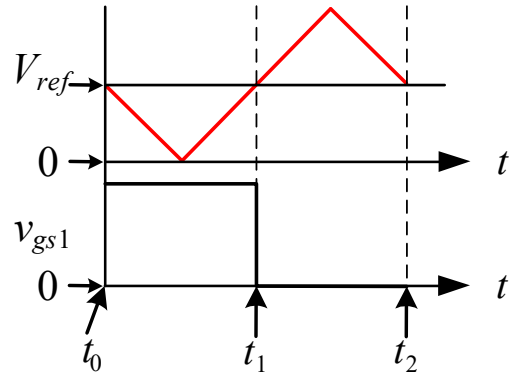

Figure 4. Gate driving signal for S_1.

Interval $[t_0 \leq t \leq t_1]$: The switch S_1 is on, but the switches S_3 and S_{10} are off. As shown in Figure 5, the current flowing through the inductors L_1 and L_2 will form a circuit loop from the input voltage to the switches S_1, S_4, S_9, S_{12} and the diodes D_2, D_7; therefore, the voltage across the terminals A and B is

$$v_{AB} = V_{in} \tag{1}$$

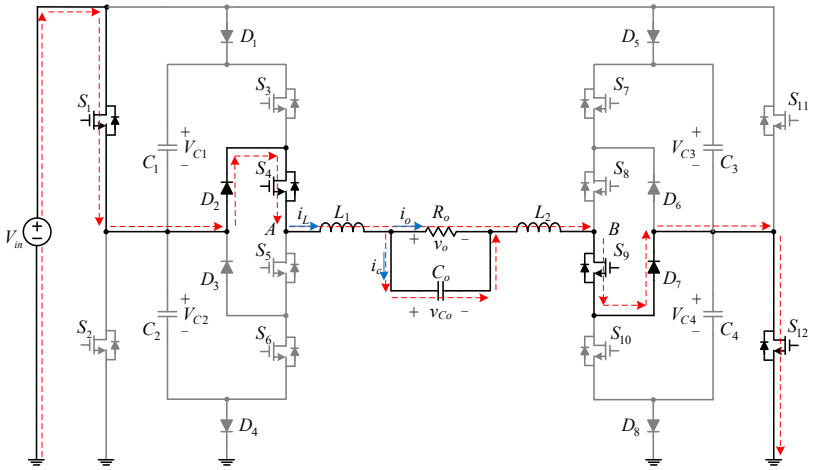

Figure 5. Current flow direction of stage I when switch S_1 is on.

Interval $[t_1 \leq t \leq t_2]$: The switches S_1, S_3 and S_{10} are all off. At the same time, the input voltage is disconnected from the output. As shown in Figure 6, the current flowing through the inductors L_1 and L_2 will form a circuit loop from the switches S_4, S_9, S_{12} to the diodes D_2, D_7 and the body diode of the switch S_2, so the voltage across the terminals A and B is

$$v_{AB} = 0 \tag{2}$$

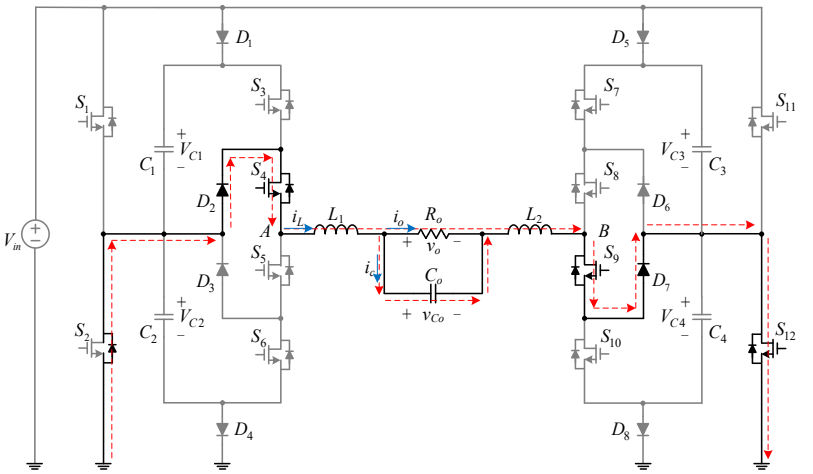

Figure 6. Current flow direction of stage I when switch S_1 is off.

2.2. Stage II

Only the switch S_3 is switched as in Figure 7.

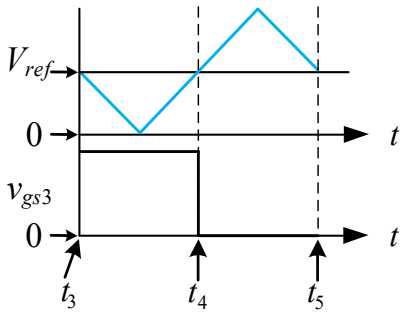

Figure 7. Gate driving signal for S_3.

Interval $[t_3 \leq t \leq t_4]$**:** The switches S_1 and S_3 are on, but the switch S_4 is off. As shown in Figure 8, the current flowing through the inductors L_1 and L_2 will form a circuit loop from the input voltage to S_1, S_3, S_4, S_9, S_{12} and the diode D_7; therefore, the voltage across the terminals A and B is

$$v_{AB} = V_{in} + V_{C1} = 2V_{in} \tag{3}$$

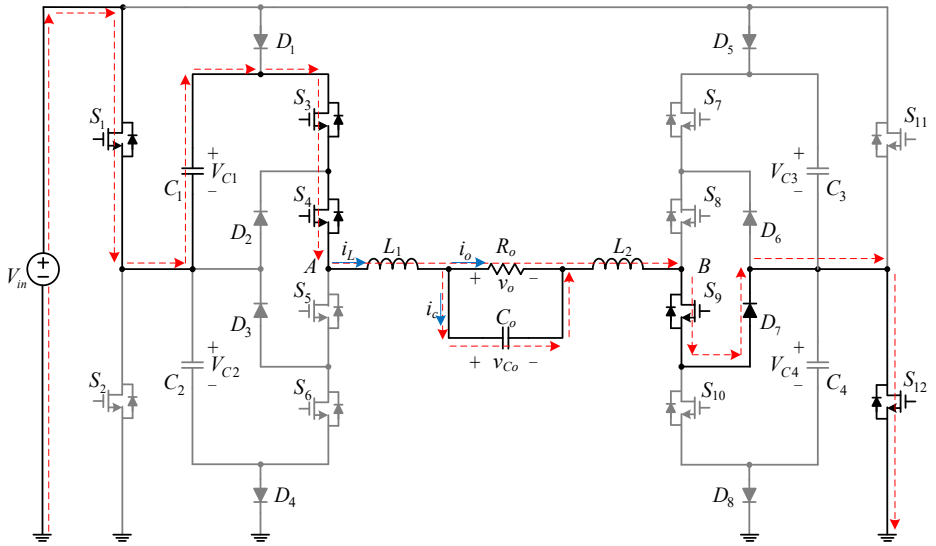

Figure 8. Current flow of stage II when switch S_3 is on.

Interval $[t_4 \leq t \leq t_5]$: The switches S_3 and S_{10} are off, but the switch S_1 is on. As shown in Figure 9, the current flowing through the inductors L_1 and L_2 will form a circuit loop from the input voltage to the switches S_1, S_4, S_9, S_{12} and the diodes D_2, D_7; therefore, the voltage across the terminals A and B is

$$v_{AB} = V_{in} \tag{4}$$

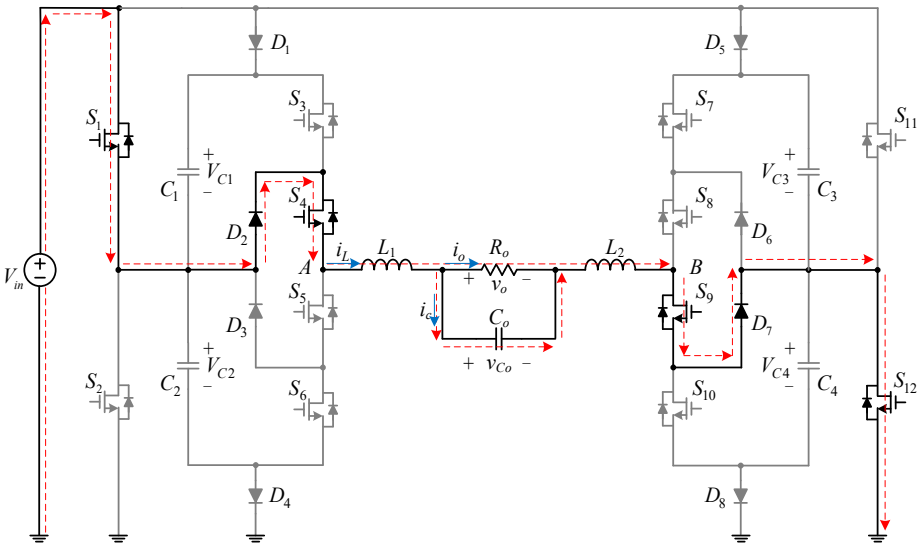

Figure 9. Current flow direction of stage II when switch S_3 is off.

2.3. Stage III

Only the switch S_{10} is switched as in Figure 10.

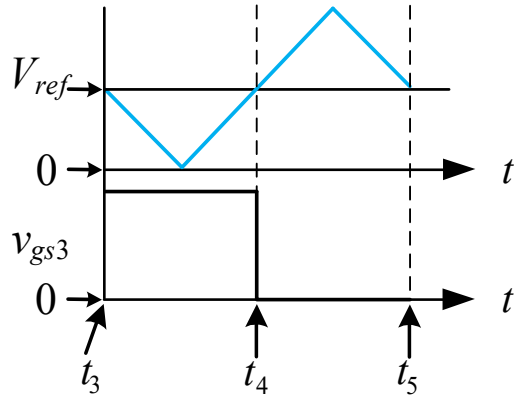

Figure 10. Gate driving signal for S_{10}.

Interval $[t_6 \leq t \leq t_7]$: The switches S_1, S_3 and S_{10} are turned on. As shown in Figure 11, the current flowing through the inductors L_1 and L_2 will form a circuit loop from the input voltage to the switches S_1, S_3, S_4, S_9, S_{10} and S_{12}; therefore, the voltage across the terminals A and B is

$$v_{AB} = V_{in} + V_{C1} + V_{C4} = 3V_{in} \tag{5}$$

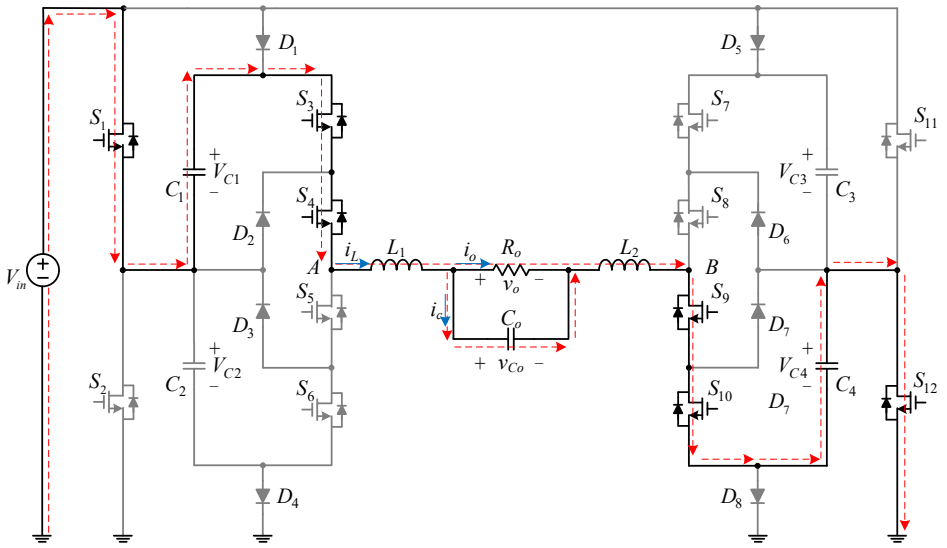

Figure 11. Current flow direction of stage III when the switch S_{10} is on.

Interval $[t_7 \leq t \leq t_8]$: The switch S_{10} is off, but the switches S_1 and S_3 are on. As shown in Figure 12, the current flowing through the inductors L_1 and L_2 will form a circuit loop from the input voltage to the switches S_1, S_3, S_4, S_9, S_{12} and the diode D_7; therefore, the voltage across the terminals A and B is

$$v_{AB} = V_{in} + V_{C1} = 2V_{in} \tag{6}$$

From the above analysis, we can see that the proposed 7-level DC-AC converter has the voltage gain of 3, which can be obtained based on (7):

$$\text{Voltage Gain} = \frac{\text{AC output voltage amplitude}}{\text{Total DC input voltage}} \tag{7}$$

Table 1 shows the switching behavior of the proposed single voltage source Class-D 7-level DC-AC converter and its corresponding maximum voltage stress, where f_{PWM} is the switching frequency and f_{line} is the output voltage frequency or mains frequency. For the

output voltage at positive half cycle to be considered, the switches S_2, S_5, S_6, S_7, S_8 and S_{11} are off, their maximum voltage stress is V_{in}. In addition, all the diodes have the maximum voltage stress of V_{in}.

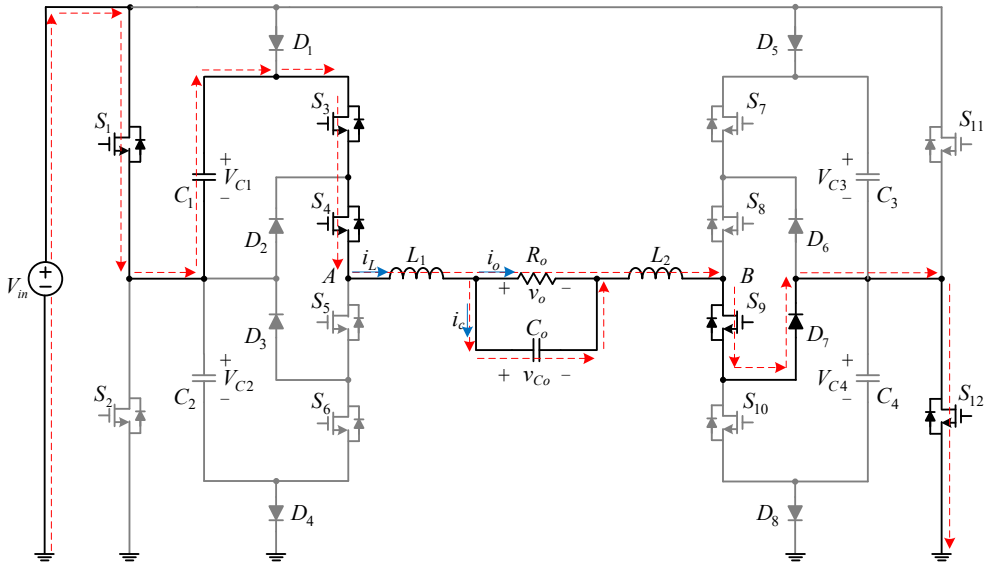

Figure 12. Current flow direction of stage III when switch S_{10} is off.

Table 1. Switching behavior of the proposed 7-level DC-AC inverter.

		S_1	S_3	S_4	S_9	S_{10}	S_{12}
Switching Frequency		f_{pwm}	f_{pwm}	f_{line}	f_{line}	f_{pwm}	f_{line}
Stage I	Switching type	1, 0	0	1	1	0	1
	Maximum voltage stress	V_{in}	V_{in}	0	0	V_{in}	0
Stage II	Switching type	1	1, 0	1	1	0	1
	Maximum voltage stress	0	V_{in}	0	0	V_{in}	0
Stage III	Switching type	1	1	1	1	1, 0	1
	Maximum voltage stress	0	0	0	0	V_{in}	0

Table 1 shows the switching behavior of the proposed single voltage source Class-D 7-level DC-AC converter and its corresponding maximum voltage stress. In addition, the switches S_1, S_3 and S_{10} take important roles in stages I, II and III.

3. Design Considerations

The specifications of the proposed 7-level DC-AC converter are shown in Table 2.

Table 2. Specifications of the 7-level DC-AC converter.

Input voltage (V_{in})	56 V
Output voltage (mains) frequency (f_{line})	60 Hz
Output voltage (v_o)	110 V_{rms}
Rated output power ($P_{o,rated}$)/Rated output current ($I_{o,rated}$)	300 W/2.72 A_{rms}
Minimum output power ($P_{o,min}$)/Minimum output current ($I_{o,min}$)	75 W/0.68 A_{rms}
Switching frequency (f_s)	60 kHz

3.1. Design of Energy-Transferring Capacitors

The energy-transferring capacitors used in the proposed converter can be divided into two types according to the discharge time. The first one is the capacitor C_1 (=C_3) which provides the AC output of stage II and stage III, whereas the second one is the capacitor C_4 (=C_2) which provides the AC output of stage III. Therefore, based on the concept from Figure 13 and by using Equations (8) and (9), the charge discharged from C_1 and C_4 over one cycle of the mains power can be calculated:

$$\Delta Q_{C1} = \frac{1}{\omega}\int_{\frac{2\pi \cdot t_1}{T_{line}}}^{\pi - \frac{2\pi \cdot t_1}{T_{line}}} i_o \ \sin(\omega\ t) d\omega\ t \tag{8}$$

$$\Delta Q_{C4} = \frac{1}{\omega}\int_{\frac{2\pi \cdot t_2}{T_{line}}}^{\pi - \frac{2\pi \cdot t_2}{T_{line}}} i_o \ \sin(\omega\ t) d\omega\ t \tag{9}$$

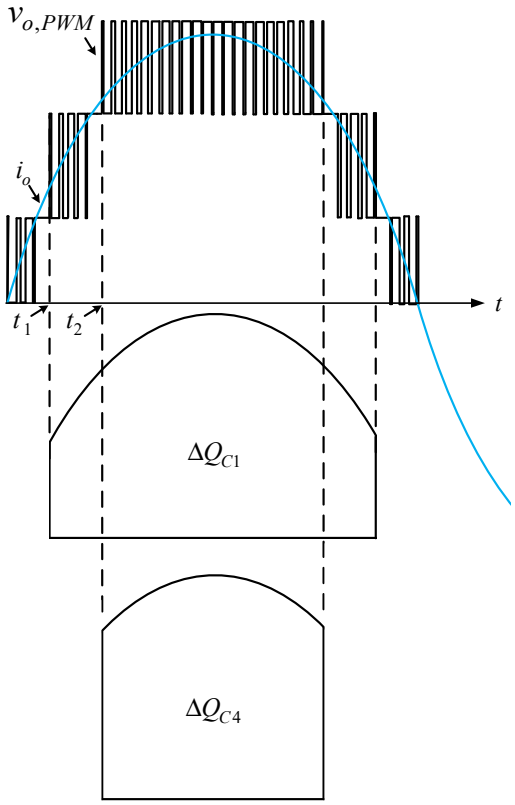

Figure 13. Charge of energy-transferring capacitors C_1 and C_4 during the discharge period.

According to (10), the voltage variation is proportional to the charge variation. Since the results of (8) and (9) can be obtained by PSIM simulation, the value of the capacitor can be worked out under a given voltage ripple percentage of 10% as below:

$$Q = CV \Rightarrow \Delta Q = C\Delta V \Rightarrow C = \frac{\Delta Q}{\Delta V} \tag{10}$$

$$\Delta V = 56 \times 10\% = 5.6 \text{ V} \tag{11}$$

$$C_1 = C_3 = \frac{\Delta Q_1}{\Delta V} = \frac{17.548 \text{ m}}{5.6} = 3.13 \text{ mF} \tag{12}$$

$$C_4 = C_2 = \frac{\Delta Q_4}{\Delta V} = \frac{8.52 \text{ m}}{5.6} = 1.52 \text{ mF} \tag{13}$$

Therefore, a 3.3 mF electrolytic capacitor is used for each capacitor, which has the voltage across it is equal to the input voltage. Since the derating of the electrolytic capacitor should be taken into considered, the voltage rating of the selected capacitor should be at least 1.25 times the input voltage, according to the usual thumb rule. Finally, a 3300 µF/100 V Rubycon electrolytic capacitor is chosen as each capacitor.

3.2. Design of the Filter

According to the harmonic voltage limit value proposed by IEEE 519-1992, the total harmonic distortion rate is up to 5% below 69 kV [15]. The proposed structure is a 7-level DC-AC converter with a double-ended symmetrical output, which has a filter shown in Figure 14. As generally known, the inductance has higher reactance for high frequency signals, whereas the capacitance has lower reactance for high frequency signals. Therefore, dividing the inductance of LC filter into L_1 and L_2 not only makes the differential-mode noise filtered by inductance and capacitance and not appear on the output load R_o, but also prevents the common-mode noise from affecting the circuit. Since the switching frequency f_s is 60 kHz, the corner frequency f_c is set at 6 kHz.

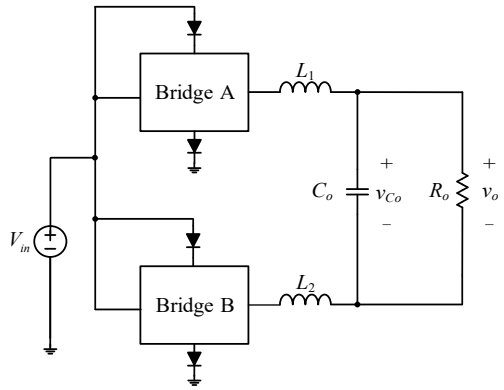

Figure 14. Filter circuit diagram for the output load.

The transfer function of the filter is shown in Equation (14), where $L = L_1 + L_2$:

$$H(s) = \frac{\omega_o}{s^2 + s\frac{Q}{\omega_o} + \omega_o^2} \tag{14}$$

In (14), we can find

$$\omega_o = 2\pi f_o = \sqrt{\frac{1}{LC_o}} \tag{15}$$

and

$$Q = R_o\sqrt{\frac{C_o}{L}} \tag{16}$$

Therefore, since f_c is 6 kHz, one relationship between L and C_o can be obtained based on (15):

$$LC_o = \left(\frac{1}{2\pi \times f_c}\right)^2 = \left(\frac{1}{2\pi \times 6\text{k}}\right)^2 = 0.703\text{n} \tag{17}$$

Additionally, by rearranging (16), the following equation can be obtained to be

$$\frac{C_o}{L} = \left(\frac{Q}{R_o}\right)^2 \tag{18}$$

Let the quality factor at rated load be 3 dB, that is, $\sqrt{2}$, and the output resistance R_o at rated load is 39.24 Ω. By substituting these values into (18), the other relationship between L and C_o can be obtained to be

$$\begin{aligned} &\frac{C_o}{L} = \left(\frac{\sqrt{2}}{39.24}\right)^2 = 1.3\ \text{m} \\ &\Rightarrow\ C_o = L \times 1.3\ \text{m} \end{aligned} \tag{19}$$

Substituting (19) into (17) yields

$$L = \sqrt{\frac{0.703\text{n}}{1.3\text{m}}} = 735.37\ \mu\text{H} \tag{20}$$

By substituting (20) into (19), the output capacitance can be obtained to be

$$C_o = 955\text{nF} \tag{21}$$

Finally, a 1 μF/275 V metal film capacitor is chosen as filter capacitor. The actual measured capacitance of 1.02 μF, which is brought into (17) to obtain the filter inductance of 690 μH. Since the filter inductor L is composed of two inductors L_1 and L_2 connected in series, the values of L_1 and L_2 are the same, equal to 345 μH.

4. System Block Diagram

Figure 15 shows the system block diagram of the proposed DC-AC converter. The system consists of the main circuit and feedback control circuit. The FPGA digital control core and digital-to-analog converter (DAC) are used to generate a sine wave used as voltage reference, and the ADC-free sampling circuit [14] sends the feedback signal v_{FB} to the FPGA to obtain the corresponding control force after calculation. This control force is then fed to the isolated gate driver to regulate the switch to achieve a stable output voltage.

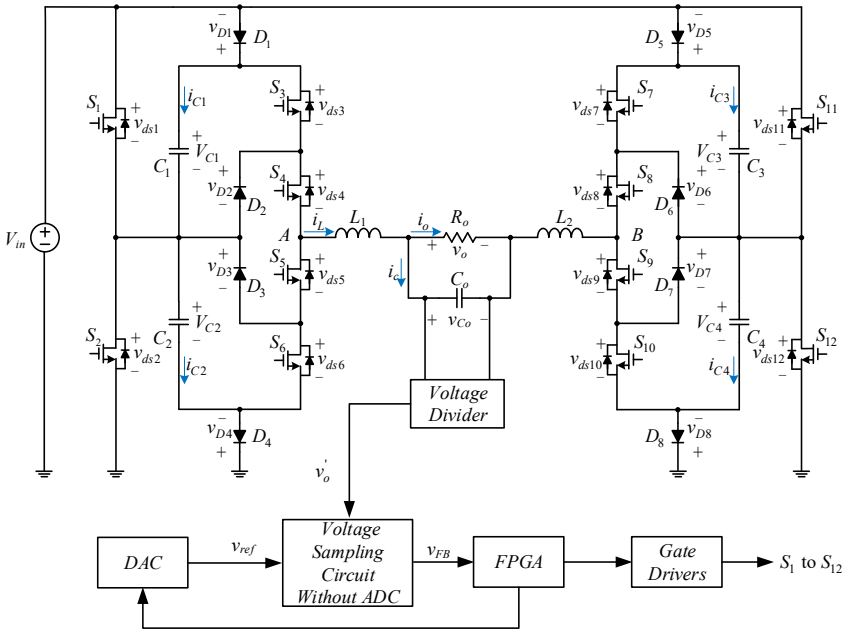

Figure 15. System block diagram of the proposed 7-level DC-AC converter.

5. Simulated and Experimental Results along with Discussions

Figure 16 shows the simulated and experimental waveforms of the proposed 7-level DC-AC converter at rated load, containing the output voltage v_o and output current i_o, the unfiltered output voltage v_{PWM}, and the voltages across C_1, C_2, C_3 and C_4, called V_{C1}, V_{C2}, V_{C3} and V_{C4}. From Figure 16a, it can be seen that the output voltage v_o and output

current i_o are AC output. From Figure 16b, it can be seen that the unfiltered output voltage v_{PWM}, formed by the high-frequency gate driving signals to turn on and off the switches, is filtered to obtain 60 Hz AC voltage. From Figure 16c,d, it can be seen that all the energy-transferring capacitors in the circuit have the characteristics of self-voltage balance. From the above simulated and experimental results, it can be seen that the proposed 7-level DC-AC converter structure is indeed feasible.

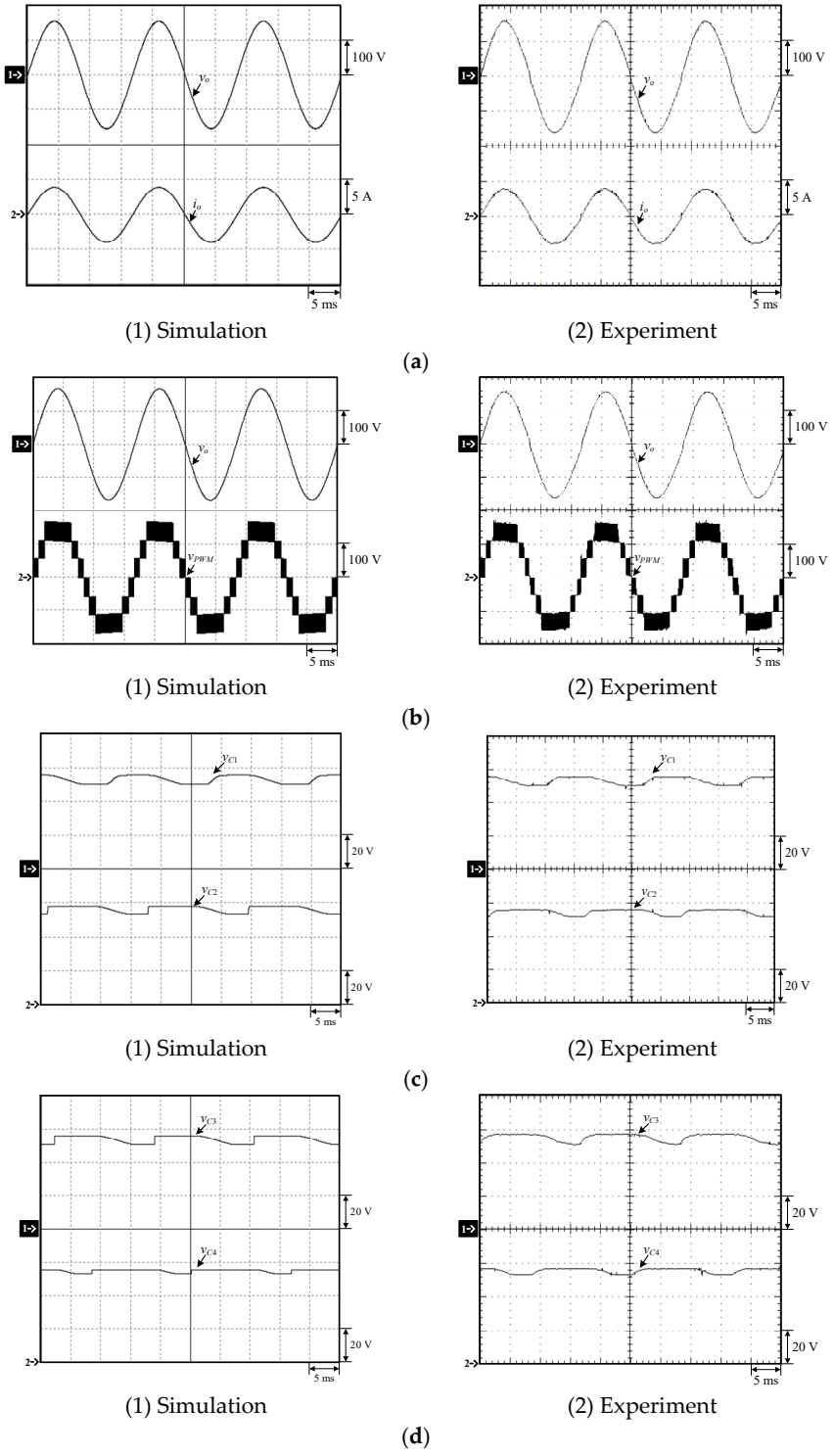

Figure 16. Simulated and experimental waveforms of the proposed DC-AC converter: (**a**) v_o and i_o; (**b**) v_o and v_{PWM}; (**c**) V_{C1} and V_{C2}; (**d**) V_{C3} and V_{C4}.

Figures 17 and 18 show the distribution of voltage harmonics at rated and minimum load, respectively. The corresponding total harmonic distortion (THD) is 2.75% and 4.1% at rated and minimum load, respectively, as measured by a power meter. The proposed 7-level DC-AC converter can indeed comply with the specifications of IEEE 519-1992, which states that the corresponding THD is less than 5%. Figure 19 displays the load transient response due to step load current change from 25% to 100% load. From this figure, it can be seen that the overshoot voltage is about 50 V and the recovery time is about 0.6 ms.

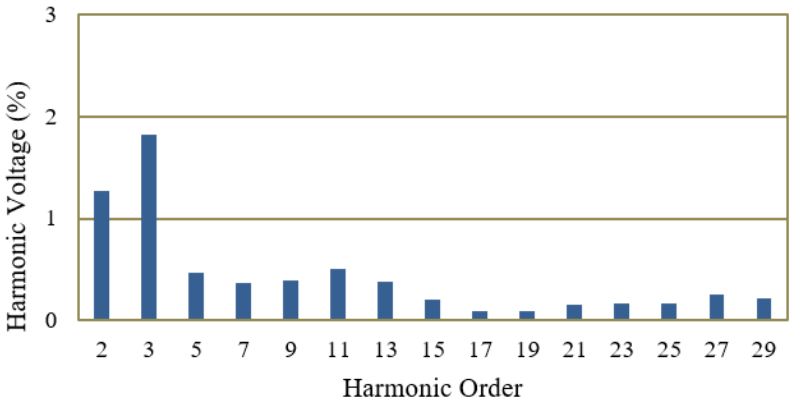

Figure 17. Distribution of harmonic voltages at rated load.

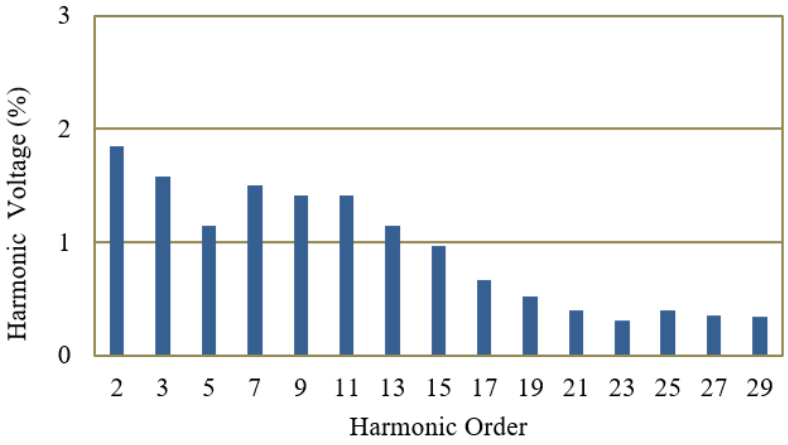

Figure 18. Distribution of harmonic voltages at minimum load.

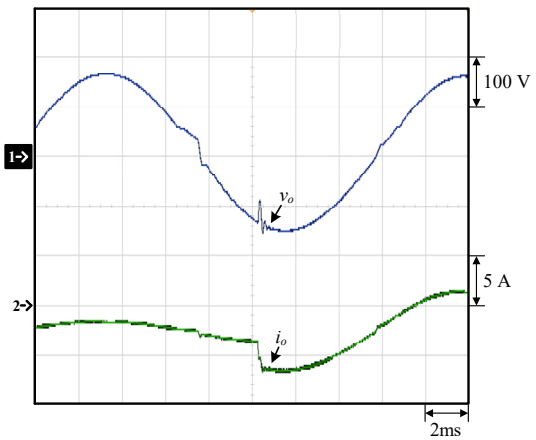

Figure 19. Load transient response due to step load current change from 25% to 100% load: (1) v_o; (2) i_o.

The efficiency of the proposed inverter under different loads is measured as shown in Figure 20. First, two digital meters, named Fluke 179, are used to measure the input voltage and the voltage across the current-detecting resistor, named shunt. Then, the output voltage, output current, total harmonic distortion, and harmonic voltage of each harmonic order are measured by using a power analyzer (PM1000+). Therefore, the input power and output power can be obtained. Moreover, the AC electronic load, named Prodigit 3255, is used at the load side. Finally, the obtained input power and output power are used to calculate the efficiency as shown in Figure 21. As can be seen in Figure 21, the proposed converter circuit belongs to a diode clamped circuit, causing the efficiency to be decreased when the load is higher.

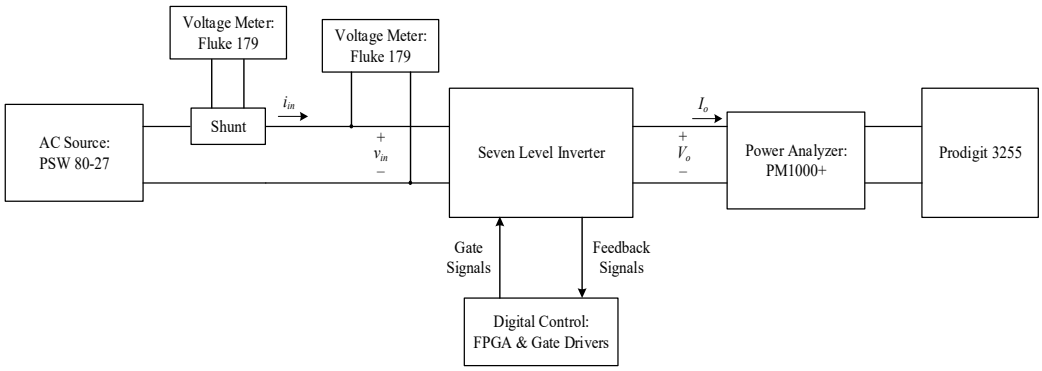

Figure 20. Block diagram of efficiency measurement.

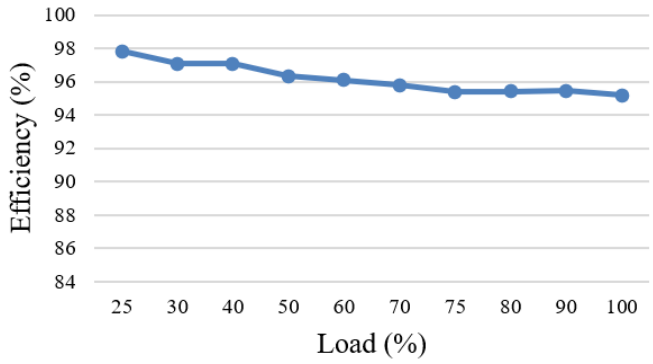

Figure 21. Curve of efficiency versus load.

6. Conclusions

This paper combines the Class-D amplifier and the conventional diode clamped DC-AC converter to create a single-voltage-source 3-voltage-gain 7-level DC-AC converter, where the DC link capacitors of the diode clamped DC-AC converter are used as energy-transferring capacitors to increase the output voltage and the number of levels. Due to the structure of this converter is symmetrical up and down, left and right, the interchangeability of mass production can be easily achieved. Furthermore, since only one switch operates at any time, not only the corresponding control is quite easy, but also any switch has very low switching voltage stress equal to the input voltage. Moreover, the proposed DC-AC converter has the highest conversion efficiency of 97.9% and the minimum THD of 2.75%, respectively.

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