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Analysis and Modeling of a Single-Power-Source T-Type 7-Level Single-Phase DC-AC Inverter with Voltage Gain of 3

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Abstract: This paper proposes a novel T-type 7-level single-phase DC-AC inverter having a single input power source, self-balancing, and voltage gain of 3 along with low total harmonic distortion (THD). Since the structure of the proposed 7-level DC-AC inverter is symmetrical, the interchangeability of mass production can be easily achieved. In addition, because only one switch works for all time, the switch has quite low switching loss and voltage stress as well as the control being very easy. Furthermore, not only the proposed 7-level DC-AC inverter is analyzed in detail by the operating principle, but also the mathematical model for the adopted level-shift sinusoidal pulse width modulation (LS-SPWM) for this multilevel DC-AC inverter is successfully developed by using the well-known state averaging technique widely employed in the DC-DC converter. As a result, the required proportional-integral (PI) controller, used in the closed loop, can be designed systematically and easily. Eventually, the feasibility and effectiveness of the proposed inverter are verified by simulated and experimental results.

Keywords: T-type; 7-level; single-phase; DC-AC inverter; modeling; voltage gain

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1. Introduction

1.1. Motivations

Multilevel DC-AC inverters (MLIs) are a popular solution for AC power sources, including renewable energy conversion such as wind energy [1,2], automotive [3–6], and photovoltaic application [3,7,8]. Compared to two-level voltage source inverters, MLIs have the advantages of low voltage stress, high efficiency, low common-mode voltage, as well as providing high quality output waveforms and improving the total harmonic distortion (THD) [9].

The basic operating principle of the multilevel DC-AC inverter is to utilize the switch path to render the output voltage stratified, and to upgrade the number of filters or levels to cause the output voltage to be sinusoidal-like. As the output voltage of an MLI is hierarchical, the voltage stress across the switch can be clamped. As a result, the high-voltage AC output can be realized by low-voltage components.

MLIs can be used in high power or low power. Generally, high power converters have the advantage that all semiconductors are rated to the same voltage, despite the ratio of output levels over the number of power semiconductors being relatively low compared to low power converters. Low power multilevel inverters are also a wide research field in which a large number of output voltage levels can be achieved by sacrificing the voltage rating of semiconductors. For switching topologies, on the other hand, MLIs can be divided into two major categories, containing step switching multilevel and pulse-width-modulated (PWM) switching multilevel.

The step switching multilevel DC-AC inverter employs DC power source, semiconductor elements and capacitors to synthesize the AC output voltage [10–12]. Although this inverter greatly reduces the number of switching cycles over one AC cycle, the DC-AC conversion current path is increased by too many semiconductor elements, thereby increasing turn-on loss. Furthermore, since multilevel DC-AC inverters operate at low frequencies, the switched capacitors require a large capacity to provide step voltages. In addition, the load dynamic response of such an inverter is rather slow.

Voltage source multilevel PWM switching DC-AC inverters can be mainly classified into four types, containing flying capacitor type, cascade type, diode clamp type, and T-Type. The diode clamp type can be furthermore classified into two types: one is neutral point clamped (NPC), the other is active neutral point clamped (ANPC). In general, the voltage-type multilevel DC-AC inverters can be classified by Figure 1.

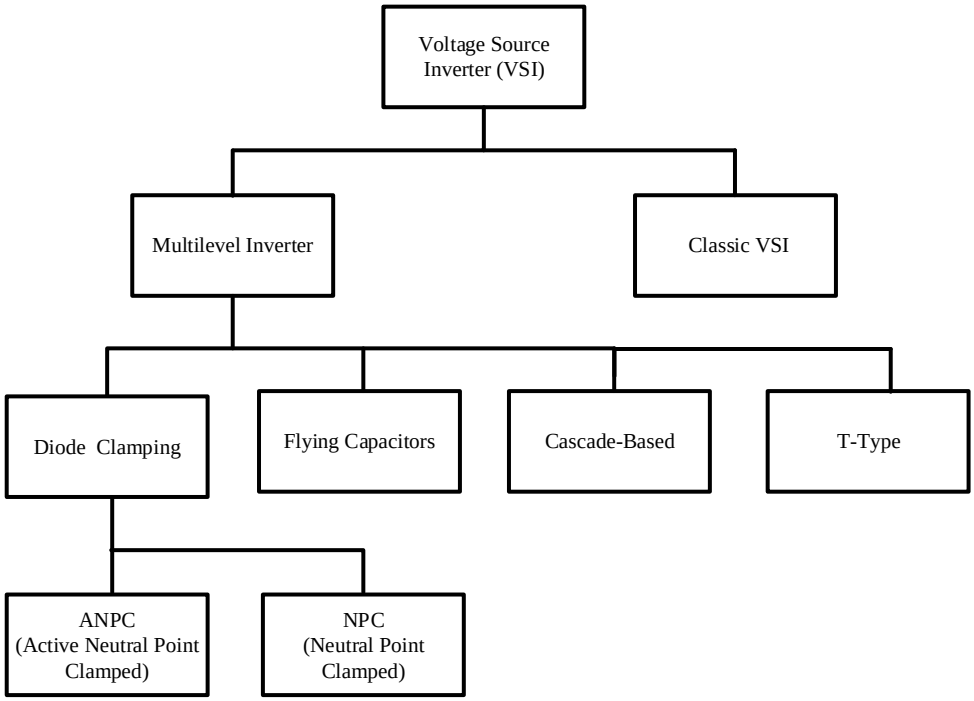


Figure 1. Voltage source DC-AC inverter classification.

The flying-capacitor-based multilevel DC-AC inverter is designed to achieve the AC output voltage clamped by interconnecting multiple capacitors [13,14]. However, a large number of capacitors and complicated control strategies for capacitor voltage balancing are required to obtain a stratified output voltage.

The cascade-based multilevel DC-AC inverter is the only type having a modular design concept and adopts the fewest components among the three types [15,16]. However, the need for multiple independent power supplies to synthesize the required levels of the AC output voltage limits its applications.

The diode-clamp-based multilevel DC-AC inverter employs a diode and a switch to generate the potential of the neutral point for the output voltage, and a PWM (Pulse Width Modulation) method to create the appropriate gate signal to turn on the switch. This results in lower harmonic components compared to the traditional 2-level DC-AC inverter [17–19]. However, the diode clamp circuit has the problem of not achieving self-balancing at high levels [19].

The conventional T-type active clamp DC-AC inverter uses fewer components than the flying capacitor and the diode clamped DC-AC converters, and the voltage stress on the switch is lower than the input voltage. In addition, complex control signals are not required to balance the capacitor voltage. However, this structure requires two capacitors

to build up the neutral point voltage and a bidirectional switch to connect the neutral point to the load, leading to only a 3-level step-down output voltage.

1.2. State of the Related Works

There are many other existing papers presented for the T-type single-phase MLIs [20–25] with a different number of levels, voltage gain and circuit structure considered. Those characteristics are summarized in Table 1. In study [20], two structures are presented by combining a T-type active clamp DC-AC inverter with multiple DC power sources. The first structure uses three DC voltage sources and ten switches to achieve a 15-level AC output with a voltage gain of 1, while the second structure uses four DC power sources and twelve switches to achieve a 25-level AC output with a voltage gain of 1. In studies [21–23], two T-type active clamp DC-AC inverters are used to form the circuit structure. In study [21], the input capacitance of the second T-type active clamp DC-AC inverter is changed to the power source voltage, and a 7-level step-up T-type DC-AC inverter having a voltage gain of 1.5 is implemented with ten switches and four capacitors. In study [22], only one capacitor is employed to boost the voltage, an inductor is utilized at the front end of the capacitor to form a buck-boost converter, and a duty cycle of 0.5 is adopted to convert the voltage on the capacitor to the power source voltage to achieve a 5-level AC output with a voltage gain of 2. The circuit structure shown in [23] takes four power inputs cross-connected to obtain two T-type actively clamped DC-AC inverters to achieve a 9-level AC output with a voltage gain of 1. However, compared with studies [21,22], the input power source is increased from a single power source to four power sources, but the 7- and 5-level DC-AC inverters in [21,22], respectively, are upgraded to the 9-level ones. In studies [24,25], 7-level DC-AC inverters are presented, formed by combining the T-type active clamp DC-AC inverter with the H-bridge. In study [24], eight switches and one floating capacitor are used to form a 7-level DC-AC inverter possessing a voltage gain of 0.75, and the space vector modulation is used to maintain the floating capacitor across the H-bridge at half of the DC input voltage. Compared with study [18], the literature [19] adds two switches to achieve a 7-level AC output with a voltage gain of 1.5.

Table 1. T-type single-phase MLIs.

Reference Number	Level Number	Voltage Gain	Circuit Structure
[20]	15	1.0	T-Type + Active Clamped
[21]	7	1.5	Asymmetric Two T-type Active Clamped
[22]	5	2.0	Two T-type Active Clamped+ Front-End Buck-Boost Converter
[23]	9	1.0	Two T-type Active Clamped+ Four Power Inputs
[24]	7	0.75	T-type + Diode Clamped+ Floating Capacitor
[25]	7	1.5	T-type + Diode Clamped+ H-bridge Switched-Capacitor

On the other hand, in order to control the power converter, modeling is very important, although there are, of course, numerous variations in analysis and measure from a theoretical and implement point of view, respectively [26]. There are many methods which were proposed for modeling the DC-DC converter, for example, the well-known state-space averaging method. However, very few examples of modeling the multilevel DC-AC inverter can be found in the literature.

1.3. Contributions

Contributions of this paper are as follows: (1) A novel T-type 7-level single-phase DC-AC inverter with a single input power source, self-balancing, voltage gain of 3 and low total THD is proposed, which is different from [27] based on class-D. (2) The mathematical model of the DC-AC inverter is successfully developed by using the well-known state-space averaging method widely used in the DC-DC converter. (3) A 300 W prototype circuit

is simulated to demonstrate the feasibility of the proposed circuit, and one-comparator voltage control [28], accordingly to the field programmable gate array (FPGA), which is utilized to verify the effectiveness of the proposed circuit. The proposed T-type 7-level DC-AC inverter not only has a rather fast load transient response due to the well-designed feedback controller, but also has the efficiency up to 97.42% and the THD down to 2.01%.

The contents of the paper may be outlined as follows. Section 2 illustrates the proposed MLI, including circuit description, switching patterns, and operating principle. Power component design is given in Section 3. Modeling and controller design is introduced for the level-shift sinusoidal pulse width modulation (LS-SPWM) in Section 4. Simulated and experimental results, along with discussions, are shown in Section 5. Finally, some conclusions are made in the last section.

2. Proposed Inverter

Figure 2a shows the proposed single-power-source T-type 7-level single-phase DC-AC inverter.

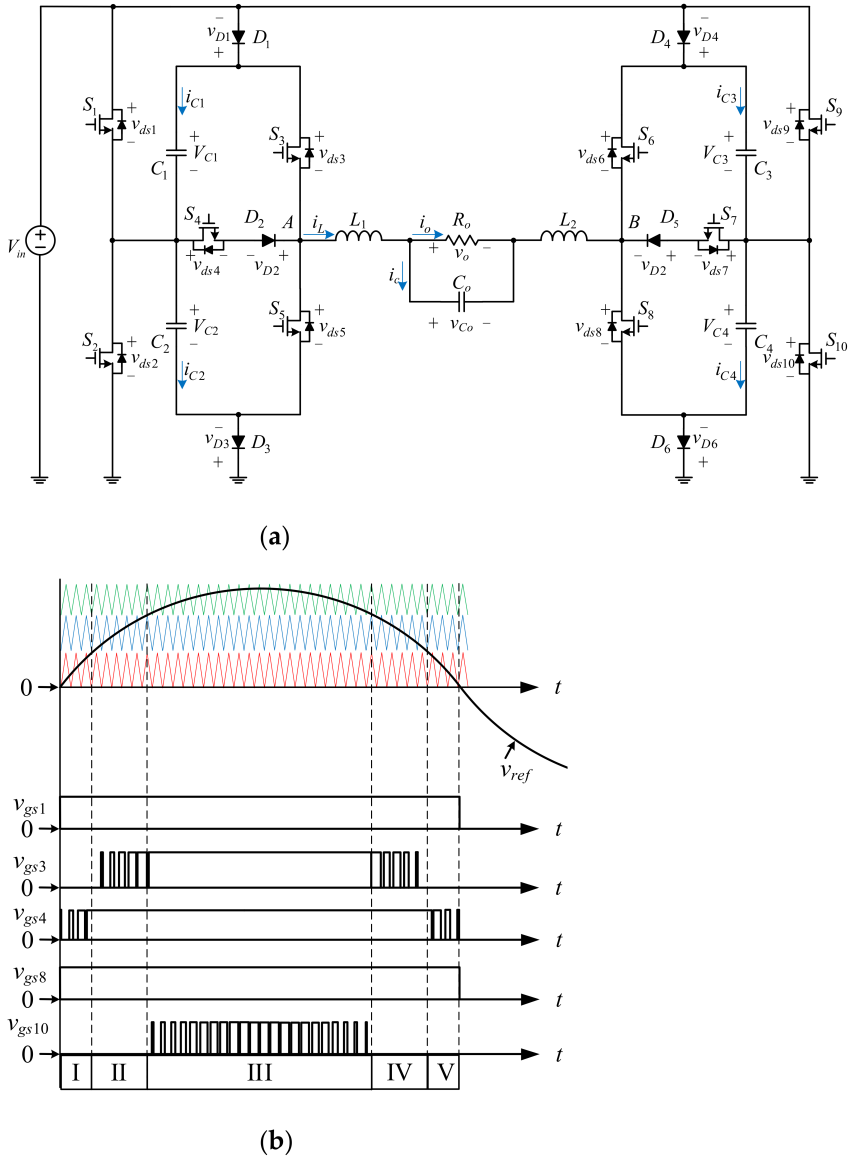


Figure 2. Proposed inverter and PWM control strategy: (**a**) Single-power-source T-type 7-level single-phase DC-AC inverter; (**b**) Gate signals of the switches.

2.1. Operating Principle

Prior to the operation analysis, we will briefly explain the definition of the symbols and the assumptions required.

(1) the input voltage is signified by V_{in}, the output voltage is denoted by v_o, and the voltage across the output capacitor C_o, V_{Co}, is identical to v_o.
(2) the voltages on S_1 to S_{10} are represented by v_{ds1} to v_{ds10}, respectively.
(3) the voltages on D_1 to D_6 are expressed by V_{D1} to V_{D6}, respectively.
(4) the currents in the energy-transferring capacitors C_1 to C_4 are denoted by i_{C1} to i_{C4}, respectively.
(5) It is assumed that the energy-transferring capacitances are large enough such that the voltages on the capacitors can be viewed as constant, i.e., $V_{C1} = V_{C2} = V_{C3} = V_{C4}$.
(6) the output current is signified by i_o, and the currents flowing through inductors L_1 and L_2 are expressed by i_L.
(7) All elements, except the body diodes of the switches, are considered as ideal.

Figure 2b displays the gate signals for the switches with level-shift sinusoidal pulse width modulation (LS-SPWM). As the gate signals at the positive half-cycle which are identical to those at the negative half-cycle, only the positive half-cycle is taken into consideration. There are five stages in circuit operation, and only one switch in each stage over one PWM switching cycle, while the rest of the switches are always on or off. Since stage I is identical to stage V and stage II is identical to stage IV, only stages I, II, and III are analyzed.

As the AC output voltage is at the positive half-cycle, the switches S_1 and S_8 are always in the on-state and the switches S_2, S_5, S_6, S_7, and S_9 are always in the off-state. The output voltage will be obtained by switching S_4, S_3, and S_{10} to comply with the circuit operations of stages I, II, and III, respectively. To speak lucidly, all the three triangular waves are compared with the sinusoidal wave. If the latter is larger than the former, the turn-on times are generated. The red line is for v_{gs4}, the blue line is for v_{gs3}, and the green line is for v_{gs10}.

2.1.1. Stage I

Only S_4 is turned on/off as in Figure 3.

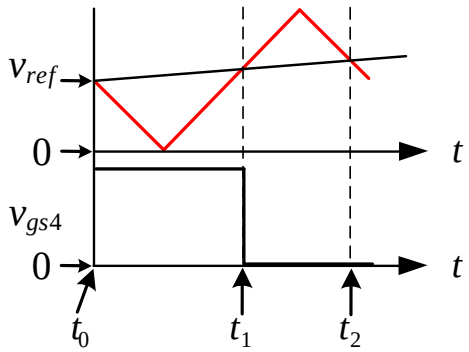


Figure 3. Gate signal of S_4.

Time interval $[t_0 \leq t \leq t_1]$: As illustrated in Figures 2b and 3, the switch S_4 is on, but the switches S_3 and S_{10} are off. As displayed in Figure 4, the power flow via the inductors L_1 and L_2 will generate a loop from the input voltage V_{in} to the switches S_1, S_4, S_8 and the diodes D_2, D_6. Hence, the voltage across the terminals A and B, called v_{AB}, is:

$$v_{AB} = V_{in} \tag{1}$$

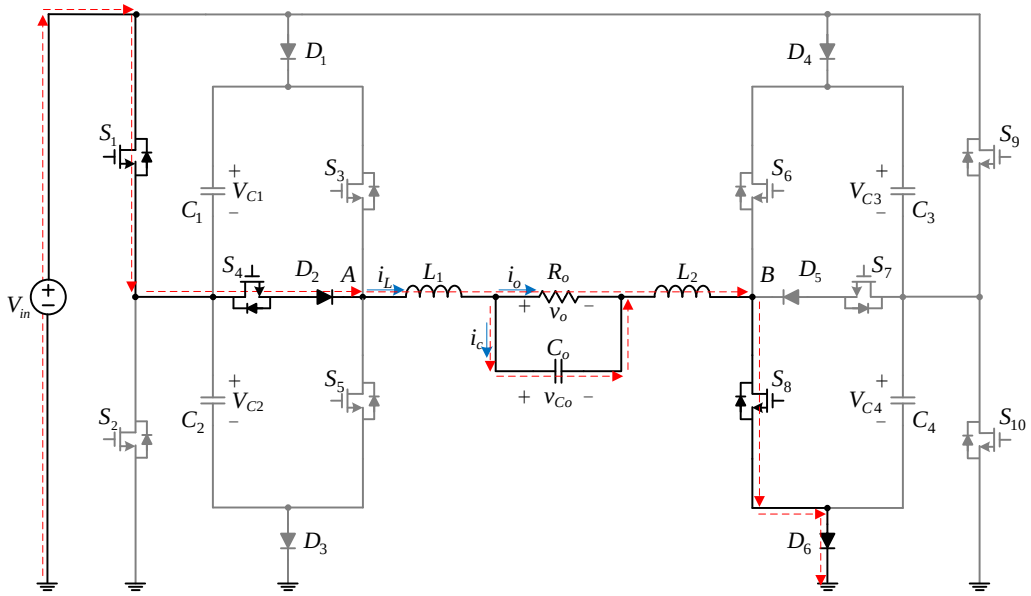


Figure 4. Power flow as S_4 is conducted.

Time interval $[t_1 \leq t \leq t_2]$: As illustrated in Figures 2b and 3, the switches S_3, S_4, and S_{10} are all off. As displayed in Figure 5, the power flow via the inductors L_1 and L_2 will generate a loop from the switches S_1, S_8, the diode D_6, and the body diode of the switch S_5. Hence, the voltage on the terminals A and B, named v_{AB}, is:

$$v_{AB} = V_{in} - V_{C1} = 0 \quad (2)$$

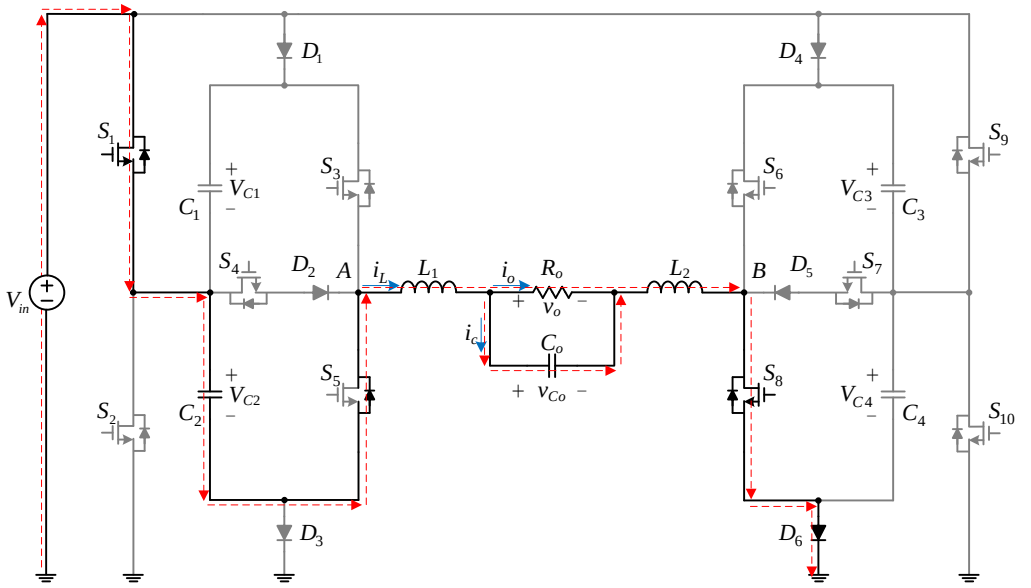


Figure 5. Power flow as S_4 is cut off.

2.1.2. Stage II

Only S_3 is turned on/off as in Figure 6.

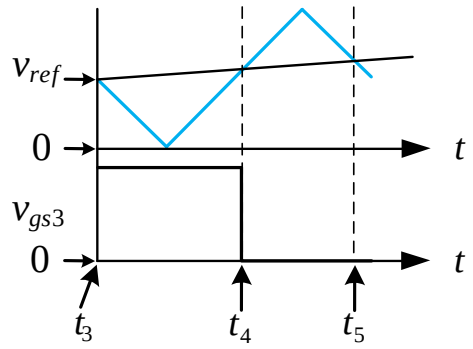


Figure 6. Gate signal of S_3.

Time interval $[t_3 \leq t \leq t_4]$: As illustrated in Figures 2b and 6, the switch S_3 is on, but the switches S_4 and S_{10} are off. Although the switch S_4 is always in the on-state during this interval, the diode D_2 is reverse biased so that no current passes through S_4, which can be considered as equal to being in the off-state. As displayed in Figure 7, the power flow via the inductors L_1 and L_2 will generate a loop from the input voltage V_{in} to the switches S_1, S_3, S_8, and the diode D_6. Hence, the voltage on the terminals of A and B, called v_{AB}, is:

$$v_{AB} = V_{in} + V_{C1} = 2V_{in} \tag{3}$$

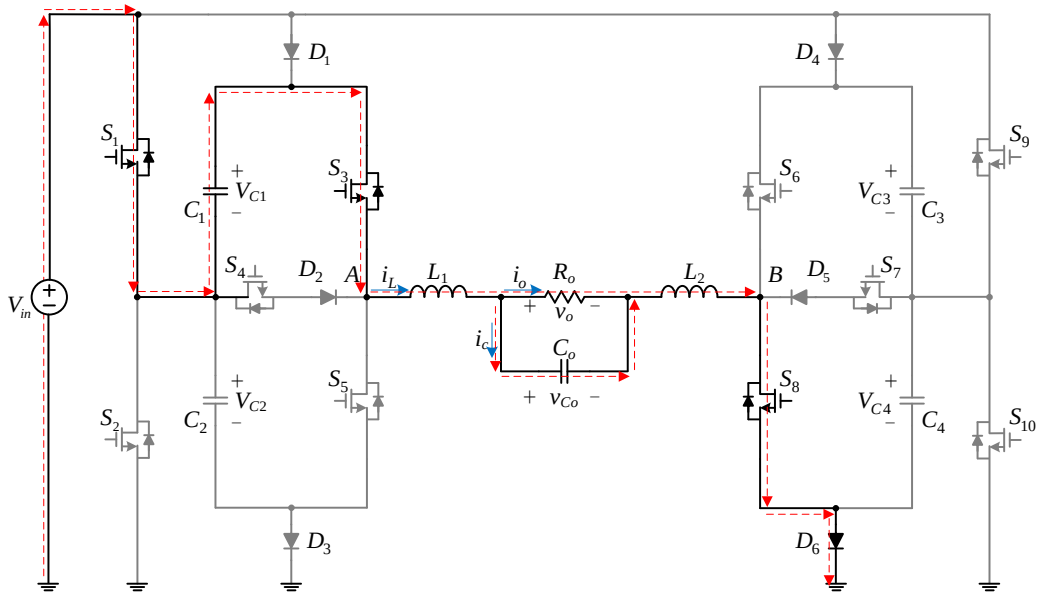


Figure 7. Power flow as S_3 is conducted.

Time interval $[t_4 \leq t \leq t_5]$: As illustrated in Figures 2b and 6, the switches S_3 and S_{10} are off, but the switch S_4 is on. The power flow in this interval is the same as Figure 4. The power flow via the inductors L_1 and L_2 will generate a loop from the input voltage V_{in} to the switches S_1, S_4, S_8, and the diodes D_2 and D_6. Hence, the voltage on the terminals A and B, named v_{AB}, is V_{in} as shown in Equation (1).

2.1.3. Stage III

Only S_{10} is turned on/off as in Figure 8.

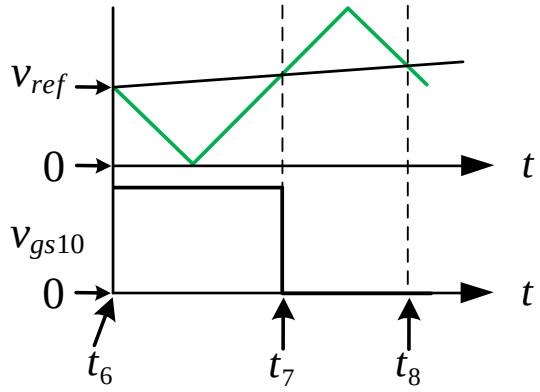


Figure 8. Gate signal of S_{10}.

Time interval $[t_6 \leq t \leq t_7]$: As illustrated in Figures 2b and 8, the switches S_3 and S_{10} are on, but the switch S_4 is off. As displayed in Figure 9, the current flow via the inductors L_1 and L_2 will generate a loop from the input voltage V_{in} to the switches S_1, S_3, S_8, and S_{10}. Hence, the voltage on the terminals of A and B, called v_{AB}, is:

$$v_{AB} = V_{in} + V_{C1} + V_{C4} = 3V_{in} \tag{4}$$

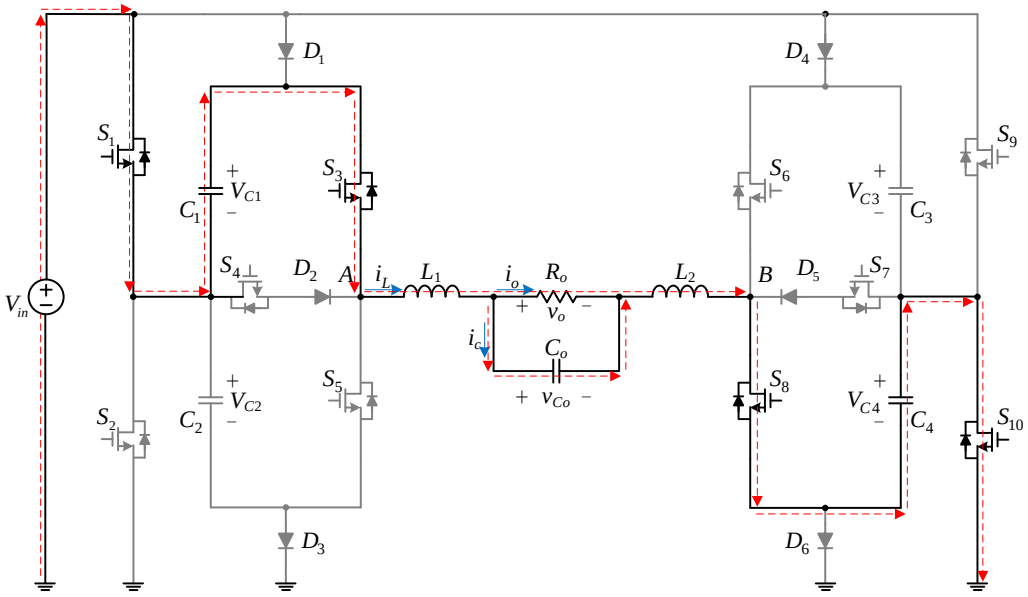


Figure 9. Power flow as S_{10} is conducted.

Time interval $[t_7 \leq t \leq t_8]$: As illustrated in Figures 2b and 8, the switches S_4 and S_{10} are cut off, but the switch S_3 is on. The power flow in this interval is the same as Figure 7. The power flow via the inductors L_1 and L_2 will generate a loop from the input voltage V_{in} to the switches S_1, S_3, S_8, and the diode D_6. Hence, the voltage on the terminals A and B, named v_{AB}, is $2V_{in}$ as shown in Equation (3).

According to the analysis mentioned above, the proposed 7-level DC-AC inverter possesses the voltage gain of 3, to be calculated based on (5):

$$\text{Voltage gain} = \frac{\text{Amplitude of AC output voltage}}{\text{Sum of input voltages}} \tag{5}$$

2.2. Switch Behavior and Maximum Voltage Stress

Table 2 displays the switch behavior of the proposed circuit and the corresponding maximum voltage stresses of switches, where f_{line} is the mains frequency and f_{PWM} is the switching frequency. Since the positive half-cycle is considered, the switches S_2, S_5, S_6, S_7, and S_9 are kept off. The maximum voltage stress is V_{in} for all switches except for the switches S_3 and S_5, whose voltage stresses both are $2V_{in}$.

Table 2. Switch behavior of the proposed circuit and the corresponding maximum voltage stresses of switches at the positive half-cycle.

		S_1	S_3	S_4	S_8	S_{10}
Switch Frequency		f_{line}	f_{pwm}	f_{pwm}	f_{line}	f_{pwm}
Stage I (S_4 PWM)	Switch status	1	0	1, 0	1	0
	Maximum voltage stress	0	$2V_{in}$	V_{in}	0	V_{in}
Stage II (S_3 PWM)	Switch status	1	1,0	1 (no power flow)	1	0
	Maximum voltage stress	0	V_{in}	0	0	V_{in}
Stage III (S_{10} PWM)	Switch status	1	1	1	1	1,0
	Maximum voltage stress	0	0	0	0	V_{in}

Note: '1' implies 'on' and '0' implies 'off'.

3. Power Component Design

The specifications for the proposed DC-AC inverter are shown in Table 3.

Table 3. Specifications for the proposed DC-AC inverter.

Specification	Value
Input Voltage V_{in}	56 V
Output Voltage (Mains) Frequency f_{line}	60 Hz
Output Voltage v_o	110 V_{rms}
Rated Output Power $P_{o,rated}$/Rated Outout Current $I_{o,rated}$	300 W/2.72 A_{rms}
Minimum Output Power $P_{o,min}$	75 W
Switching Frequency f_s	60 kHz

3.1. Energy-Transferring Capacitor Design

The PSIM simulation results can be used to get the charge of two energy-transferring capacitors discharged at the positive half-cycle of the mains. By setting the voltage ripple rate at 10%, the capacitance can be obtained as below:

$$\Delta V = 56 \times 10\% = 5.6 \text{ V} \tag{6}$$

$$C_1 = C_3 = \frac{\Delta Q_1}{\Delta V} = \frac{17.48 \text{ m}}{5.6} = 3.12 \text{ mF} \tag{7}$$

$$C_4 = C_2 = \frac{\Delta Q_4}{\Delta V} = \frac{8.26 \text{ m}}{5.6} = 1.47 \text{ mF} \tag{8}$$

Consequently, for design convenience, a 3.3 mF electrolytic capacitor is used for each of the four energy-transferring capacitors, and the voltage across each capacitor is identical to the input voltage according to Section 2.1. Since the derating should be considered in

use of the electrolytic capacitor, the voltage rating of the selected capacitor, based on thumb theorem, should be at least 1.25 times of the input voltage V_{in}, namely:

$$V_C \geq 56 \times 1.25 = 70 \text{ V} \tag{9}$$

Eventually, the specifications of the selected capacitors are shown in Table 4.

Table 4. Specifications for four energy-transferring capacitors.

Product Name	Rubycon
Rted Voltage	100 V
Capacitance	3300 μF

3.2. Filter Design

The maximum total harmonic distortion is 5% under 69 kV or less [29], according to the harmonic voltage limit proposed by IEEE 519–1992. Since a multilevel DC-AC converter is operated at high frequencies, the output voltage contains high frequency components, leading to a total harmonic distortion greater than 5%. Consequently, a filter should be adopted to reduce the total harmonic distortion of the output voltage.

Since the proposed circuit has a double-ended symmetrical output, the inductance L of LC filter as shown in Figure 10a is divided into L_1 and L_2 as shown in Figure 10b, not only rendering the differential-mode (DM) noise to not exist at the output terminals, but also keeping the common-mode noise (CM) from influencing the operation of the circuit. Accordingly, L_1 is connected with L_2 in series as displayed in Figure 10b so let L be equal to the sum of L_1 and L_2 to do analysis and calculation, i.e., $L = L_1 + L_2$, where $L_1 = L_2 = 0.5L$.

High frequency switching is used to reduce the size of the filter, and the cut-off frequency f_c of the filter is designed at 0.1 times the switching frequency f_s to ensure that the fundamental and harmonics of the switching frequency can be filtered out by this filter. Since the switching frequency is prescribed at 60 kHz, the value of f_c is prescribed at 6 kHz.

The transfer function of the filter, called $F(s)$, is indicated in Equation (10) as follows:

$$F(s) = \frac{\frac{1}{C_o L}}{s^2 + s\frac{1}{R_o C_o} + \frac{1}{C_o L}} \tag{10}$$

In Equation (10), we can find the expressions of the cut-off frequency f_c and the quality factor Q as below:

$$f_c = \frac{1}{2\pi}\sqrt{\frac{1}{C_o L}} \tag{11}$$

and:

$$Q = \sqrt{\frac{C_o}{L}} R_o \tag{12}$$

Substituting the value of f_c into Equation (11) yields:

$$C_o L = \left(\frac{1}{2\pi \times f_c}\right)^2 = \left(\frac{1}{2\pi \times 6\text{ k}}\right)^2 = 0.7 \text{ n } (\text{s}^2/\text{rad}^2) \tag{13}$$

At the same time, rearranging Equation (12) yields:

$$\frac{C_o}{L} = \left(\frac{Q}{R_o}\right)^2 \tag{14}$$

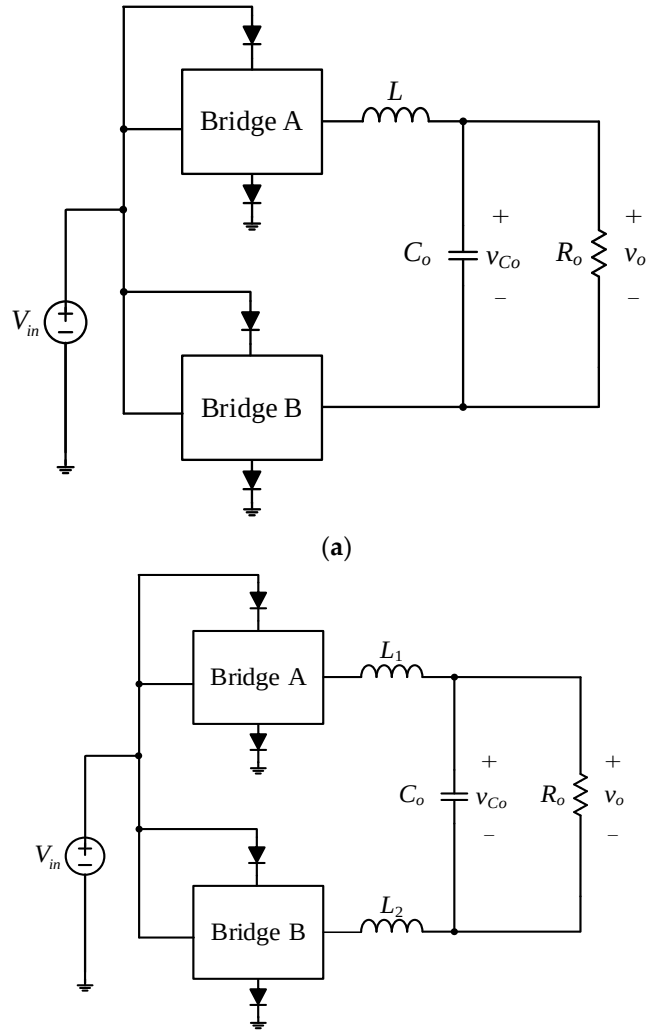


Figure 10. Filter circuit diagram from the point of view of the output load with the inductance of (**a**) L; (**b**) L_1 and L_2.

The value of Q at full load is set to 3 dB, that is $\sqrt{2}$, and substituting this value into Equation (14) yields:

$$\frac{C_o}{L} = \left(\frac{\sqrt{2}}{39.24}\right)^2 = 1.3\ \text{m}^2 \Rightarrow\ C_o = L \times 1.3\ \text{m} \tag{15}$$

Substituting Equation (15) into Equation (13) yields:

$$L = \sqrt{\frac{0.7\ \text{n}}{1.3\ \text{m}}} = 734\ \mu\text{H} \tag{16}$$

Substituting Equation (16) into Equation (15) yields:

$$C_o = 954\ \text{nF} \tag{17}$$

One 1 μF/275 V metal film capacitor, manufactured by HJC Co., is selected as C_o. Therefore, the value of the individual values of L_1 and L_2 can be chosen to be:

$$L_1 = L_2 = 0.5L = 367\ \mu\text{H} \tag{18}$$

Eventually, the individual values of L_1 and L_2 are selected as 367 μH.

Two low permeability cores are selected for cores of L_1 and L_2 along with the following parameters shown in Table 5.

Table 5. Specifications for the used cores.

Ring Core	T106–26
Outside Diameter (*OD*)	26.9 mm
Inner Diameter (*ID*)	14.5 mm
Thickness (*HT*)	14.6 mm
Relative Permeability (μ_r)	75
Inductance Coefficient (A_L)	124 ± 10% (nH/N^2)
Effective Area (A_e)	0.858 cm^2
Effective Magnetic Length (l_e)	6.49 cm
Effective Volume (V_e)	5.57 cm^3

Since the inductors L_1 and L_2 are the same, whose values are 367 μH, the required number of turns N, wound on the T106-26 core, is:

$$\begin{aligned} &L = N^2 \times A_L \\ &\Rightarrow N = \sqrt{\frac{L_1}{A_L}} = \sqrt{\frac{L_2}{A_L}} = \sqrt{\frac{367}{124\times10^{-3}}} = 54.4\text{Turns} \end{aligned} \tag{19}$$

Eventually, each inductance is 375 μH with 55 turns.

On the other hand, the current density J_f is designed to be 400 A/cm^2, and by considering the skin effect and using a wire diameter Φ_f of 0.5 mm, the required number of strands is:

$$N_{L,turn} = \frac{I_{o,rated}}{\pi(\frac{\Phi_f}{2})^2 \times J_f(\text{A/mm}^2)} = \frac{2.72}{\pi \times (\frac{0.5}{2})^2 \times 400 \times 0.01} = 3.46 \tag{20}$$

According to the result of Equation (20), 4 wires of 0.5 mm diameter enameled wire are wound on the used cores to obtain the filter inductors L_1 and L_2.

In addition, the product name for S_1, S_2, S_4, S_7, S_9, and S_{10} is AP75T45GP-HF, while the product name for S_3, S_5, S_6, and S_8 is IPP076N15N5. The product name for D_1 to D_6 is SBR20A100CTFP.

4. Modeling and Controller Design

4.1. Modeling

4.1.1. Small-Signal Analysis of Stage I

The state-space equations of the circuit are shown in Equation (21) and Equation (22) as the switch S_4 is turned on and off, respectively, during stage I:

$$\begin{cases} L\frac{di_L}{dt} = v_{in} - v_o \\ C_o\frac{dv_o}{dt} = i_L - \frac{v_o}{R_o} \end{cases} \tag{21}$$

$$\begin{cases} L\frac{di_L}{dt} = 0 - v_o \\ C_o\frac{dv_o}{dt} = i_L - \frac{v_o}{R_o} \end{cases} \tag{22}$$

Based on the state-space averaging method [26], it is assumed that the switch S_4 is on during the period of dT_s and the switch S_4 is off during the period of $(1-d)T_s$, where d is duty cycle and T_s is the switching period. After this, by multiplying Equation (21) by dT_s

and Equation (22) by $(1-d)T_s$, the state-space averaging equations of stage I, via summing these two corresponding results, can be obtained to be:

$$\begin{cases} L\frac{di_L}{dt} = d \times v_{in} - v_o \\ C_o\frac{dv_o}{dt} = i_L - \frac{v_o}{R_o} \end{cases} \tag{23}$$

Since each parameter of the converter contains a DC quiescent operating point and an AC small signal, we can express the corresponding parameters as shown in Equation (24):

$$\begin{cases} d = D + \hat{d} & D >> \hat{d} \\ v_{in} = V_{in} + \hat{v}_{in} & V_{in} >> \hat{v}_{in} \\ i_L = I_L + \hat{i}_L & I_L >> \hat{i}_L \\ v_o = V_o + \hat{v}_o & V_o >> \hat{v}_o \end{cases} \tag{24}$$

Substituting Equation (24) into Equation (23) yields the small-signal AC model equation:

$$\begin{cases} L\frac{d\hat{i}_L}{dt} = (\hat{d}V_{in} + D\hat{v}_{in}) - \hat{v}_o \\ C_o\frac{d\hat{v}_o}{dt} = \hat{i}_L - \frac{\hat{v}_o}{R_o} \end{cases} \tag{25}$$

4.1.2. Small-Signal Analysis of Stage II

The state-space equations of the circuit are shown in Equation (26) and Equation (21) as the switch S_3 is turned on and off, respectively, during stage II:

$$\begin{cases} L\frac{di_L}{dt} = v_{in} + v_{C1} - v_o = 2v_{in} - v_o \\ C_o\frac{dv_o}{dt} = i_L - \frac{v_o}{R_o} \end{cases} \tag{26}$$

where according to the analysis in Section 2, the voltage across the energy-transferring capacitor C_1 is treated as the input voltage, i.e., $v_{C1} = v_{in}$.

Sequentially, it is assumed that the switch S_3 is on during the period of dT_s and the switch S_3 is off during the period of $(1-d)T_s$. Afterwards, by multiplying Equation (26) by dT_s and (21) by $(1-d)T_s$, the state-space averaging equations of stage II, via summing these two corresponding results, can be obtained to be:

$$\begin{cases} L\frac{di_L}{dt} = v_{in} + d \cdot v_{in} - v_o \\ C_o\frac{dv_o}{dt} = i_L - \frac{v_o}{R_o} \end{cases} \tag{27}$$

Substituting Equation (24) into Equation (27) yields the small-signal AC model equation, which is the same as Equation (25).

4.1.3. Small-Signal Analysis of Stage III

The state-space equations of the circuit are shown in Equation (28) and Equation (26) as the switch S_{10} is turned on and off, respectively, during stage III:

$$\begin{cases} L\frac{di_L}{dt} = v_{in} + v_{C1} + v_{C4} - v_o = 3v_{in} - v_o \\ C_o\frac{dv_o}{dt} = i_L - \frac{v_o}{R_o} \end{cases} \tag{28}$$

where according to the analysis in Section 2, the voltage across the energy-transferring capacitors C_1 and C_4 are treated as the input voltage, i.e., $v_{C1} = v_{C4} = v_{in}$.

Sequentially, it is assumed that the switch S_{10} is on during the period of dT_s and the switch S_{10} is off during the period of $(1-d)T_s$. After this, by multiplying Equation (28)

by dT_s and Equation (26) by $(1-d)T_s$, the state-space averaging equations of stage III, via summing these two corresponding results, can be obtained to be:

$$\begin{cases} L\frac{di_L}{dt} = 2v_{in} + dv_{in} - v_o \\ C_o\frac{dv_o}{dt} = i_L - \frac{v_o}{R_o} \end{cases} \tag{29}$$

Substituting Equation (24) into Equation (29) yields the small-signal AC equation, which is the same as Equation (25).

From above analysis, it can be seen that the small-signal ac model of the proposed inverter is the same for any stage, and it is shown in Figure 11. From this figure, it can be seen that the small-signal AC model of the proposed inverter is the same as that of the conventional DC-DC buck converter. As a result, the control design can be carried out easily and systematically.

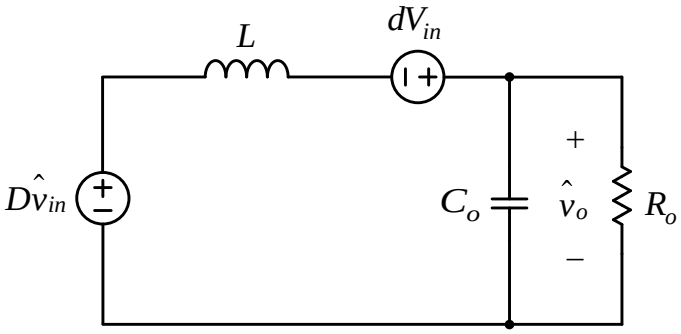


Figure 11. Small-signal AC model of the proposed inverter.

4.2. Controller Design

First, taking the Laplace transform of the circuit shown in Figure 11 yields the control-force-to-output-voltage transfer function $G_{vd}(s)$:

$$G_{vd}(s) = \frac{\hat{v}_o(s)}{\hat{d}(s)} = \frac{V_{in}}{s^2LC_o + s\frac{L}{R_o} + 1} \tag{30}$$

Accordingly, the system block diagram for voltage feedback control of the proposed circuit can be obtained as shown in Figure 12, where $G_c(s)$ represents the controller transfer function, V_M denotes the peak-to-peak triangular wave transfer function, and $H(s)$ signifies the voltage divider transfer function. The loop gain $T(s)$ is equal to $G_c(s) \cdot G_{vd}(s) \cdot H(s)/V_M$.

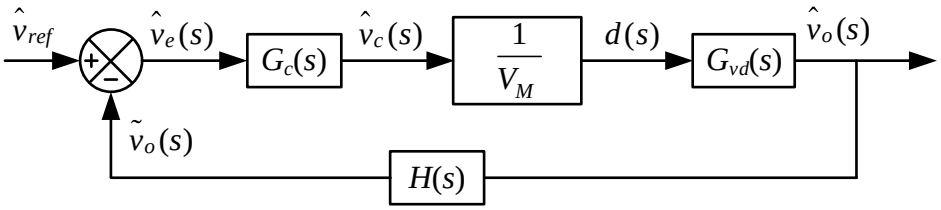


Figure 12. System block diagram for voltage feedback control of the proposed circuit.

First, let $G_c(s) = 1$ and $s = j\omega$, the phase angle at the crossover radian frequency ω_{cr} is calculated by MATLAB to be approximately -151°, and based on the radian frequency compensation parameter table as described in [30] and the designed values of components as shown in Section 3, $T(j\omega_{cr})$ can be obtained to be:

$$T(j\omega_{cr}) = T(j0.8) = 0.9064\angle -151.6^\circ \tag{31}$$

In general, the general system stability condition is set at the compensation phase between 45° and 60°, so the compensation phase is set at 55° to calculate the required angle θ after compensation as follows:

$$\theta = -180^{\circ} + 55^{\circ} - (-151.6^{\circ}) = 26.6^{\circ} \tag{32}$$

Substituting the phase calculated by Equation (32) into the formula of the proportional gain k_p shown in Equation (33) and the integral gain k_i shown in Equation (34) to find their corresponding values as below:

$$k_p = \frac{\cos\theta}{|T(j\omega_{cr})|} = \frac{\cos(26.6^{\circ})}{0.9064} = 0.986 \tag{33}$$

$$k_i = \frac{\sin\theta}{|T(j\omega_{cr})|} = \frac{\sin(26.6^{\circ})}{0.9064} = 0.493 \tag{34}$$

Figure 13 shows the control flow chart. The signal v_{sense} is after no analog-to-digital converter (ADC) sampling so it is a digital value. This value is positive and is subtracted from the reference value v_{ref} to get *VFB*, which is a positive/negative number. Afterwards, set the variable *Error* to store the current error value and multiply it by the coefficient k_p to get the proportional control force *P*. At the same time, set the variable *accum* to store the cumulative value, and each operation will add the previous error value to this operation, then multiply this variable by the coefficient k_i to get the integral control force *I*. Finally, add *P*, *I*, and the digital sine wave signal, called *sinewave_data*, to get the control force, called *Force*, which is restricted by a limiter, called *Duty Limiter*, between −1023 and 1023.

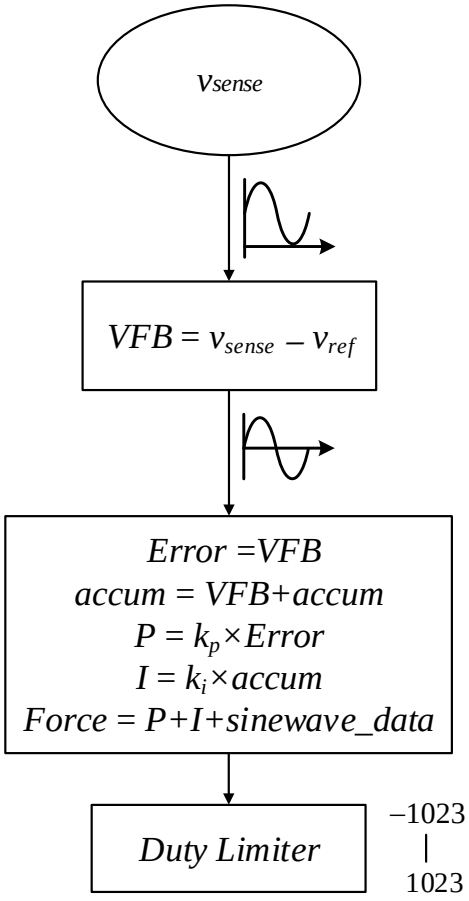


Figure 13. Control flow chart.

5. Results and Discussion

5.1. System Configuration

Figure 14 shows the system configuration for the proposed 7-level single-phase DC-AC inverter. This system is built up by the main circuit and the feedback circuit. The field-programmable gate array (FPGA) and digital-to-analog converter (DAC) are used to create sinusoidal voltage reference signal v_{ref}, and no ADC sampling circuit is used to transmit the feedback signal v_{FB} to the FPGA to get the resulting control effort after calculation. This control effort is then sent to the isolated gate driver to make the switch on/off to achieve a desired output voltage.

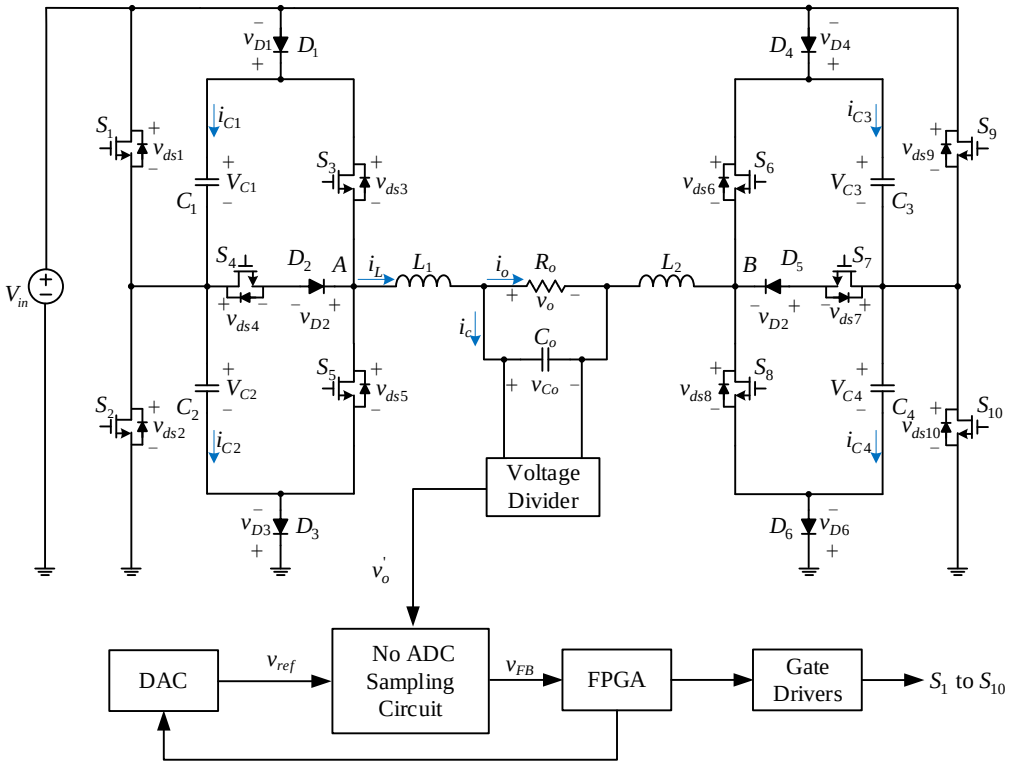


Figure 14. System configuration for the 7-level single-phase DC-AC inverter.

5.2. Simulation and Experiment with Discussion

Under closed loop at rated load, Figure 15 shows the output voltage v_o and current i_o. Figure 16 displays the output voltage v_o and the unfiltered output voltage v_{PWM}. Figures 17 and 18 show the voltages on the energy-transferring capacitors C_1, C_2, C_3, and C_4. Figure 19 only shows the voltage stresses on the switches S_1 to S_5 due to the circuit symmetry. Figures 20 and 21 display the upload and download transient responses based on load variations from 25% to 100% load and from 100% to 25% load, respectively.

From Figure 15, it can be seen that the output voltage v_o and output current i_o are both AC outputs. From Figure 16, it can be seen that the unfiltered output voltage v_{PWM} possesses 7 levels generated by the gate signal with high switching frequency to conduct and cut off the switch and is filtered to get 60 Hz AC voltage with voltage gain of 3. As can be seen from Figures 17 and 18, the energy-transferring capacitors possess self-balancing. From Figure 19, it can be seen that all switches have voltage stresses of the input voltage except the switches S_3 and S_5, whose voltage stresses are double the input voltage. From Figures 20 and 21, it can be seen that the former has an undershoot voltage of about 50 V and a recovery time of about 0.6 ms, and the latter has an overshoot voltage of about 45 V and a recovery time of about 1.5 ms. From the above simulated and measured results, it is obvious that good agreement between the simulated and experimental results validates the

feasibility and effectiveness of the proposed single-power-source T-type 7-level single-phase DC-AC inverter.

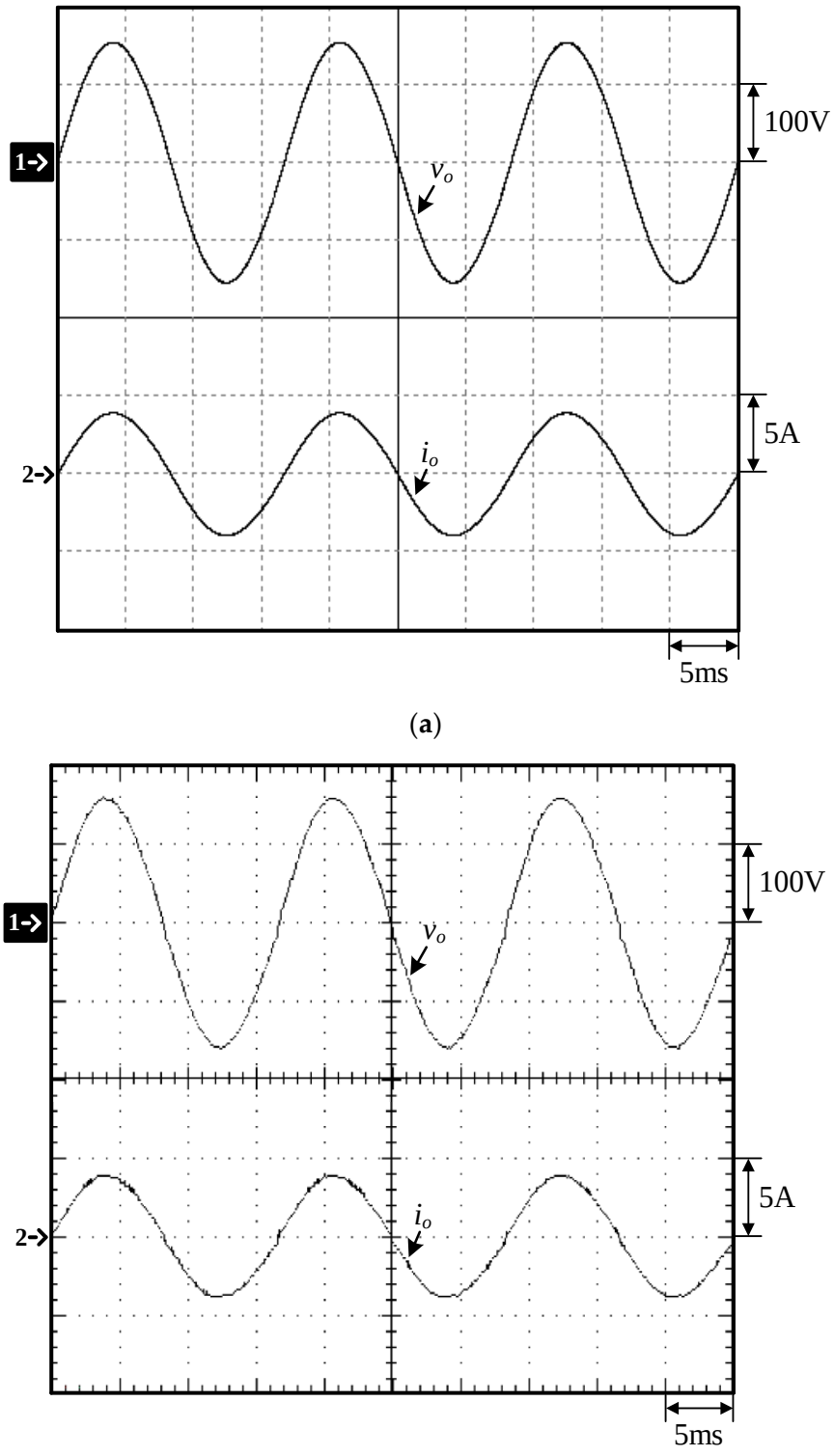
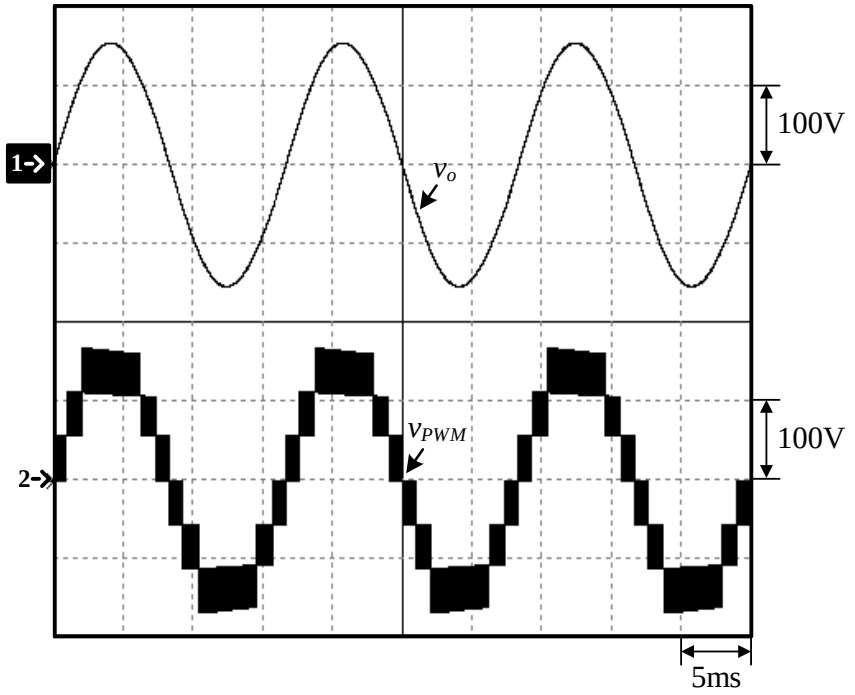
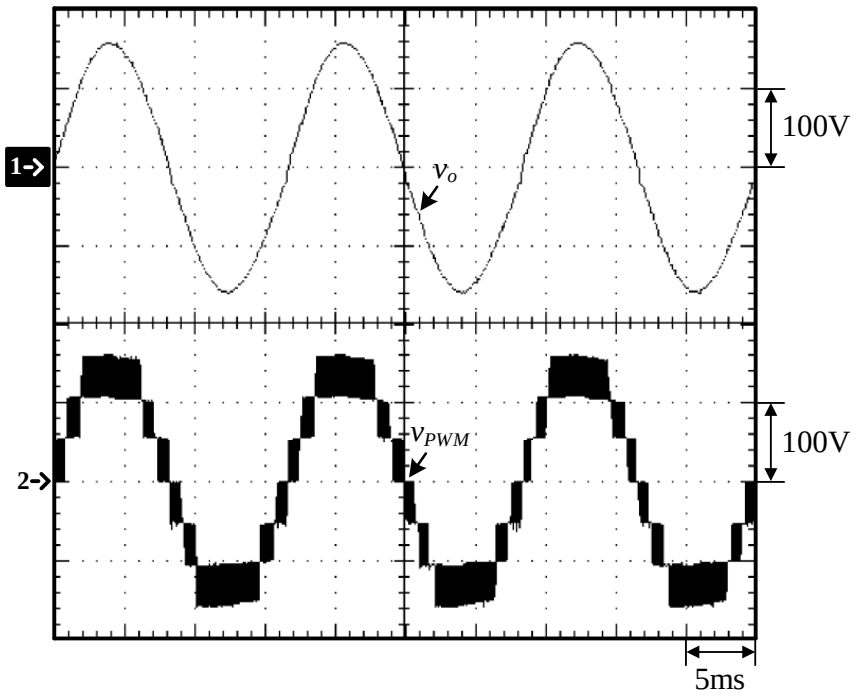


Figure 15. Waveforms at rated load with (1) v_o and (2) i_o: (**a**) simulated; (**b**) measured.

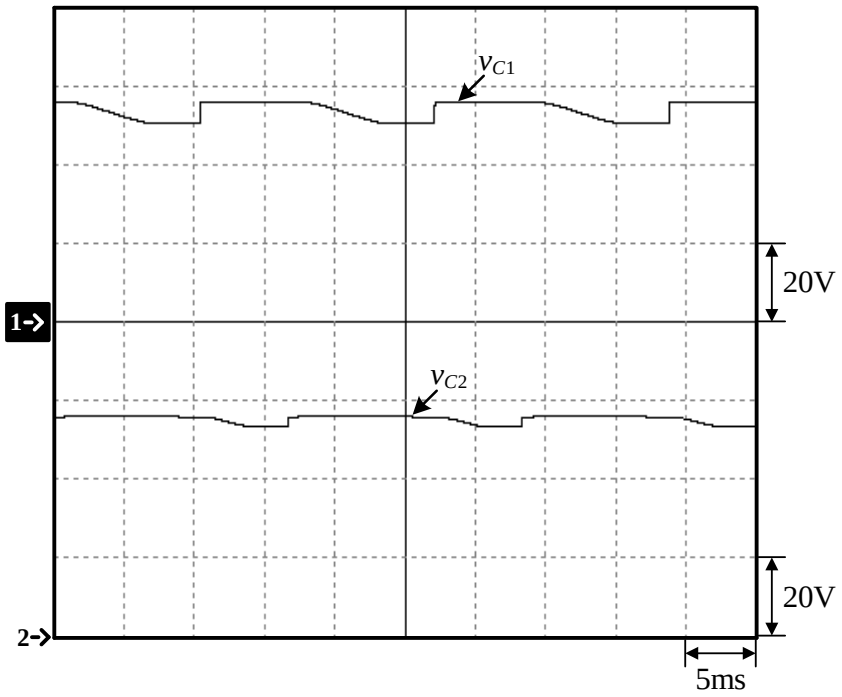


(**a**)

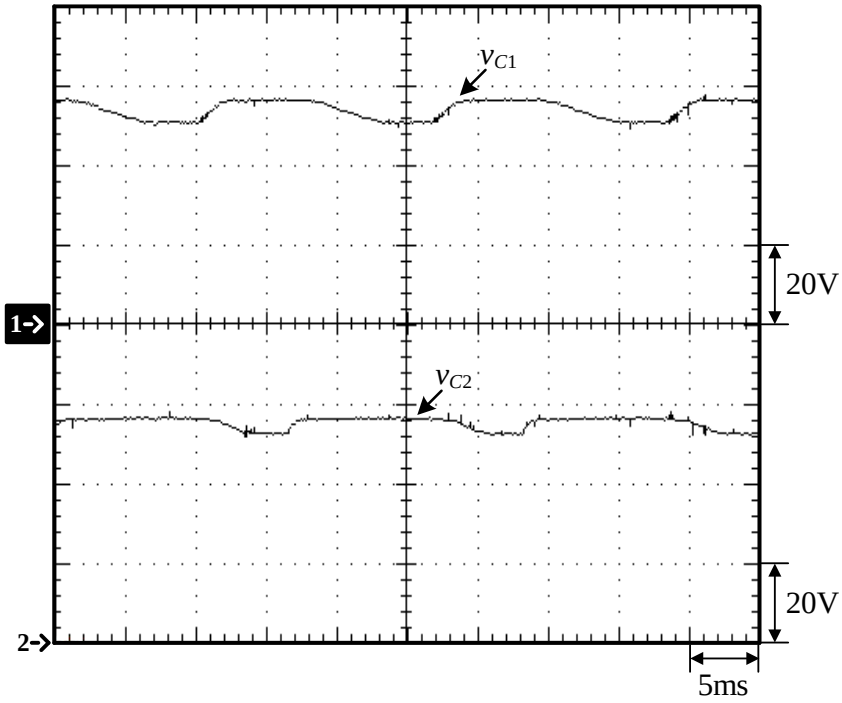


(**b**)

Figure 16. Waveforms at rated load with (1) v_o and (2) v_{PWM}: (**a**) simulated; (**b**) measured.

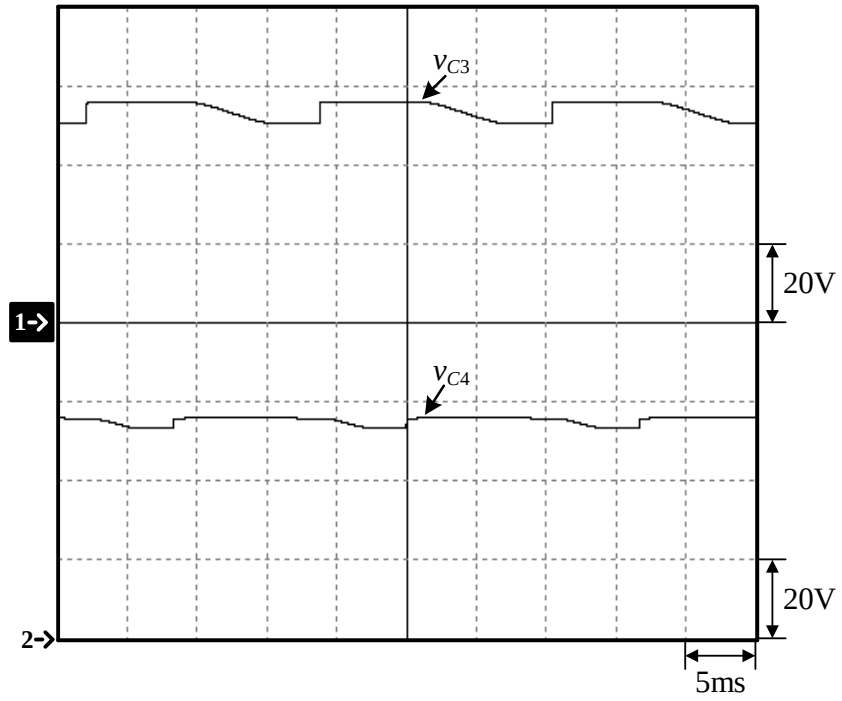


(**a**)

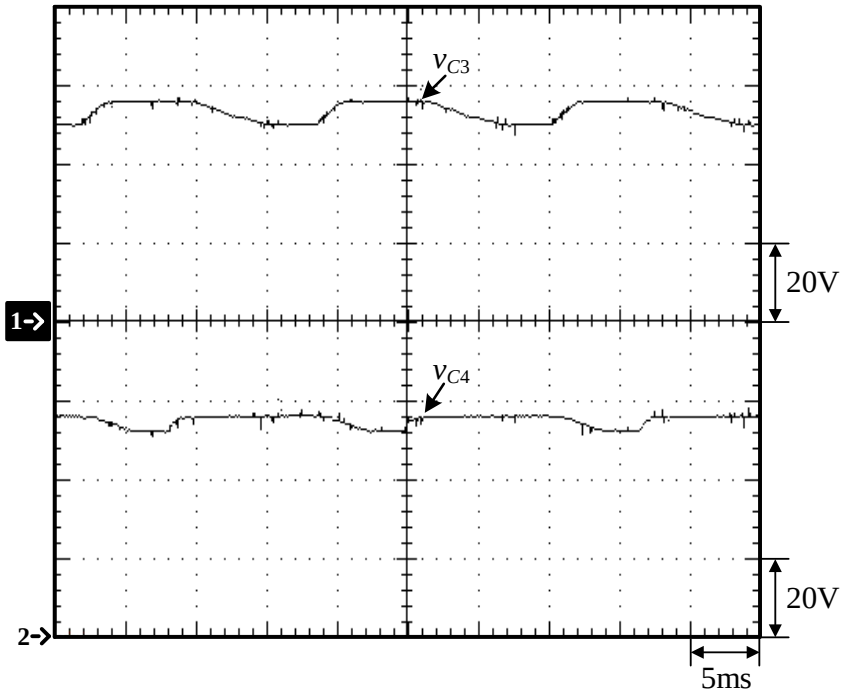


(**b**)

Figure 17. Waveforms at rated load with (1) v_{C1} and (2) v_{C2}: (**a**) simulated; (**b**) measured.

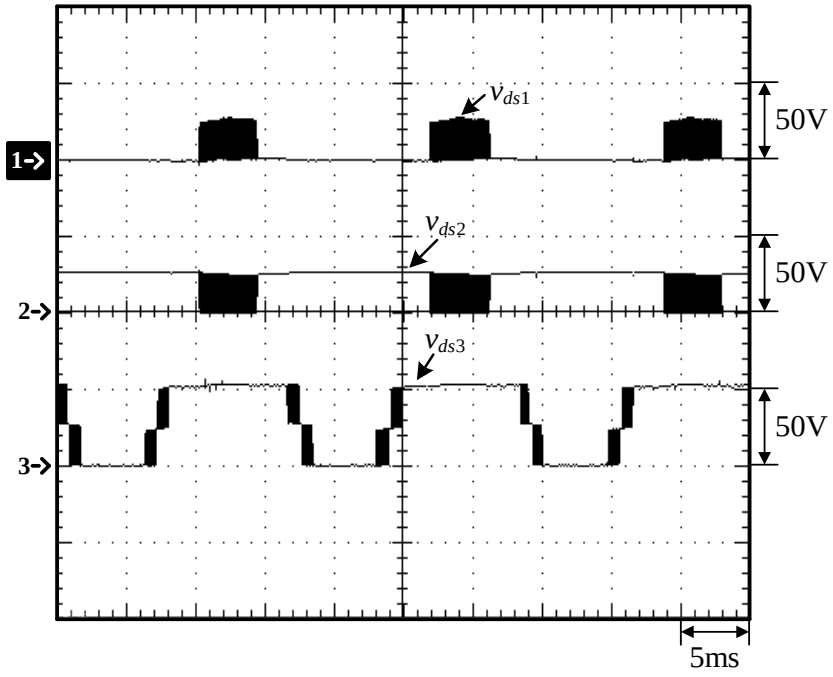


(**a**)

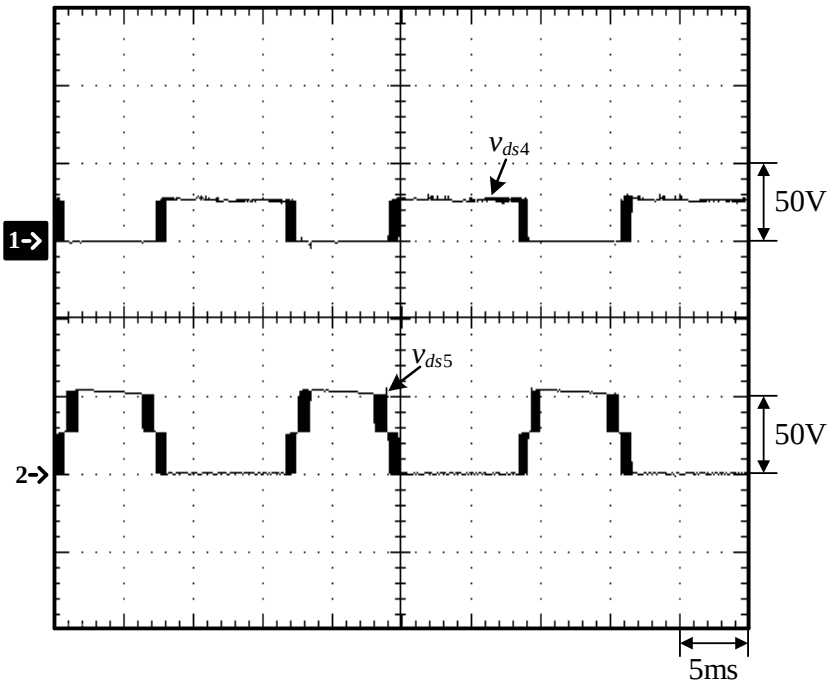


(**b**)

Figure 18. Waveforms at rated load with (1) v_{C3} and (2) v_{C4}: (**a**) simulated; (**b**) measured.



(**a**)



(**b**)

Figure 19. Waveforms measured at rated load with (**a**) (1) v_{ds1}, (2) v_{ds2}, and (3) v_{ds3}; (**b**) (1) v_{ds4} and (2) v_{ds5}.

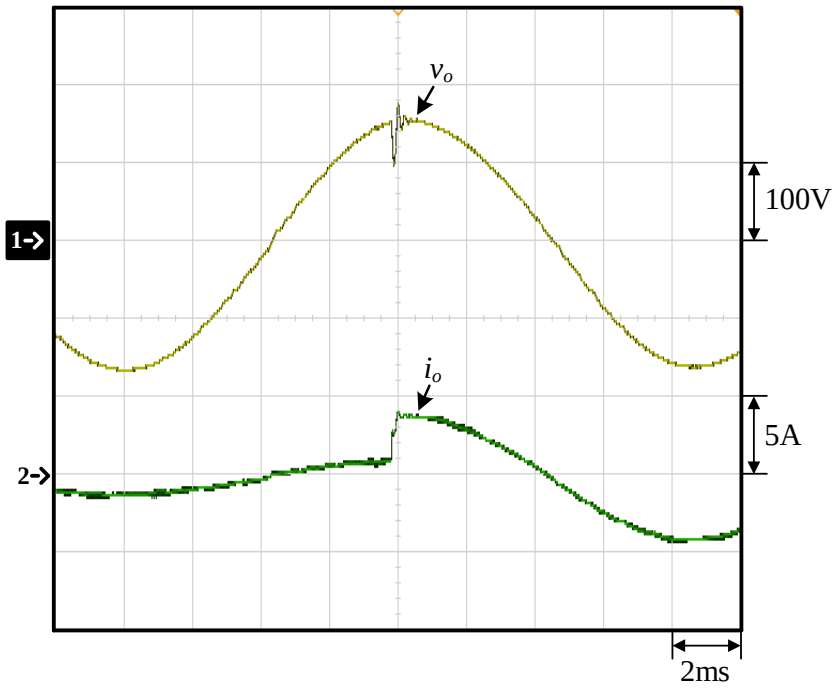


Figure 20. Measured waveforms of uploading from 25% load to 100% load: (1) v_o; (2) i_o.

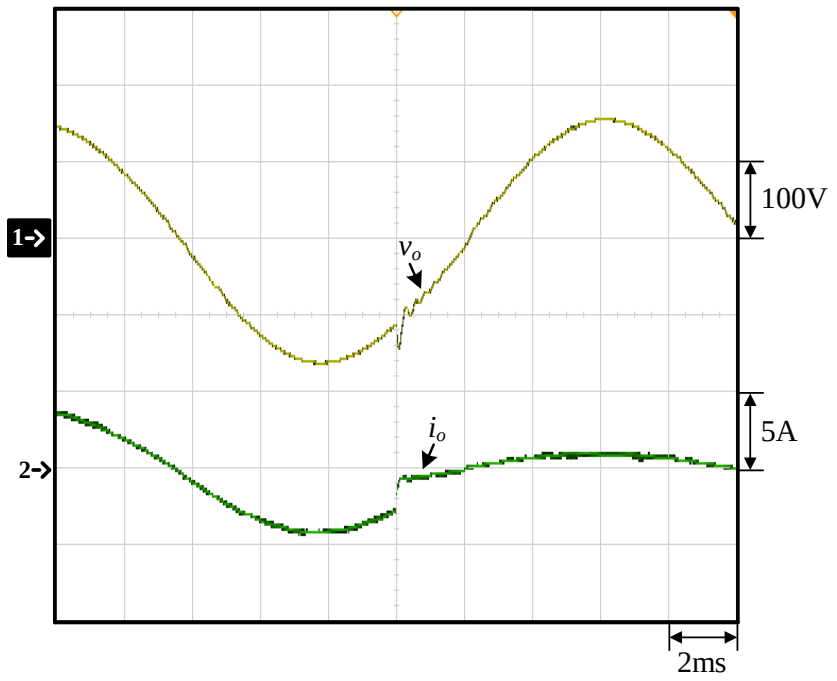


Figure 21. Measured waveform of downloading from 100% load to 25% load: (1) v_o; (2) i_o.

5.3. Voltage Harmonic Distribution

Figures 22 and 23 show the voltage harmonic distribution at 100% and 25% load, respectively. The total harmonic distortion (THD) of the output voltage of the single source T-type 7-phase DC-AC inverter at 100% load and 25% load are 2.01% and 3.36%, respectively, which are small enough to remove or downsize the output filter, leading to less volume and cost. Furthermore, the proposed DC-AC inverter can indeed meet the IEEE 519–1992 requirement of less than 5% THD of voltage harmonics.

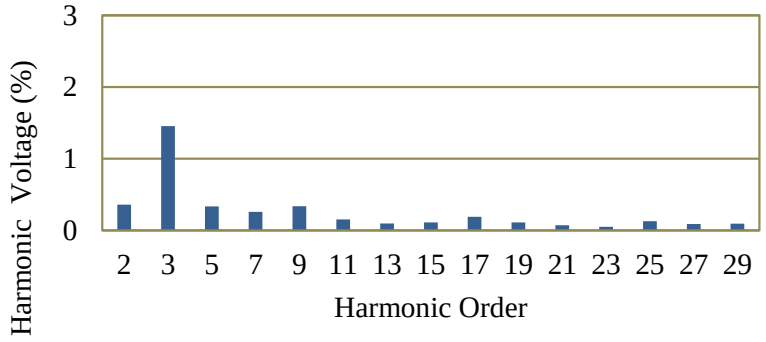


Figure 22. Voltage harmonic distribution at 100% load.

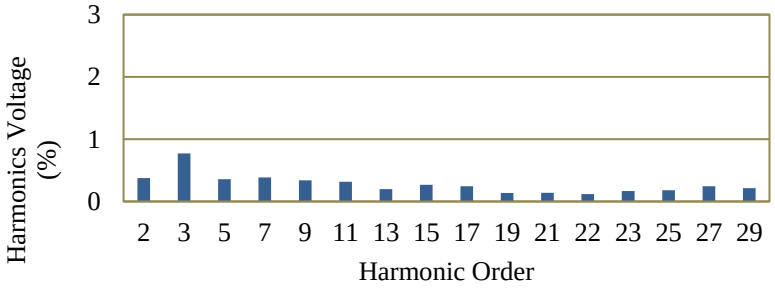


Figure 23. Voltage harmonic distribution at 25% load.

5.4. Efficiency Measurement

The efficiency of the proposed inverter circuit at various loads is measured as shown in Figure 24. First of all, a digital meter (Fluke 179) is used to measure the input voltage and the voltage on a current-sensing resistor (Shunt) to obtain the input current. Sequentially, the output voltage and current, total harmonic distortion, and harmonics of each number are measured by utilizing a power analyzer (PM1000+). Afterwards, the input and output powers can be obtained. Moreover, an AC electronic load (Prodigit 3255) is adopted at the load side. Eventually, the resulting input and output powers are employed to calculate the overall efficiency as illustrated in Figure 25. From this figure, it can be seen that the proposed inverter is based on the T-type circuit, thereby making the efficiency reduced as load is increased. The efficiency all over the load range is above 94% and the maximum efficiency is 97.42%.

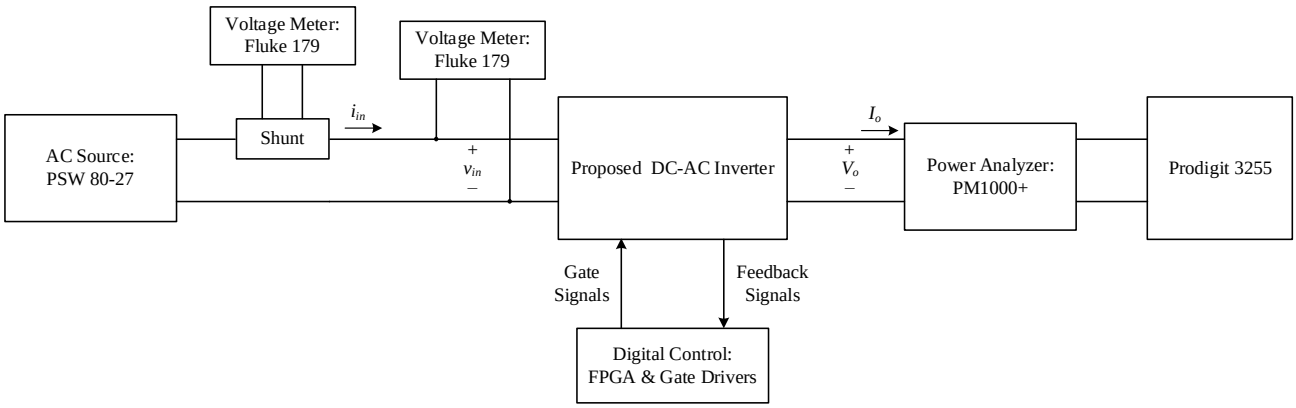


Figure 24. Efficiency measurement block diagram.

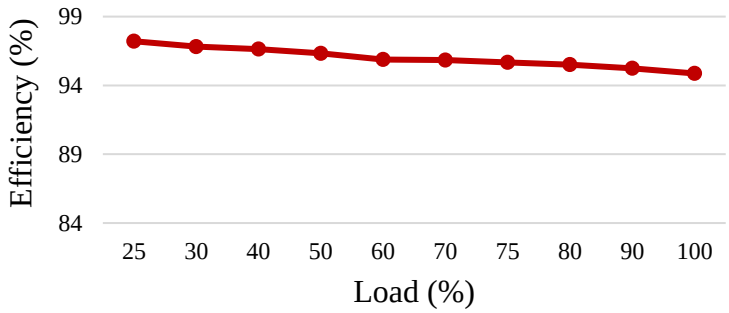


Figure 25. Curves of Efficiency against load.

5.5. Comparison between Proposed Inverter and Other Topologies

Comparisons of the proposed inverter with topologies [10–12,21,25,31–33] in various criteria and feature emphases are tabulated in Table 6. From this table, only the proposed inverter has the feedback control design and the highest voltage gain although it has the largest number of diodes.

Table 6. Comparisons between the proposed single-phase multilevel DC-AC inverter and existing topologies.

	[10]	[11]	[12]	[21]	[25]	[31]	[32]	[33]	**Proposed**
Number of Levels	7	9	9	7	7	7	7	9	7
Number of Switches	10	11	11	10	10	10	16	10	10
Number of Diodes	0	0	0	0	0	0	0	0	6
Number of Capacitors	4	2	3	4	3	0	2	2	4
Number of Transformers	0	0	0	0	0	0	0	2	0
Voltage Gain	1.5	2	2	1.5	1.5	2	3	1	3
Number of DC Power Sources	1	1	1	1	1	3	1	1	1
Rated-load Power (W)	270	300	500	150	1000	100	45	500	300
Input Voltage (V)	100	160	70	100	200	100	30	100	56
Peak Output Voltage (V)	150	150	320	150	300	200	90	100	168
Rated-load THD (%)	—	13.10	14.1	—	—	19.05	—	12.25	3.36
Peak Efficiency (%)	96.52	—	97.80	98.20	96.13	99.11	96.25	93.50	97.42
Control Strategy	SVPWM	LS-PWM	PD-PWM	SHE-PWM	SVM	SHE-PWM	SPWM	SPWM	LS-SPWM
Modeling	x	x	x	x	x	x	x	x	v
Feedback Controller Design	x	x	x	x	x	x	x	x	v

6. Conclusions

The proposed inverter has the following features as described below:

1. This circuit has a symmetrical structure possessing voltage gain of 3 and self-balancing along with low THD. As a result, the mass production interchangeability can be obtained easily.
2. Only one switch operates at any time, and not only is the corresponding control quite easy, but also any switch has very low switching losses and voltage stress.
3. Since the mathematical model of the multilevel DC-AC inverter is successfully developed using the state-space averaging method, the voltage controller for the multilevel DC-AC inverter can be designed systematically and easily.

Furthermore, since the proposed DC-AC inverter possesses low THD, the possible applications of the proposed inverter in the industry are mentioned below:

1. It can be applied to a single AC motor to reduce the torque ripple.
2. It can be also applied to the low-frequency transformer to reduce the core loss.
3. It can be applied to utility parallel of green power with relatively low electric pollution.

However, two switches have the maximum voltage stress of double input voltage. Consequently, this should be considered in practical perspective.

In addition, the possible developments of the proposed inverter in this research activity are mentioned below:

1. Many researchers have focused on the structure and output of the multilevel inverter, but comparatively few researchers on the THD and product usefulness. Accordingly, THD reduction and circuit symmetry should be investigated.
2. In general, only open-loop steady-state waveforms are shown in many papers. That is, dynamic responses are not considered. Accordingly, modeling of the multilevel inverter and closed-loop controller design should be developed.
3. Up to now, there is no standard of the input voltage. Accordingly, by taking 12 V as a base, a multiple of this base to get 24 V, 48 V, and 96 V makes the user commonality achieved.

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Conflicts of Interest: The authors declare no conflict of interest.

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