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Analytical Model and Design of Voltage Balancing Parameters of Series-Connected SiC MOSFETs Considering Non-Flat Miller Plateau of Gate Voltage

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Abstract: Series connection is an attractive approach to increase the blocking voltage of SiC power MOSFETs. Currently, the voltage balancing design of the series connection of the SiC MOSFETs highly relies on offline calibration and is challenging in the complex field operation. In this paper, a quantitative model to assess the voltage balancing performance is proposed to achieve a clear mathematical interpretation of the dynamic response of the voltage imbalance control loop. To begin with, an analytical model of the drain-source voltage rising time during the turn-off transient concerning the non-constant Miller plateau is proposed. Based on the turn-off model of the single device, the voltage imbalance sensitivity (VIS) is proposed to describe the influence of the parameters on the gate driving signals on the voltage imbalance. The VIS parameter can be easily achieved from the behavior of single devices, abandoning the complex variables in series connection. Further, for the typical case, active time delay voltage balancing methods are selected to demonstrate the application of the VIS analysis method. Based on VIS, the accurate close-loop design is proposed for controlling the delayed time among the devices. The proposed analysis and method are verified in simulation and experiment. The paper offers a generalized approach to assess the performance and the design of the series connection of the SiC MOSFETs, which can be further applied in many other methods for parameter design and engineering applications.

Keywords: voltage balancing; SiC power MOSFETs; analytical model; active time delay control

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1. Introduction

The applications of medium voltage (MV) high power converters are rapidly growing in smart grids, motor drives, supercharge stations, and many other applications. The performance of the conventional MV converters is largely defined by the performance of the Si devices. Compared with Si devices, SiC MOSFETs have higher switching frequency, higher blocking voltage capability and lower switching loss, which make it attractive in the medium voltage and high-power applications [1].

However, the highest voltage rating of commercially available SiC MOSFETs is only 1.7 kV. Some companies offer 10 kV SiC device samples [2], yet there is still a long way for the high voltage devices to be widely available. To increase the blocking voltage of the SiC MOSFETs, direct series connection is one of the superior techniques. The potential benefits include low cost and high current density per unit area of chips [3,4]. Much research has gone into realizing a reliable series connection operation of the power devices.

Due to the variation of the parameters of the devices and external circuit parameters, voltage imbalance is unavoidable in the series connection of power devices. Voltage imbalance elimination is the most important issue in the series connection. Since the

series connection of IGBTs has been widely adopted in industry, the series connection of SiC MOSFETs inherits the techniques from IGBT at first. However, due to the fast-switching characteristic, the series connection of SiC MOSFETs is more sensitive to the uneven parameters among the devices, such as gate driver signals delay time.

The widely applied method in the series connection is to adopt simple parallel passive snubbers, such as the resistor-capacitor (RC) snubber, to attenuate the deviation of the parameters [5,6]. Based on the basic circuit, some improvements on passive clamping circuit are proposed. A DC breaker composed of two series-connected devices with the passive balancing circuit is given in [7]. A 3600 V/200 A power module based on the series connection of three 1200 V SiC MOSFETs is proposed in [8,9], where a resistor-capacitor-diode (RCD) snubber is adopted to balance the voltage. The combination of SiC MOSFETs and SiC JFET, called super-cascade, is proposed with a simple structure and high blocking voltage [4,10]. A series-connected 4000 V SiC MOSFETs is applied in a flyback circuit in [11], where an extra parallel capacitor is added in parallel with RC snubber to compensate the imbalanced parasitics in the circuit. However, for these passive methods, the drawback is the extra switching loss introduced by the snubbers, which is especially not desired in high switching speed SiC devices. A clamping circuit with an energy recovering function is presented in [12] to balance the voltage as well as reduce the switching loss. However, the snubber loss cannot be fully avoided. A single gate driving circuit for two series-connected SiC MOSFETs is proposed in [13]. However, the influence of the DC bus voltage on the switching speed of the devices cannot be fully eliminated.

As an improvement, the close loop control of voltage imbalance has been widely adopted. Generally, the turn-off voltage rising speed (*dv/dt*) and gate signal delay time are the two most widely adopted control freedoms. The voltage rising slope can be adjusted by the multi-stage gate driver [14] or by adding a compensating signal to the driving voltage [15,16]. An active *dv/dt* control method is proposed to compensate the parasitic capacitance between the devices and the ground [17]. However, due to the extremely fast switching speed of SiC MOSFETs, there is a high requirement on the response speed of the close loop *dv/dt* controller, which is difficult to design and sensitive to the EMI noise of the circuit.

The active gate driving signal delay control method, which adds a compensated delay time in the gate driving signals among the series-connected devices to balance the voltage, has been widely explored for many years [18–20]. Compared with passive snubbers and *dv/dt* control methods, it has limited influence on the switching speed of the device. Thus, the voltage balancing control is independent of the switching of the power device. Recently, studies on active gate time delay method in the series connection of SiC MOSFETs have been proposed. In [21], the delayed time is generated by a fast drain-source voltage sampling circuit compared with a preset reference voltage. However, the reference voltage is difficult to set considering the variable operating conditions. In [22], proportional-integral (PI) controller with active time delay is adopted in the series connection of SiC MOSFETs. However, the relationship between the delayed time and the voltage imbalance must be calibrated offline, which is challenging in complex operation conditions. In [23], it is pointed out that the relationship varies with operation points and makes it difficult to design the close loop parameters. The accurate modeling of the voltage imbalance is necessary to assist the control loop deign.

To overcome the challenge, in this paper, the turn-off behavior of the SiC MOSFETs is deeply investigated first. Conventionally, the model of the turn-off relies on the assumption that there is a constant gate-source voltage during the voltage rising transition, called the Miller plateau [24]. In this paper, an improved device turn-off model considering the non-constant gate-source voltage during the Miller plateau is proposed. Then, the drain voltage rising time is accurately calculated and the analytical model of the voltage imbalance is proposed to realize quantitative control loop design of the active voltage balancing methods. With the proposed model, the mathematical boundary of the parameter selection is clear, and the stability of the control loop can be guaranteed under different operation conditions.

2. Analytical Model of Voltage Rising Time at Turn-Off of SiC Power Module

Typically, voltage imbalance occurs when SiC MOSFETs are turned off. Therefore, it is necessary to give a deep analysis on the turn-off behavior of the device. The classical models adopt linear parameter approximation of the voltage-dependent junction capacitance and nonlinear transconductance [24,25]. However, the linearity of the parameters has a significant impact on the operation of the devices and requires special consideration [26,27].

In this section, the turn-off behavior of devices in a half-bridge circuit under hard switching with inductive load is investigated. The equivalent circuit is given in Figure 1. The lower device is the switching device and the upper device acts as the freewheel diode. V_{dc} is the DC bus voltage. V_{g_on} is the static positive gate-source voltage and V_{g_off} is the static negative gate-source voltage. L_d is the leakage inductance in the power loop. L_s is the common source inductance.

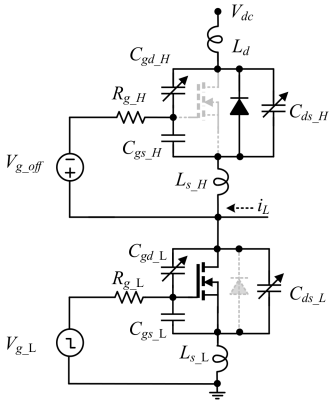

Figure 1. Equivalent circuit of half-bridge SiC MOSFET circuit in hard switching with inductive load.

In this paper, the series connection of high-power modules is considered. Typically, the high-power SiC MOSFET modules have separate gate-source driving loop (realized by Kelvin terminal). Therefore, in the following analysis, the assumption L_s = 0 nH is adopted. However, L_s cannot be fully eliminated and the assumption here is for the sake simplification. C_{gd}, C_{ds}, and C_{gs} are the gate-drain capacitance, drain-source capacitance, and gate-source capacitance accordingly. R_g is the gate driving resistor. The subscript '$\_L$' means the parameter in the lower device and '$\_H$' means the parameter in the upper device in the phase leg.

As demonstrated in Figure 2, the turn-off process is divided into three stages, namely turn-off delay stage (s_0: t_0–t_1), voltage rising stage (s_1: t_1–t_2), and current dropping stage (s_2: t_2–t_3). The stage t_1–t_2 is mainly considered due to the extremely fast rising speed of the drain-source voltage, which dominates the voltage imbalance in the series connection.

At t_0, the device starts to turn off, the gate-source voltage decreases from V_{g_on} to the beginning of the Miller plateau voltage. In this stage, SiC MOSFET operates in the linear region. This stage ends when gate-source voltage cannot support the output current I_L and the device enters the saturation region. The relationship between the gate-source voltage $v_{gs\_L}(t)$ and the channel current i_{ch} during the saturation region is [28]

$$i_{ch} = g_s\left(v_{gs} - V_{th}\right)^2 \tag{1}$$

where g_s is the transconductance, V_{th} is the threshold voltage. At $t = t_1$, $i_{ch} = I_L$, the gate-source voltage V_{mil} is

$$V_{mil} = V_{th} + \sqrt{\frac{I_L}{g_s}} \tag{2}$$

The expression of the gate-source voltage $v_{gs\_L}(t)$ is

$$v_{gs\_L}(t) = \left(V_{g\_on} - V_{g\_off}\right)e\left(-\frac{t - t_3}{R_{g\_L}C_{gs\_L}}\right) + V_{g\_off} \tag{3}$$

The duration of this stage is

$$t_1 - t_0 = \ln\left(\frac{V_{g\_on} - V_{g\_off}}{V_{mil} - V_{g\_off}}\right) \tag{4}$$

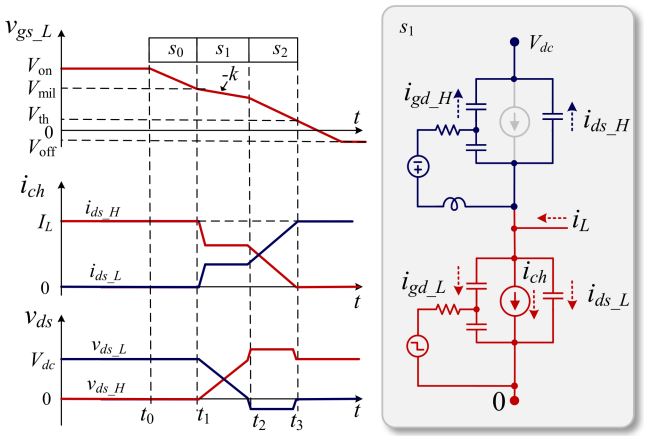

Figure 2. Simplified waveform of gate source voltage, channel current, and drain source voltage. On the right, the equivalent circuit when drain source voltage is dramatically increasing.

In the stage (t_1–t_2), SiC MOSFET operates in the saturation region and the drain-source voltage rises dramatically. The power MOSFET acts as a gate-source voltage-controlled current source, as the equivalent circuit demonstrated in Figure 2. Meanwhile, the drain-source capacitor of the lower device is charged and the upper device is discharged by the difference between load current and channel current of the lower device. When the drain-source voltage is increasing, there is a displaced current injected into the lower gate-source capacitor to prevent the decrease of the gate-source voltage, which is called the Miller effect. The load current is composed of the charging or discharging current of the parallel capacitor and the channel current. According to the equivalent circuit in Figure 1, the status equation is

$$\begin{cases} V_{g\_off} = R_{g\_L}i_{g\_L} + v_{gs\_L} \\ V_{dc} = v_{ds\_L} + v_{ds\_H} + L_d\frac{di_{ds\_L}}{dt} \\ i_{g\_L} = C_{gs\_L}\frac{dv_{gs\_L}}{dt} + C_{gd\_L}\frac{dv_{gd\_L}}{dt} \\ I_L = i_{ch} + \left(C_{ds\_L} + C_{gd\_L}\right)\frac{dv_{ds\_L}}{dt} + \left(C_{ds\_H} + C_{gd\_H}\right)\frac{dv_{ds\_H}}{dt} \\ i_{ds\_L} = i_{ch} + C_{ds\_L}\frac{dv_{ds\_L}}{dt} \\ i_{ch} = g_s\left(v_{gs\_L} - V_{th}\right)^2 \end{cases} \tag{5}$$

It is obvious that the above equation is a nonlinear differential equation that contains the nonlinear transconductance and voltage dependent junction capacitor. It is difficult to solve the equation directly, and further simplification is required to get the time domain expression of the parameters.

Firstly, during the Miller plateau, a measured waveform of SiC power MOSFET module is given in Figure 3 as an example. It is demonstrated that a gate-source voltage drop is observed during the voltage rising period, which is not the same as the phenomenon in Si IGBTs. The non-constant Miller plateau is due to the feedback gate-drain displacement current is not enough to support the gate-source voltage. This phenomenon can also be

found in other literatures on SiC devices characterization results [5,29]. Thus, the gate-source voltage is slightly decreasing during the voltage rising period. In this paper, this stage is described by a linear approximation of the gate-source voltage drop in this stage, which is

$$v_{gs\_L} = V_{mil} - k(t - t_1) \tag{6}$$

where k is the voltage decreasing slope. The stage ends when the voltage of the lower device rises to the DC bus voltage, and then the diode of the upper device starts to conduct and clamps the drain-source voltage. The duration of the stage is the voltage rising time t_{rv}.

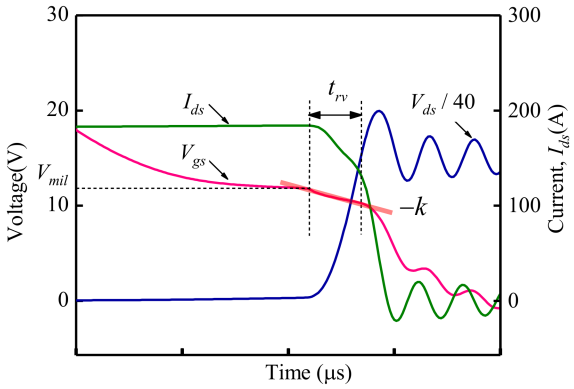

Figure 3. Measured waveform during Miller plateau. Gate source voltage drop is observed and linearly approximated.

Secondly, another consideration is the voltage dependence of the junction capacitance. Since the detailed transition curve of the drain-source voltage is not of interest in to calculating the voltage rising time, by integration, both sides of the differential Equation (5) is transferred into charge equation as

$$\begin{cases} \frac{V_{g\_off}}{R_{g\_L}} t_{rv} = \int_0^{t_{rv}} \left(C_{gs\_L} \frac{dv_{gs\_L}}{dt} + C_{gd\_L} \frac{dv_{gd\_L}}{dt} + \frac{v_{gs\_L}}{R_{g\_L}} \right) dt \\ I_L t_{rv} = Q_{ch} + Q_{oss\_L} + Q_{oss\_H} \end{cases} \tag{7}$$

where t_{rv} is voltage rising time and Q_{ch}, Q_{oss_L}, and Q_{oss_H} are the charge flow through the MOSFET channel during the voltage rising time, parallel output capacitance of lower device, and upper device, respectively. The charge flow through parallel capacitance can be extracted from datasheet as

$$Q_{oss} = \int_{V_1}^{V_2} C_{oss}(v_{ds}) dv_{ds} \tag{8}$$

where V_1, V_2 are voltage at the initial and end time of the voltage rising curve. In the analysis, V_1 is the voltage when the device enters the saturation region and V_2 equals to V_{dc}. Moreover, if the extra parallel capacitor is added in some applications, the charge of the capacitor should also be included in (8). With the approximation of the gate-source voltage in (6) and the charge equation, (7) is simplified as

$$\begin{cases} \frac{V_{g\_off}}{R_{g\_L}} t_{rv} = C_{gs\_L}(-kt_{rv}) + \frac{V_{mil} t_{rv}}{R_{g\_L}} - \frac{k t_{rv}^2}{2R_{g\_L}} + Q_{gd\_L} \\ I_L t_{rv} = \frac{g_s}{-3k}(V_{mil} - kt_{rv} - V_{th})^3 + \frac{g_s}{3k}(V_{mil} - V_{th})^3 + Q_{oss\_L} + Q_{oss\_H} \end{cases} \tag{9}$$

The above equation contains only two unknown parameters, namely the voltage rising time t_{rv} and the gate-source voltage decreasing slope k. Thus, they can be directly acquired by solving the equation. Since it is the high-order equation, the result can be numerically solved with the help of mathematical software such as Matlab.

In this section, the analytical model of the turn-off of SiC MOSFETs is given, considering the nonlinear parameters. The gate-source voltage is described by a linear voltage drop

and time-domain differential equation is transferred into the charge equation to achieve the accurate voltage rising time. The parameters in the calculation come from the datasheet or the characterization test of the SiC MOSFETs. The turn-off drain voltage rising time will be adopted as the link between the voltage imbalance and the gate driver time delay, which will be discussed in the following section.

3. Voltage Imbalance Model of Series Connected SiC Power Module

Although it is expected that the series-connected devices switch at the same time, due to the deviation of various parameters, the turn-off of series-connected SiC MOSFETs is not ideally synchronized. The relationship between the voltage imbalance and the different turn-off time is analytically modeled in this section. Further, the concept of voltage imbalance sensitivity is proposed to evaluate the influence of the gate driver time deviation on the voltage imbalance.

3.1. Analytical Model of Voltage Imbalance

Take two devices in series for example. The equivalent circuit is demonstrated in Figure 4. In the following analysis, the gate driver time delay is assumed to be far smaller than the voltage rising time t_{rv}. It is a reasonable assumption considering the parameters of the series-connected device and the circuit parameters are designed to be as identical as possible in engineering practice. Under this assumption, the equivalent circuit of two series-connected devices and the operation waveform is given in Figure 5. The DC bus voltage is 2 V_{dc}, where V_{dc} is the voltage stress of one device.

Based on the analysis in Section 2, the gate-source voltage will slightly drop during the voltage rising stage (stage t_1–t_2). The gate-source voltage is in (6) and the channel current is given in (1). As pictured in Figure 5a, the MOSFET channel current is viewed as gate-source voltage controlled current source. In the figure, i_{ds} is the device drain-source current, i_{ch1} and i_{ch2} are the channel current, and i_{oss1} and i_{oss2} are the charging current of the equivalent drain-source capacitance.

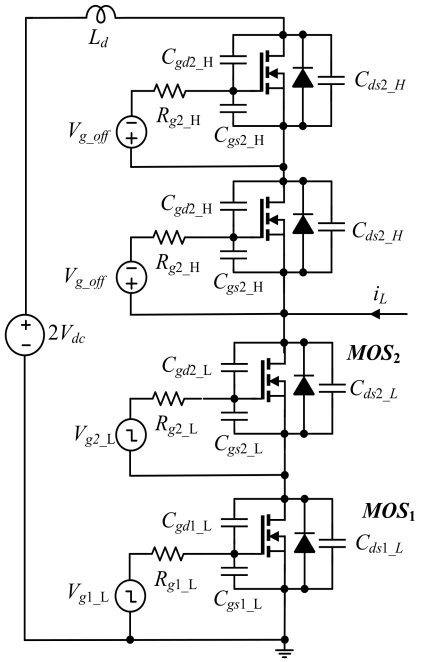

Figure 4. Equivalent circuit of two series connected SiC MOSFETs.

As demonstrated in Figure 5b, before the saturation region of the SiC MOSFETs, the gate-source voltages of the two devices are V_{mil}. The MOSFET channel current equals to the load current I_L. Assume at time $t = 0$, MOS_1 begins to turn off and after time Δt, MOS_2 starts to turn off. The drain-source voltage of MOS_1 rises first, followed by MOS_2. This stage ends

at the sum of drain-source voltages equal to the bus voltage, then the antiparallel diode of the upper device starts to conduct. During the process, the MOS_1 has a higher drain-source voltage than MOS_2, as a result, the total charge feedback from Miller capacitance is larger than MOS_2. Thus, the gate-source voltage drop slope k_1 of MOS_1 is slower than k_2 of MOS_2. Therefore, the voltage rising slope of MOS_2 is less than MOS_1. Due to this self-regulation mechanism, at the end of the period, the gate-source voltage of the two devices can be viewed as nearly the same.

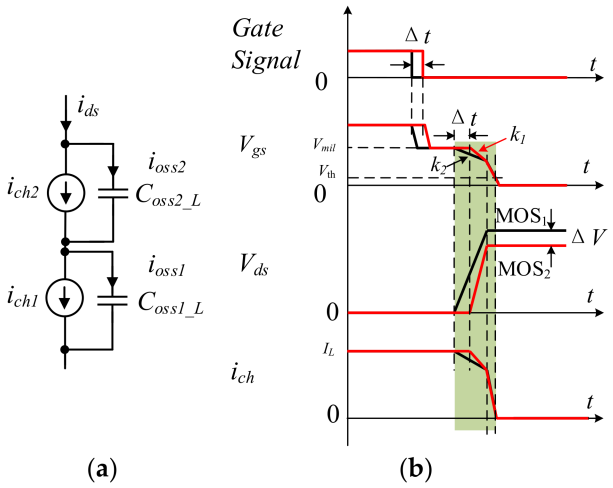

Figure 5. (**a**) Equivalent circuit of series connection; (**b**) turn off waveform approximation under small gate driving time delay condition.

Assuming the ideal balanced conditions, the gate-source voltage decreasing slope is k. Introducing the deviation Δk to describe the difference when Δt exists, the gate voltage decreasing slope of MOS_1 and MOS_2 is $k_1 = k + \Delta k$, $k_2 = k - \Delta k$, respectively. The expression of the gate voltage of MOS_1 and MOS_2 is

$$\begin{aligned} v_{gs1\_L} &= \begin{cases} V_{mil} & 0 < t < \Delta t \\ V_{mil} - (k + \Delta k)(t - \Delta t), & \Delta t < t < t_{rv} \end{cases} \\ v_{gs2\_L} &= V_{mil} - (k - \Delta k)t, \qquad 0 < t < t_{rv} \end{aligned} \tag{10}$$

where t_{rv} is the voltage rising time in the ideal balanced condition and can be calculated by (9) in a single device by dividing the circuit parameters in series connection by half. At $t = t_{rv}$, $V_{gs1\_L} = V_{gs2\_L}$, Δk is expressed as

$$\Delta k = \frac{\Delta t}{2t_{rv}} k \tag{11}$$

Accordingly, the channel current during the voltage rising period is

$$\begin{aligned} i_{ch1} &= \begin{cases} I_L, & 0 < t < \Delta t \\ g_s(V_{mil} - (k + \Delta k)(t - \Delta t) - V_{th})^2, & \Delta t < t < t_{rv} \end{cases} \\ i_{ch2} &= g_s(V_{mil} - (k - \Delta k)t - V_{th})^2, \qquad 0 < t < t_{rv} \end{aligned} \tag{12}$$

As demonstrated in Figure 5a, the current flow through MOS_1 and MOS_2 satisfies

$$\begin{aligned} i_{ds} &= i_{ch1} + i_{oss1} \\ i_{ds} &= i_{ch2} + i_{oss2} \end{aligned} \tag{13}$$

To convert the current equation into the charge equation, time integration is conducted on both sides of (13) giving

$$\begin{array}{l} Q_{ds} = \int_0^{t_{rv}} i_{ch1}(\tau)d\tau - Q_{oss1} \\ Q_{ds} = \int_0^{t_{rv}} i_{ch2}(\tau)d\tau - Q_{oss2} \end{array} \tag{14}$$

where Q_L is the load charge flow to the lower devices, Q_{oss1} and Q_{oss2} are charge flow through the parallel capacitors of the device. Substituting (12) into (14)

$$\begin{array}{rl} Q_{oss2} - Q_{oss1} = & \int_{\Delta t}^{t}\left(g_s(V_{mil} - k_1(\tau - \Delta t) - V_{th})^2\right)d\tau \\ & -\int_{\Delta t}^{t}\left(g_s(V_{mil} - k_2\tau - V_{th})^2\right)d\tau \\ & +I_L\Delta t - \int_0^{\Delta t}\left(g_s(V_{mil} - k_2\tau - V_{th})^2\right)d\tau \end{array} \tag{15}$$

In time interval [0, Δt], the channel current starts to decrease from I_L, under the small gate driving delayed time condition, the charging current of the output capacitor is very small in this period, thus the second and third item in (15) can be neglected. Meanwhile, although the output capacitance is voltage dependent, the capacitance can be viewed as the same under high blocking voltage conditions and can be extracted from the datasheet. The voltage imbalance can be calculated as

$$\Delta V = \frac{2g_s k\Delta t\left(F_{turnofff}(t_{rv}) - F_{turnoff}(\Delta t)\right)}{C_{oss}} \tag{16}$$

where C_{oss} is the output capacitance of the SiC MOSFET at half DC bus voltage conditions. The function $F_{turnoff}(t)$ is

$$F_{turnoff}(t) = (V_{mil} - V_{th})t - \left(k + \frac{V_{mil} - V_{th}}{t_{rv}}\right)\frac{t^2}{2} + \frac{k}{t_{rv}}\frac{t^3}{3} \tag{17}$$

(16) is the final expression of the voltage unbalance. The parameters k and t_{rv} are the gate-source voltage decreasing slope and voltage rising time under ideal conditions.

Moreover, when the voltage of the series-connected device exceeds the bus voltage and then enters stage (t_2–t_3), the channel current will decrease rapidly. Since the channel current of the two series-connected devices are nearly the same at the beginning of the stage (t_2–t_3), the voltage imbalance remains the same during this period.

3.2. Voltage Imbalance Sensitivity

It is of vital importance to evaluate the influence of the gate driving signal time delay on the voltage imbalance. The expression of the voltage imbalance indicates that this relationship is related to various parameters coupled together. Here, the voltage imbalance sensitivity (*VIS*) is defined as the ratio between the voltage imbalance and the time delay Δt, as

$$VIS = \frac{\Delta V}{\Delta t} \tag{18}$$

VIS has clear physical meaning that it is the value of voltage imbalance caused by a unit time delay. For example, if *VIS* = 20 V/ns, it means the voltage imbalance caused by 1 ns gate driver time delay is 20 V. Smaller *VIS* means smaller voltage imbalance from the external disturbance, which is desired for series connection of power devices. It can be acquired from (9) that

$$kt_{rv} = \frac{3(V_{miller} - V_{th}) - \sqrt{9(V_{miller} - V_{th})^2 - \frac{12(Q_{oss\_L} + Q_{oss\_H})}{g_s t_{rv}}}}{2} \tag{19}$$

Substituting (19) into (16), following expression is achieved

$$VIS = \frac{2V_{dc}}{t_{rv}} \tag{20}$$

This is an important relationship describing *VIS* between the DC bus voltage and voltage rising time. When the increasing speed of the DC bus voltage increases, *VIS* increases to make the series-connected device more sensitive to the gate drive signal delay time. The influence of the load current, extra parallel capacitance, and DC bus voltage are also included in the expression of t_{rv}.

Although previous research has adopted the linear relationship between the gate driver time delay and voltage imbalance in the design, the proposed model gives a theoretical proof and analytical model to calculate the proportional coefficient.

Further important information is that the performance of the single device reflects the performance of the series connection. In (20), the parameters are calculated from the single device and with no need to consider the multiple devices in series. By adjusting the parameter of the single device, the performance of the series-connected device is acquired. There is no need to build the relatively complex test setup for the series-connected device in the early design stage in engineering applications. In addition, the voltage rising time can also be acquired from a double pulse test in a single device so as to simplify the test setup.

4. Close Loop Design of Active Time Delay Voltage Balancing Method

Without causing extra switching loss for SiC MOSFETs, active time delay for voltage balance control has been widely adopted in the series connection of SiC MOSFETs. The challenge is to ensure a stable close-loop design and reduce the amount of the offline calibration. Few existing studies discuss how to design the control loop parameter and are mostly based on experimental tests. However, the mathematical interpretation is not clear yet and the optimized design cannot be guaranteed. With the help of the *VIS* model, the quantitative close-loop design is realistic.

Figure 6 demonstrates the general structure of the close loop active gate driving time delay method. After the devices are turned off and the drain-source voltage reaches the steady-state, the drain-source voltage of each device is sampled and sent to a central controller. In the central controller, the gate driver time delay is generated from the control algorithm and distributed to each device. Traditionally, a lookup table is adopted to generate the delayed time [12,23,30]. However, the relationship between delayed time and the voltage imbalance needs offline calibration and may change over time. As a result, the application is limited in the variable operation conditions of the converter.

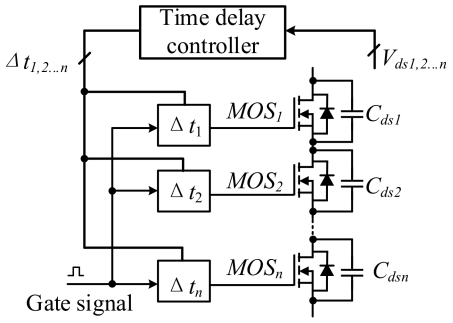

Figure 6. Close loop control of voltage imbalance with active gate drive time delay.

4.1. Control Loop Design

In this section, a PI controller is adopted to control the operation time. The control diagram is given in Figure 7. $\Delta v_{cmd} = 0$ is the reference of the voltage unbalance of the series-connected devices. T_s is the switching period. K_p and K_i are parameters of the PI controller.

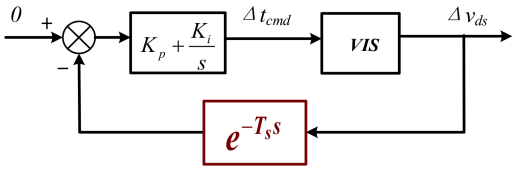

Figure 7. Control diagram of the active time delay for voltage balancing.

Since the delayed time is effective in the next switching cycle, there exists one switching period delay in the control loop. As discussed before, the coefficient between the delayed time and the imbalance voltage is *VIS*.

The transfer function of the close loop is

$$G(s) = VIS \cdot \left(K_p + \frac{K_i}{s}\right) e^{-T_s s} \tag{21}$$

With this control diagram, the traditional control loop design can be leveraged here. Based on the previous analysis, the parameter *VIS* increases with the operation point of the device, including the voltage and the load current. Thus, in the control loop design, *VIS* at the maximum operation voltage and current should be selected to ensure overall stability of the control loop.

The calculation of the PI parameter is mainly based on the engineering experience. One commonly adopted strategy is the crossover frequency is 0.05 times the switching frequency. The zero of the PI controller is selected as ten times the crossover frequency. Then, K_i and K_p can be calculated accordingly. Taking *VIS* as 20 V/ns and the switching frequency as 10 kHz, for example, the bode plot of the designed controller is demonstrated in Figure 8.

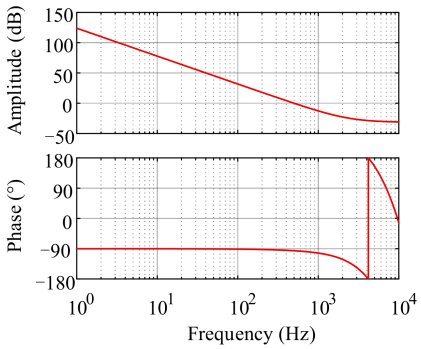

Figure 8. Bode plot of the designed control loop.

4.2. Simulation Verification

To verify the effectiveness of the proposed method, spice simulation of two series of connected devices was conducted. The Pspice model of the SiC MOSFET from Rohm 1200 V/200 A module was adopted in the simulation. In the simulation, *VIS* was set at 12.5 V/ns by adjusting the turn-off resistor of the SiC MOSEFT. Initially, 8 ns gate driver time delay was added in one MOSFET, thus leading to around 100 V voltage imbalance among the series-connected devices. Figure 9 demonstrates the variation of the voltage imbalance after each switching cycle at 500 Hz bandwidth (a) and 1 kHz bandwidth (b). It is demonstrated that the voltage imbalance reduces to zero after several switching cycles. When the bandwidth is 1 kHz, the phase margin reduces due to the switching period time delay in the control loop. Thus, there exists overshoot in the response curve. Since the control loop is discrete in the digital control systems, the response of the control model in Figure 7 is discretized and calculated in Matlab at the same time. The response of the voltage imbalance matches well with the simulation in both cases.

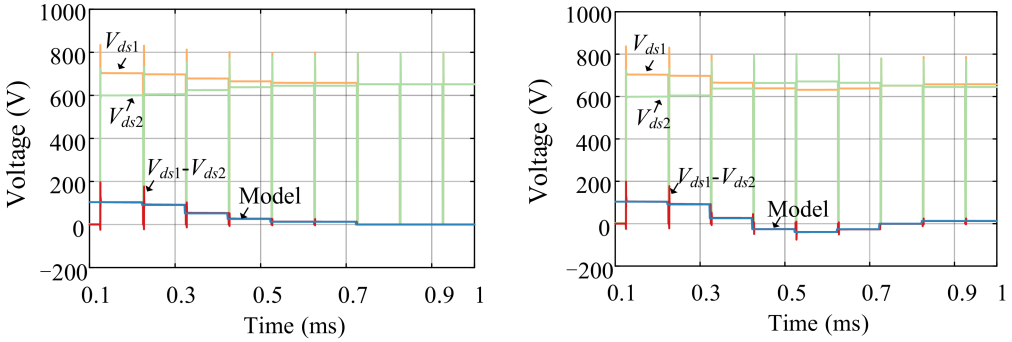

Figure 9. Simulation verification of the control loop design at 1300 V/200 A. (**a**) Crossover frequency is 500 Hz; (**b**) crossover frequency is 1 kHz.

The proposed scheme adopts the PI controller to adjust the active gate driver delay time. Since the bandwidth of the control loop is not very high, the proposed scheme can be fulfilled in most conventional digital controllers and does not require high-speed sampling circuit of the drain-source voltage. Further, in this design, the PI controller is selected in active time delay for voltage imbalance control. Other similar controllers can also be adopted. The theoretical basis is the analytical model of the *VIS*, which realizes the quantitative control loop design.

5. Experimental Verification

In this section, the verification of the analytical model of turn-off of SiC MOSFETs, the voltage imbalance model, and the control loop design are given step by step.

5.1. Experimental Platform and Parameters of SiC MOSFETs

The circuit of the double pulse tester was the same as Figure 1 and the load was inductor. The photograph of the test platform is shown in Figure 10. The lower device acted as the device under test. The Rohm 1200 V/200 A SiC MOSFET power module was the device under test and the freewheel diode was the antiparallel diode of the power module. In each half-bridge module, two devices were connected in series and each device had an independent gate driver. Each gate driver had a digital controller and drain-source voltage sampling circuit. The digital controller sent the drain-source voltage to a FPGA by communication through fiber optics and the drive PWM of the gate driver could be controlled independently. The PI controller was realized in FPGA. The drain-source current was sampled by the shunt resistor with 200 MHz bandwidth. The bandwidth of the voltage probe was 75 MHz.

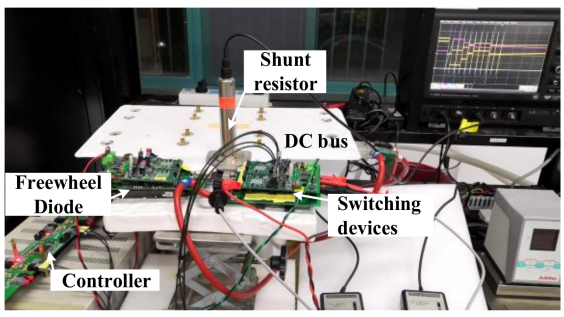

Figure 10. Inductive load test setup of two devices in series connection.

The 1200 V/200 A SiC power module from Rohm company was adopted in the experiment. The parameters of the SiC MOSFET are demonstrated in Table 1. The gate drive voltage was +18 V/−2 V as suggested by the application note. Different values of

gate resistor were adopted to verify the model under various operation conditions. The leakage inductance in the power loop was 58 nH. According to the datasheet, the gate-source capacitor was 17.8 nF. Traditionally, the threshold voltage of the power device is directly achieved from the datasheet. However, it may lead to a relatively large error in the V_{gs}-I_{ds} transfer characteristic of the device. As an improvement, the transconductance was selected as g_s = 5.9 A/V^2 and V_{th} = 6.9 V by curve fitting. As demonstrated in Figure 11, the blue curve is the V_{gs}-I_{ds} from the datasheet value, and the red curve is the fitted one. It can be seen that a better overall match can be achieved with the adjusted value. In this assumption, the threshold voltage does not have physical meaning but is closer to the curve in the datasheet. Moreover, the total charge stored in output capacitance under the DC bus voltage was 1154.0 nC. The total charge stored in Miller capacitance under the DC bus voltage was 138.2 nC. Accordingly, the junction capacitor C_{ds} = 2.2 nF and C_{gd} = 27.2 pF.

Table 1. Parameters of the analytical turn off model.

Name	Value
Gate voltage V_{g_on}/V_{g_off} (V)	+18/−2
Gate resistor R_g (Ω)	3.8, 6.3, 8.7
Leakage inductor L_d (nH)	58
Gate capacitor C_{gs} (nF)	17.8
Threshold voltage V_{th_c} (V)	6.3
Tranconductance g_s (A/V^2)	5.9
DC bus voltage V_{dc} (V)	600
Q_{ds} at 600 V (nC)	1154.0
Q_{gd} at 600 V (nC)	138.2
C_{ds} at 600 V (nF)	2.2
C_{gd} at 600 V (pF)	27.2

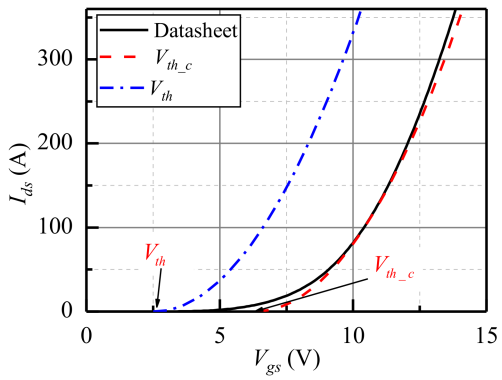

Figure 11. Improved approximation of the V_{gs}-I_{ds} transfer curve of the SiC MOSFETs.

5.2. Experimental Verification of Analytical Turn-Off Model

Based on the parameters in the table, the analytical model of the turn-off time of the SiC MOSFETs was calculated. Meanwhile, the single device double pulse test was conducted in the test platform. The switching waveform at 600 V/200 A is given in Figure 12. The voltage rising time was then measured from turn-off waveform. A set of experiments was conducted to measure the voltage rising time. The result is demonstrated in Table 2. At 600 V/200 A condition, the voltage rising time was measured at 3.8 Ω, 6.2 Ω, 8.7 Ω. Then, the calculated results from (9) were compared with experiments. It demonstrates that at the different turn-off gate driver resistor conditions, the voltage rising time matched well with the analytical model. The maximum error was −6.2%. There are several factors that contribute to the error. Firstly, the parameters of the actual device may have a slight difference from the datasheet. Secondly, the linear approximation of the gate-source voltage at the device turn off also contributes to the error. Moreover, the existing L_s still contributes to the voltage imbalance.

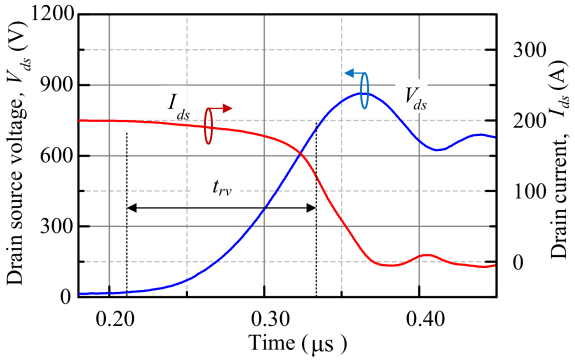

Figure 12. Turn off waveform at 600 V/200 A, R_g = 8.7 Ω.

Table 2. Comparison between t_{rv} model and the experiment.

	R_g = 3.8 Ω, 600 V/200 A	R_g = 6.2 Ω, 600 V/200 A	R_g = 8.7 Ω, 600 V/200 A
Model (ns)	53.8	79.0	102.6
Experiment (ns)	59.6	84.3	105.9
Absolute Error (%)	5.8	6.2	3.1

5.3. Experimental Verification of the VIS

VIS is defined as the value of voltage imbalance divided by the gate driver delay time. To measure the accurate *VIS* in the experiments, the gate drive signal was adjusted manually to get a gate driver time-delay and the voltage imbalance curve. In the experimental setup, the clock of the FPGA was 210 MHz, thus the accuracy of the delayed time was 4.8 ns minimum. Since the initial parameter deviation of the power devices remains unknown, a set of voltage imbalances under different delay times was measured.

As demonstrated in Figure 13, generally, the voltage imbalance changed linearly with the gate driver time delay. It should be noticed that when time delay equaled 0 ns, there was still a voltage imbalance due to the naturally existing uneven parameters among the device. The slope of the curve was linearly fitted as pictured. The comparison between the experiments and the model is given in Figure 13. At 6.2 Ω gate resistor and 1300 V bus voltage condition, the measured *VIS* at 200 A was 16.51 V/ns and 100 A was 14.84 V/ns. Accordingly, the calculated *VIS* was 16.59 V/ns and 14.21 V/ns. Then, the switching condition was changed to 11.2 Ω gate resistor and 1200 V/200 A condition. The experimental result was 9.77 V/ns and the model predicted 9.97 V/ns, as demonstrated in Table 3. Compared with the measured *VIS*, the error was below ±5%, which verifies the proposed *VIS* model.

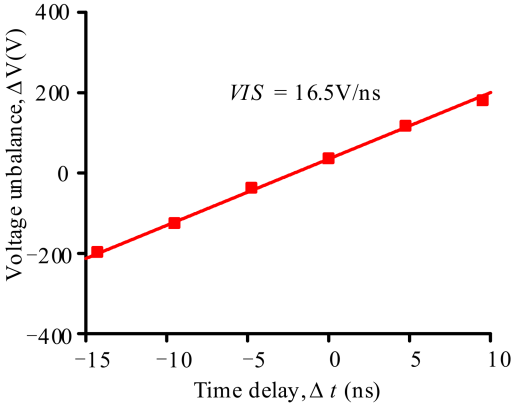

Figure 13. Relationship between the gate driver time delay and the voltage imbalance.

Table 3. Comparison between the VIS model and the experimental measurement.

	R_g = 6.2 Ω, 1300 V/200 A	R_g = 6.2 Ω, 1300 V/100 A	R_g = 11.2 Ω, 1200 V/200 A
Model (V/ns)	16.59	14.21	9.27
Experiment (V/ns)	16.51	14.84	9.77
Absolute Error (%)	0.4	4.3	5.0

Moreover, (18) is a simple equation to analyze the performance of the series-connected devices. Under some conditions, the parameters of the device cannot be acquired directly, the turn-off voltage rising time can still be measured with the help of the simple double pulse test, and the *VIS* of the series-connected devices can be acquired and adopted to assess the performance of the series connection.

5.4. Experimental Verification of the Close Loop Design

To verify the control loop design, a series of experiments was conducted in the experimental platform. At the beginning of the first switching cycle, 19.2 ns gate driver time delay was added to MOS_2, introducing an initial voltage imbalance in the circuit. Then, during each switching cycle, the turn-off steady-state drain-source voltage was sampled and sent to the central controller. With the parameter design method in Section 4, the experimental waveform is demonstrated in Figure 14.

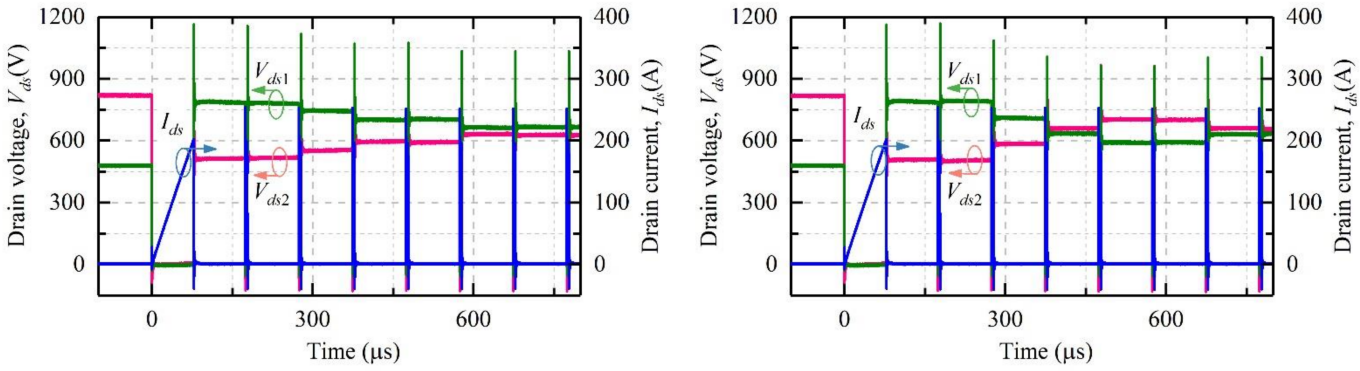

Figure 14. Experimental results of voltage balance control under 10 kHz pulse switching operations: (**a**) crossover frequency is 500 Hz; (**b**) crossover frequency is 1 kHz.

The experimental result demonstrates that after several switching cycles, the voltage imbalance caused by 19.2 ns delay was compensated. Figure 14a demonstrates the results at 500 Hz crossover frequency. There was no overshoot in the response curve. Figure 14b demonstrates the results at 1 kHz crossover frequency. There was a significant overshoot in the response. Both results reflect a stable voltage balancing response, which verifies the effectiveness of the proposed method. In addition, there was a relatively large voltage imbalance before the switching of the device. This is the result of the static voltage sharing, which is not discussed in this paper.

To further compare the proposed model with the experimental results, the comparison between the experimental results and calculated voltage response is given in Figure 15. The operation points were 1300 V/100 A and 1300 V/200 A. The waveforms of the two devices were measured and the voltage imbalances were calculated. The results demonstrate the transition of the voltage unbalance under the close loop control. Figure 15a,b is the response comparison at 500 Hz crossover frequency. Figure 15a is measured at 100 A load current and Figure 15b is measured at 200 A load current. The experimental results demonstrate

that after each switching cycle, the voltage imbalance decreased significantly and matched well with the calculated result based on the control loop diagram in Figure 6.

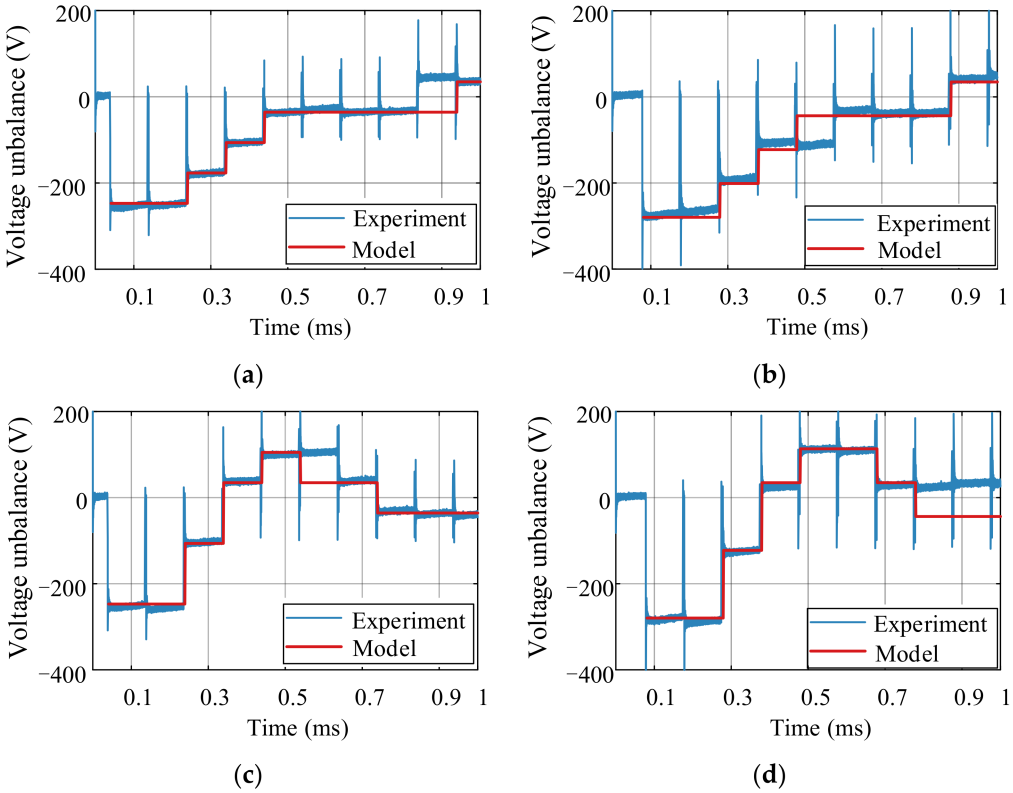

Figure 15. Measured imbalance voltage response compared with control model in Figure 7, at different operation points and crossover frequency of control loop: (**a**) 1300 V/100 A, crossover frequency is 500 Hz; (**b**) 1300 V/200 A, crossover frequency is 500 Hz; (**c**) 1300 V/100 A, crossover frequency is 1 kHz; (**d**) 1300 V/200 A, crossover frequency is 1 kHz.

To go one step further, another set of PI parameters was calculated at the 1 kHz crossover frequency. The result is demonstrated in Figure 15c,d. Since the crossover frequency increased and the time delay in the control loop was the same, the phase margin decreased and oscillation occurred in the response curve. The response curve matched well with the calculated results. In the engineering application of the series connection of SiC MOSFETs, the overshoot in the control loop is suggested to be limited to ensure the safe operation of the devices.

In the response curve, there was deviation in one or two switching cycles between the model and the experiment. There are two factors that contribute to the error. One is the error of the parameters of the device between the parameters in the datasheet and the reality. In addition, in each switching cycle, the load current is charged by the DC source during the on-state of the lower device. Thus, the load current increases a little bit after each switching cycle, which causes the variation of the *VIS* after each cycle and causes the error between the model and the experiment.

Although the voltage imbalance is greatly reduced under close loop control, there is still voltage imbalance at the end of the response curve. The reason is that the accuracy of the active delayed time is limited by the clock of the digital controller. Therefore, it is difficult to fully eliminate the voltage imbalance. It can be further improved by increasing the clock of the digital controllers properly or using a soft delay line that uses the build-in phase-locked loop (PLL) in FPGA to achieve time resolution larger than clock [23].

Above all, the experiment verifies the effectiveness of the proposed analysis and the control loop design. It is demonstrated that the voltage imbalance in the series-connected

device can be theoretically modeled and controlled, which supports the design of the voltage imbalance loop.

6. Conclusions

A quantitative close-loop design of the voltage balancing of the series connection of SiC power MOSFETs is proposed in this paper. The proposed analytical design method abandons the conventional experimental calibration with the help of an accurate mathematical model. To begin with, a turn-off model of SiC MOSFET considering the non-flat Miller plateau was proposed, which describes the turn-off behavior more accurately than the constant Miller plateau voltage approximation. Further, the voltage imbalance model of series connection was given based on the proposed turn-off model of the single SiC MOSFET. The model matches well with the experiments with an error less than $\pm 5\%$. It should be pointed out that the accuracy of the proposed control model depends on the difference between the parameters in the datasheet and the reality of the considered device. Better accuracy can be achieved with more accurate device parameters as inputs. Then, the active gate driving time delay control, which is the widely adopted method in series connection, was modeled with the proposed voltage imbalance model. The experimental results matched well with the theoretical prediction. The methodology proposed in this paper offers a theoretical model on voltage imbalance and can be adopted to design control parameters of other control methods of voltage balancing in the series connection of the SiC MOSFETs.

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References

1. Marzoughi, A.; Burgos, R.; Boroyevich, D. Investigating impact of emerging medium-voltage SiC MOSFETs on medium-voltage high-power industrial motor drives. *IEEE J. Emerg. Sel. Top. Power Electron.* **2019**, *7*, 1371–1387. [CrossRef]
2. Das, M.K.; Capell, C.; Grider, D.E.; Leslie, S.; Ostop, J.; Raju, R.; Schutten, M.; Nasadoski, J.; Hefner, A. 10 kV, 120 a SiC half H-bridge power MOSFET modules suitable for high frequency, medium voltage applications. In Proceedings of the 2011 IEEE Energy Conversion Congress and Exposition, Phoenix, AZ, USA, 17–22 September 2011; IEEE: Manhattan, NY, USA; pp. 2689–2692.
3. Bolotnikov, A.; Losee, P.; Permuy, A.; Dunne, G.; Kennerly, S.; Rowden, B.; Nasadoski, J.; Harfman-Todorovic, M.; Raju, R.; Tao, F.; et al. Overview of 1.2 kV–2.2 kV SiC MOSFETs targeted for industrial power conversion applications. In Proceedings of the 2015 IEEE Applied Power Electronics Conference and Exposition (APEC), Charlotte, NC, USA, 15–19 March 2015; pp. 2445–2452.
4. Song, X.; Huang, A.Q.; Zhang, L.; Liu, P.; Ni, X. 15 kV/40 A FREEDM super-cascode: A cost effective SiC high voltage and high frequency power switch. *IEEE Trans. Ind. Appl.* **2017**, *53*, 5715–5727. [CrossRef]
5. Vechalapu, K.; Bhattacharya, S.; Aleoiza, E. Performance evaluation of series connected 1700 V SiC MOSFET devices. In Proceedings of the 2015 IEEE 3rd Workshop on Wide Bandgap Power Devices and Applications (WiPDA), Blacksburg, VA, USA, 2–4 November 2015; IEEE: Manhattan, NY, USA, 2015.

6. Wang, R.; Liang, L.; Chen, Y.; Kang, Y. A single voltage-balancing gate driver combined with limiting snubber circuits for series-connected SiC MOSFETs. *IEEE J. Emerg. Sel. Top. Power Electron.* **2020**, *8*, 465–474. [CrossRef]
7. Ren, Y.; Yang, X.; Zhang, F.; Wang, K.; Chen, W.; Wang, L.; Pei, Y. A compact gate control and voltage-balancing circuit for series-connected SiC MOSFETs and its application in a DC breaker. *IEEE Trans. Ind. Electron.* **2017**, *64*, 8299–8309. [CrossRef]
8. Wu, X.; Cheng, S.; Xiao, Q.; Sheng, K. A 3600 V/80 A series–parallel-connected silicon carbide MOSFETs module with a single external gate driver. *IEEE Trans. Power Electron.* **2014**, *29*, 2296–2306. [CrossRef]
9. Xiao, Q.; Yan, Y.; Wu, X.; Ren, N.; Sheng, K. A 10 kV/200 A SiC MOSFET module with series-parallel hybrid connection of 1200 V/50 A dies. In Proceedings of the 2015 IEEE 27th International Symposium on Power Semiconductor Devices & IC's (ISPSD), Hong-Kong, China, 10–14 May 2015; IEEE: Manhattan, NY, USA, 2015.
10. Biela, J.; Aggeler, D.; Bortis, D.; Kolar, J.W. Balancing circuit for a 5-kV/50-ns pulsed-power switch based on SiC-JFET super cascode. *IEEE Trans. Plasma Sci.* **2012**, *40*, 2554–2560. [CrossRef]
11. Chen, X.; Chen, W.; Yang, X.; Han, Y.; Hao, X.; Xiao, T. Research on a 4000-V-ultrahigh-input-switched-mode power supply using series-connected MOSFETs. *IEEE Trans. Power Electron.* **2018**, *33*, 5995–6011. [CrossRef]
12. Zhang, F.; Yang, X.; Chen, W.; Wang, L. Voltage balancing control of series-connected SiC MOSFETs by using energy recovery snubber circuits. *IEEE Trans. Power Electron.* **2020**, *35*, 10200–10212. [CrossRef]
13. Yang, C.; Pei, Y.; Xu, Y.; Zhang, F.; Wang, L.; Zhu, M.; Yu, L. A Gate Drive Circuit and Dynamic Voltage Balancing Control Method Suitable for Series-Connected SiC mosfets. *IEEE Trans. Power Electron.* **2020**, *35*, 6625–6635. [CrossRef]
14. Baraia, I.; Barrena, J.A.; Abad, G.; Segade, J.M.C.; Iraola, U. An experimentally verified active gate control method for the series connection of IGBT/diodes. *IEEE Trans. Power Electron.* **2012**, *27*, 1025–1038. [CrossRef]
15. Lobsiger, Y.; Kolar, J.W. Closed-Loop di/dt and dv/dt IGBT Gate Driver. *IEEE Trans. Power Electron.* **2015**, *30*, 3402–3417. [CrossRef]
16. Dymond, H.C.P.; Liu, D.; Wang, J.; Dalton, J.J.O.; Stark, B.H. Multi-level active gate driver for SiC MOSFETs. In Proceedings of the 2017 IEEE Energy Conversion Congress and Exposition (ECCE), Cincinnati, OH, USA, 1–5 October 2017; IEEE: Manhattan, NY, USA, 2017.
17. Marzoughi, A.; Burgos, R.; Boroyevich, D. Active Gate-Driver With dv/dt Controller for Dynamic Voltage Balancing in Series-Connected SiC MOSFETs. *IEEE Trans. Ind. Electron.* **2019**, *66*, 2488–2498. [CrossRef]
18. Gerster, C.; Hofer, P.; Karrer, N. Gate-control strategies for snubberless operation of series connected IGBTs. In Proceedings of the PESC Record. 27th Annual IEEE Power Electronics Specialists Conference, Baveno, Italy, 23–27 June 1996; IEEE: Manhattan, NY, USA, 1996; Volume 2.
19. Gerster, C. Fast high-power/ high-voltage switch using series-connected IGBTs with active gate-controlled voltage-balancing. In Proceedings of the 1994 IEEE Applied Power Electronics Conference and Exposition-ASPEC'94, Orlando, FL, USA, 13–17 February 1994; pp. 469–472.
20. Ji, S.; Lu, T.; Zhao, Z.; Yu, H.; Yuan, L. Series-connected HV-IGBTs using active voltage balancing control with status feedback circuit. *IEEE Trans. Power Electron.* **2015**, *30*, 4165–4174. [CrossRef]
21. Parashar, S.; Bhattacharya, S. Active Voltage Balancing Methodology for Series connection of 1700V SiC MOSFETs. In Proceedings of the 2019 IEEE 7th Workshop on Wide Bandgap Power Devices and Applications (WiPDA), Raleigh, NC, USA, 29–31 October 2019; IEEE: Manhattan, NY, USA, 2019.
22. Wang, P.; Gao, F.; Jing, Y.; Hao, Q.; Li, K.; Zhao, H. An integrated gate driver with active delay control method for series connected SiC MOSFETs. In Proceedings of the 2018 IEEE 19th Workshop on Control and Modeling for Power Electronics (COMPEL), Padova, Italy, 25–28 June 2018; IEEE: Manhattan, NY, USA, 2018.
23. Wang, T.; Lin, H.; Liu, S. An Active Voltage Balancing Control Based on Adjusting Driving Signal Time Delay for Series-Connected SiC MOSFETs. *IEEE J. Emerg. Sel. Top. Power Electron.* **2020**, *8*, 454–464. [CrossRef]
24. Wang, J.; Chung, H.S.; Li, R.T. Characterization and experimental assessment of the effects of parasitic elements on the MOSFET switching performance. *IEEE Trans. Power Electron.* **2013**, *28*, 573–590. [CrossRef]
25. Chen, K.; Zhao, Z.; Yuan, L.; Lu, T.; He, F. The impact of nonlinear junction capacitance on switching transient and its modeling for SiC MOSFET. *IEEE Trans. Electron Devices* **2015**, *62*, 333–338. [CrossRef]
26. Roy, S.K.; Basu, K. Analytical estimation of turn on switching Loss of SiC MOSFET and Schottky Diode Pair from datasheet parameters. *IEEE Trans. Power Electron.* **2019**, *34*, 9118–9130. [CrossRef]
27. Li, C.; Lu, Z.; Chen, Y.; Li, C.; Luo, H.; Li, W.; He, X. High off-state impedance gate Driver of SiC MOSFETs for crosstalk voltage elimination considering common-source inductance. *IEEE Trans. Power Electron.* **2020**, *3*, 2999–3011. [CrossRef]
28. Baliga, B.J. *Fundamentals of Power Semiconductor Devices*; Springer: Cham, Switzerland, 2008.
29. Zeng, Z.; Li, X. Comparative study on multiple degrees of freedom of gate drivers for transient behavior regulation of SiC MOSFET. *IEEE Trans. Power Electron.* **2018**, *33*, 8754–8763. [CrossRef]
30. Zhang, Z.; Gui, H.; Niu, J.; Chen, R.; Wang, F.; Tolbert, L.M.; Costinett, D.J.; Blalock, B.J. High precision gate signal timing control based active voltage balancing scheme for series-connected fast switching field-effect transistors. In Proceedings of the 2018 IEEE Applied Power Electronics Conference and Exposition (APEC), San Antonio, TX, USA, 4 March 2018; IEEE: Manhattan, NY, USA, 2018.