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Parasitic Capacitance Effects on Active Clamp Flyback Output Characteristics: Application to IPOP Connection

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Abstract: Different mechanisms for balancing power between parallel connected modules have been presented in recent years. They have been broadly classified into active and passive methods. The high output impedance of topologies, including active clamp networks, suggests that they can achieve output current sharing passively when they are connected in parallel. However, some parasitic elements, such as stray capacitances and leakage inductances, have not been considered in the theoretical analyses. Moreover, these need to be taken into account when a high step-up ratio is required because they modify the behavior and output impedance of a module, which changes the current balance. This paper presents a detailed analysis of the influence of parasitic capacitances on active clamp flyback converters that were parallel connected, using the output impedance as a current self-balance method. The proposed solution to alleviate the negative effects on current balance was also studied and validated as a successful method that did not increase the complexity of the controller. Finally, the results that were obtained using an experimental prototype with two 100W modules helped to verify the theoretical results.

Keywords: DC–DC power conversion; active clamp flyback; parallel connected modules; current sharing; output impedance; high step-up voltage ratio

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1. Introduction

Systems that are based on DC–DC converters aim to obtain improved efficiency, high energy density and integration [1]. Improvements can be made when the overall system is split into modules or smaller subsystems that manage parts of the total power [2,3]. In that way, a scalable system can be produced, which, is more reliable as more identical modules can be added in order to achieve redundancy, which is easier to repair in the event of the failure of a module. To obtain the maximum benefits from the modular system, it is necessary for the different modules to manage the power equally [4]. Any differences between the modules, components or even the layout can cause differences in the power sharing; hence, it is a challenge to achieve an equal power distribution, which could otherwise lead to overloads in some of the modules and even the complete failure of the system. Therefore, the system must be provided with some sort of mechanism to ensure an equal power distribution.

When modules are input-parallel output-parallel connected (IPOP), which is the most popular connection [5], all of the modules have the same input and output voltages. Under this condition, the power balance mechanism focuses on the equal distribution of the current between the modules [6]. The use of the same duty cycle for all modules avoids its influence on load sharing, but current imbalance exists due to differences between module components [7]. Nonetheless, load sharing is feasible even in the presence of mismatches of 10% between various converter parameters.

Current sharing methods can be classified into active and passive methods [8,9]. In an active current sharing method, a module adjusts its own current using information from the

other modules. In this case, perfect current sharing and a good regulation of output voltage are achieved. Nevertheless, both additional circuitry and a dedicated current sharing control loop are needed, which leads to the higher complexity and lower reliability of the overall system. Recently, some efforts have been made to reduce the complexity of control techniques and improve efficiency in IPOP systems [10].

On the other hand, a passive method that is called the "droop" method is implemented by linearly reducing the DC output voltage as the output current increases, without the use of external information. It can be easily carried out by connecting a resistor to the module output. Even though it is so simple, the resistor adds losses into the system. Figure 1a shows the V–I output characteristics for two modules when resistors are connected to the outputs. It is represented assuming that the resistance, R_a and R_b, and the output voltage with no load, V_{01} and V_{02}, are different.

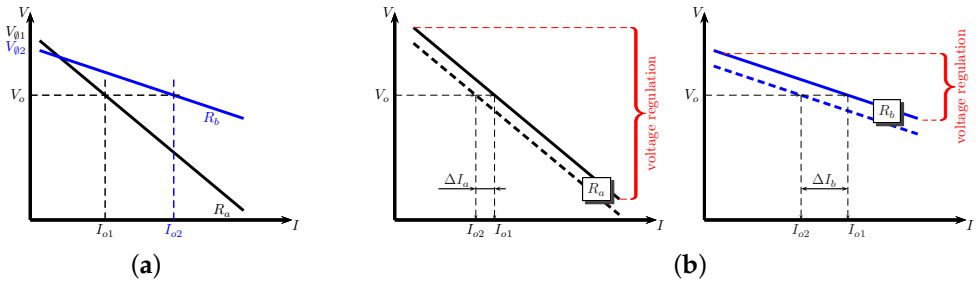


Figure 1. Output characteristics for two parallel connected modules with an added resistor at the output: (**a**) different values; (**b**) same values (R_a on the left and R_b on the right when $R_a > R_b$).

When modules are parallel connected, they have an equal output voltage (Vo), so each has a different output current (I_{o1} and I_{o2}). When both modules have the same added resistance, output characteristics can be obtained as shown in Figure 1b, in which it can be seen that current sharing depends on impedance. The smaller the difference between the elements, the better the current distribution and its effects can be minimized by increasing the slope, although the voltage regulation would become worse.

Another way to achieve this interdependency between voltage and current is through the existing control loop [11]. This behavior is a characteristic that can be found in some DC–DC topologies, such as resonant converters [12] that have high output impedances [13] or converters in discontinuous conduction mode (DCM) [14]. In these cases, the converter behaves as if it had a resistive element connected to its output, but without added losses.

Active clamp topologies [15] have high impedances [16,17], which makes them suitable for parallel connection and able to achieve passive current sharing within a modular system. In these topologies, zero voltage switching (ZVS) is possible under certain conditions, which reduces switching losses and improves converter efficiency. To extend the ZVS to lower power levels, an additional inductance is usually added.

After all of these considerations, the active clamp flyback (ACF) becomes a potential candidate for use as a module for an IPOP multiphase converter, through which the load sharing would be guaranteed without increasing the complexity of the control loop.

Nevertheless, the influence of the transformer must be taken into account, as it adds parasitic elements into the circuit and causes resonances with other elements. Moreover, when the transformation ratio is high, the resonances are magnified. The resonances can change the behavior of the converter [18] by modifying the expected current sharing.

Therefore, to improve current sharing in an ACF multiphase converter, the resonances must be minimized. Different approaches have been proposed: the RC–RCD snubber [19], which has the drawback of increasing losses; the inclusion of an additional diode to clamp the voltage and avoid resonances [20,21], although this has not been applied to a flyback; and the use of a voltage doubler for the integrated boost flyback topology [22]. In the last case, resonances are minimized and the transformation ratio is reduced. A similar solution has been used in an ACF topology as first stage of a solar micro-inverter design in [23].

In a previous paper [24], it was detected that the load sharing was not as good as existing models predicted. Resonances were identified as the cause, but were not modeled or analyzed in detail. In that paper, experimental results were obtained for the proposed solution that were based on the use of a diode to clamp the voltage, which showed a better current sharing between modules.

This paper deals with the reasons for bad current sharing in depth and demonstrates how minimal differences between parasitic capacitances have a great impact on power distribution. In this paper, we analyzed the following topics, which have not been studied before:

- Obtaining an analytical expression that relates the output voltage to the output current when there are no parasitic elements, i.e., the converter output characteristics, which show how modules can share the current and the effects of the tolerances;
- Obtaining the output characteristics, including the parasitic terms, and comparing them to data that were obtained using simulations (since they are based on parameters that are difficult to measure in practice);
- An in-depth analysis of the new topology using the clamp that was proposed in [24], which describes and studies the stages within a cycle;
- Obtaining an analytical expression of the output characteristics when the clamp diode is incorporated, including the parasitic elements, and its validation using simulations;
- Comparing the output characteristics when the clamp diode and parasitic elements are included to find the ideal configuration. Using this, it can be checked that they are quite close, even for large variations in the parasitic capacities.

The paper is organized as follows. In Section 2, the principles of the operation of an ACF and the effects of resonances in load sharing are explained. This section also includes how to obtain the analytical expression of the output characteristics, including the expression for when parasitic elements are incorporated. A modified topology to alleviate these effects is shown in Section 3. In Section 4, the experimental results are presented and our conclusions are reported in Section 5.

2. Analysis of Active Clamp Flyback Converter

ACF converters have been previously analyzed in [25] and the topology that was selected in this paper is shown in Figure 2. It comprises a main switch S_1 (which includes its body diode D_1), a magnetizing inductance L_m, with m being the transformer ratio and an output diode D_3. The active clamp network includes an auxiliary switch S_2 (which includes its body diode D_2) and a clamp capacitor C_c. An additional inductor L_r could be included to extend the ZVS for a wider load range. The parasitic components are also shown in the same figure: the transformer parasitic components L_{lk} and C_t and the junction capacitance of the output diode C_{D3}. A resonant capacitance C_r represents the parallel combination of the parasitic capacitances of the two switches.

To understand how the parasitic components affect the current sharing between power stages in steady-state conditions, we explored how the currents are distributed among simplified ideal converters and what happens when they are taken into account.

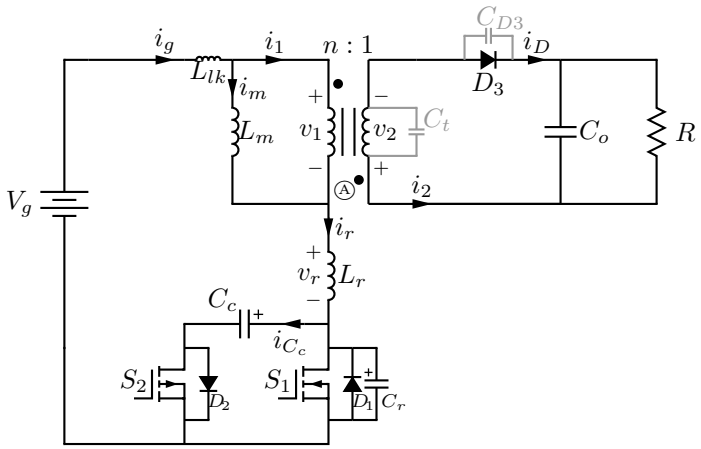


Figure 2. ACF converter with parasitic elements.

2.1. Load Sharing under Ideal Behavior

In Figure 3, the voltages to be applied to the magnetizing inductance and resonant inductor, $v_1(t)$ and $v_r(t)$, respectively, are represented for an ideal converter. Curves for the resonant inductor $i_r(t)$ when the converter is ideal (solid line) and when parasitic elements are considered (dashed line) are also included in the same figure.

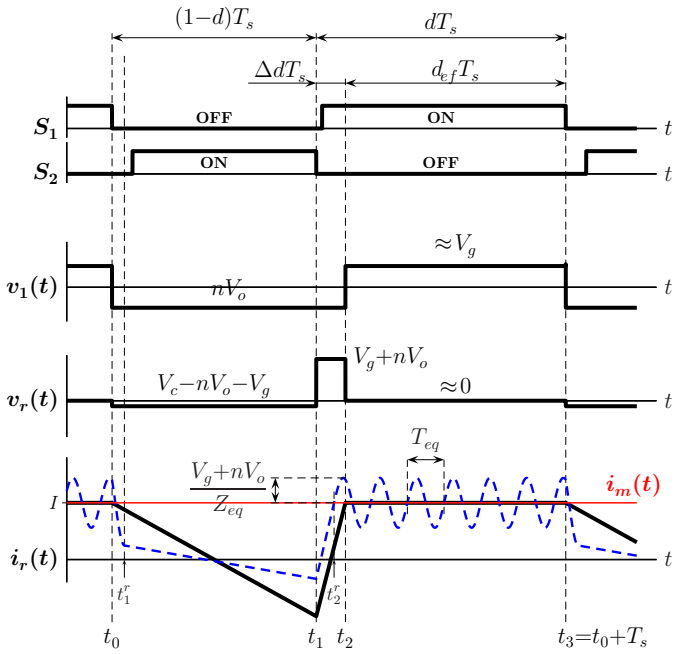


Figure 3. Main curves for circuit in Figure 2: $i_r(t)$ is plotted for the ideal case (solid) and when parasitic elements are included (dashed).

The following simplifications were made. The magnetizing inductance was high enough to consider a ripple-free magnetizing current $i_m(t)$ that was only compromised by its average value I, as can be seen in Figure. L_r was much less than L_m and the leakage inductance L_{lk} was assumed to be small enough to be included in L_r. The output and clamp capacitors were also high enough to have constant voltages V_o and V_c, respectively. On the other hand, the main and auxiliary switches were treated as ideal components. They operated in a complementary way with a constant duty cycle d. The circuit behavior could be divided into six time intervals over the switching period T_s. In the following description, three of them are neglected because they were short amounts of time and the resonant intervals were very fast at charging–discharging C_r. These operations are only cited when they took place.

- Time interval $[t_0, t_1]$: Prior to t_0, S_1 was on and the same constant current was passing through L_m and L_r and $i_r(t_0) = i_m(t_0) \approx I$. When the main switch was turned off at t_0, the resonant current charged C_r very quickly. After that, the current was directed to the clamp capacitor through the auxiliary diode D_2 and the auxiliary switch S_2 could be switched on at zero voltage. The output diode was forward-biased at this point and energy could be transferred to the output through the coupled inductors. The current $i_D(t)$ was identified as the reversed secondary side current $-i_2(t)$ and was related to the primary current $i_1(t)$ by a factor of n. On the other side, L_r and C_c exchanged energy in a resonant way. The resonant current became reversed and had a negative value $i_r(t_1)$ at the end of this interval.
- Time interval $[t_1, t_2]$: At t_1, S_2 was switched off and the resonant current evolved from $i_r(t_1)$, a negative value, into a positive value under constant voltage $V_g + nV_o$ for the majority of the time. Firstly, the resonant current helped to discharge C_r very quickly. Secondly, the resonant current flowed across D_1, thereby allowing a zero voltage switching of the main switch before $i_r(t)$ became a zero value. Finally, when $i_r(t)$ obtained a positive value, it flowed through S_1 until it matched to magnetizing current at t_2. The output diode was reverse-biased at this moment.
- Time interval $[t_2, t_3]$: From t_2 to the end of the switching period at $t_3 = t_0 + T_s$, the same current was passing through L_r and L_m, which increased their stored energy.

By applying the volt-second balance in L_m over the switching period, the output voltage V_o was derived as (1), considering Δd as the duty cycle variation. It was related to $(t_2 - t_1)$:

$$V_o = V_g \frac{d - \Delta d}{(1 - d + \Delta d)n} = V_g \frac{d_{ef}}{(1 - d_{ef})n} \tag{1}$$

The output voltage of the ACF seemed to be similar to the output voltage of the conventional flyback in CCM when the term $(d - \Delta d)$ was collected in a single term d_{ef}, which named the *effective duty cycle*. It was related to the time interval during which L_m was effectively charged.

The charge balance in C_c led to $i_r(t_1) = -I$. Then, an expression for Δd was deduced from the current variations in L_r at the time interval $[t_1, t_2]$ as (2). It revealed a direct dependence of duty cycle variation on the average value of the magnetizing current:

$$\Delta d = \frac{L_r \Delta i_r}{v_r T_s} = \frac{L_r[i_r(t_2) - i_r(t_1)]}{(V_g + nV_o)T_s} = \frac{L_r f}{V_g + nV_o} 2I \tag{2}$$

By combining Kirchhoff's current law in node A with the current ratio in the coupled inductors, (3) was obtained:

$$\left.\begin{array}{c} i_m(t) + i_1(t) = i_r(t) \\ i_D(t) = -n i_1(t) \end{array}\right\} \Rightarrow i_m(t) - \frac{1}{n} i_D(t) = i_g(t) \tag{3}$$

By averaging (3) over one switching period and assuming ideal components, the output current I_o and magnetizing current were related by (4). Then, Δd depended on the output current in (5):

$$I - \frac{I_o}{n} = \frac{V_o I_o}{V_g} \tag{4}$$

$$\Delta d = \frac{L_r f}{n V_g} 2 I_o \tag{5}$$

The last expression indicated that when the output current became higher, Δd increased. Therefore, at a constant duty cycle value, the output voltage decreased when

the output current increased. It looked as though a lossless resistance was placed at the converter output. Nevertheless, this dependence came from the existence of additional elements, which managed a portion of the processed energy even though it passed to the output. As more output power was required, more time to manage the stored energy was also needed.

The relationship between the duty cycle, output current and output voltage (6) could be deduced by combining (5) and (1):

$$V_o = \frac{V_g \frac{d}{(1-d)n} - I_o \frac{2L_r f}{(1-d)n^2}}{1 + I_o \frac{2L_r f}{(1-d)nV_g}} \tag{6}$$

The output impedance was obtained from the derivation of (6) with respect to I_o. A more compact expression could be deduced when I_o was isolated from (6) and introduced into the new expression, as shown in (7):

$$\frac{dV_o}{dI_o} = -\frac{\frac{2L_r f}{(1-d)^2 n^2}}{\left[1 + I_o \frac{2L_r f}{(1-d)nV_g}\right]^2} = -2L_r f \left[\frac{V_g + nV_o}{nV_g}\right]^2 \tag{7}$$

It revealed that the output impedance in steady-state conditions depended on L_r and the input and output voltages, but there was no dependence on the duty cycle. Moreover, when N ideal ACF modules were parallel connected and used the same duty cycle, the output current for the k stage $I_{o,k}$ depended on every resonant inductor, as stated in (8):

$$I_{o,k} = I_o \Big/ \sum_{i=1}^{N} \left(\frac{L_{r,k}}{L_{r,i}}\right) \tag{8}$$

2.2. Introducing the Effects of Parasitics

When parasitic capacitances were considered, L_r exchanged energy with them in a resonant way after D_3 was switched off. The resonances modified the behavior of the converter and also affected the duty cycle variation Δd. To bring together C_t and C_{D3} on the primary side, an equivalent capacitance C_{eq} was defined as (9). A high turn ratio contributed toward enlarging its value:

$$C_{eq} = \frac{C_t + C_{D3}}{n^2} \tag{9}$$

The resonant current could be expressed as (10) during time interval $[t_2, t_3]$, which is shown by the dashed line in Figure 3:

$$i_r(t) = I + \frac{V_g + nV_o}{Z_{eq}} \sin \omega_{eq} t \tag{10}$$

where

$$Z_{eq} = \sqrt{L_r / C_{eq}} \quad \text{and} \quad \omega_{eq} = 1/\sqrt{L_r C_{eq}} \tag{11}$$

Two remarkable instants of time should be cited here. After S_2 was opened, the point in time where the resonant current $i_r(t)$ equaled the $i_m(t)$ changed from t_2 to t_2^r and the point at which the voltage in C_{eq} reached $-nV_o$ using part of the current that was stored in L_r was stated at t_1^r. The output diode D_3 was forward-biased at the same time.

It must be stressed that the current at instant t_1 depended on the current at t_1^r, which in turn depended on the current at t_0. However, $i_r(t_0)$, as a consequence of the high value of ω_{eq}, presented large variations, although C_{eq} only changed slightly.

By analyzing the current over the new intervals, the duty cycle variation under resonances $\Delta^r d$ was obtained using (12):

$$\begin{aligned}\Delta^r d = &-\frac{(V_g+nV_o-V_c)}{(V_g+nV_o)}d_1^r - \frac{L_r f}{Z_{eq}}\sin\left[(w_{eq}(d_0^r+d_{ef}^r)T_s\right] \\ &+\frac{V_c L_r f}{(V_g+nV_o)Z_{eq}}\sin(w_{eq}d_0^r T_s)\end{aligned} \tag{12}$$

where $d_0^r T_s = (t_1^r - t_0)$, $d_1^r T_s = (t_1 - t_1^r)$ and $d_{ef}^r T_s = (t_3 - t_2^r)$ are the time intervals and the clamp voltage in C_c is $V_c = V_g/(d_0^r + d_1^r)$.

By the charge balance at C_{eq} and C_c, some relationships between the intervals were obtained:

$$\cos\left[\omega_{eq}(d_0^r+d_{ef}^r)T_s\right] = 1 + \frac{V_c\left[\cos(\omega_{eq}d_0^r T_s)-1\right]}{(V_g+nV_o)} \tag{13}$$

$$\begin{aligned}&I(d_0^r+d_1^r) + \left[\cos(\omega_{eq}d_{ef}^r T_s)-1\right]\frac{(V_g+nV_o)}{Z_{eq}w_{eq}T_s} \\ &-(V_g+nV_o)\frac{d_1^r T_s \Delta^r d}{L_r} - \frac{d_1^r T_s}{2L_r}(V_g+nV_o-V_c) = 0\end{aligned} \tag{14}$$

The uncontrollable nature of C_{eq} resulted in nearly random changes in $\Delta^r d$ because it depended on the time intervals. They were interrelated with the circuit parameters, as is stated in the latter expressions.

It was very useful to show how the parasitic capacitances influence the output voltage–current relationship. A procedure to obtain the paired values of output voltage and output current was developed. An equation system comprising (12) and (13) mhad to be solved to obtain d_0^r and d_{ef}^r values. Then, the output current value was calculated by combining (4) and (14).

2.3. Output Characteristic Curves

The output characteristics of the ideal case (6) is plotted in Figure 4a using the parameters that are included in Table 1. The ideal duty cycle was obtained by adding two terms: the effective duty cycle derived from (1) and the duty cycle variation in (5), considering an output current of 0.25 A. In this way, $d_{ef} = 0.625$, $\Delta d = 0.06$ and $d = 0.685$.

Table 1. Active clamp flyback parameters that were used to obtain the curves in Figure 4.

Parameters for the Output Voltage to Output Current Curves		
$V_g = 20$ V	$C_o = 5$ µF	n_1:n_2 = 1:12
$V_o = 400$ V	$C_c = 2.2$ µF	$L_m = 24$ µH
$f = 100$ kHz	$C_r = 1$ nF	$C_f = 45$ pF
$t_m = 100$ ns	$L_r = 2$ µH	$C_t =$ 60 pF, 63 pF and 70 pF

Using the same parameters and duty cycles as the ideal case, the paired values $V_o - I_o$ were determined using the method that was described in the previous section when the parasitic capacitances were taken into account. The curves for 60 pF and 63 pF (a five percent variation) are shown in the same Figure while $C_f = 45$ pF. This method was repeated with duty cycle values of 0.6 and 0.65 and the curves were added to the same graph. The computer simulations of ACF with the parasitic elements showed a good agreement with the numerical calculations, as shown in Figure 4b.

As can be seen in all of the plotted curves, the output voltage generally decreased when the output current increased as an output impedance behavior. While a monotonous decreasing trend of the output impedance was observed in the represented ideal curve, when the parasitic capacitances were included, the output impedance evolved in a different

way: it increased and decreased based upon the output voltage levels. For example, the slope of the curve was nearly flat at the output voltage around 300 V, regardless of the duty cycle value. A higher slope was also observed when the voltage was taken beyond or below this value for the same curves. The curves showed that a change in duty cycle did not alter the tendency for non-ideal curves but did produce a displacement.

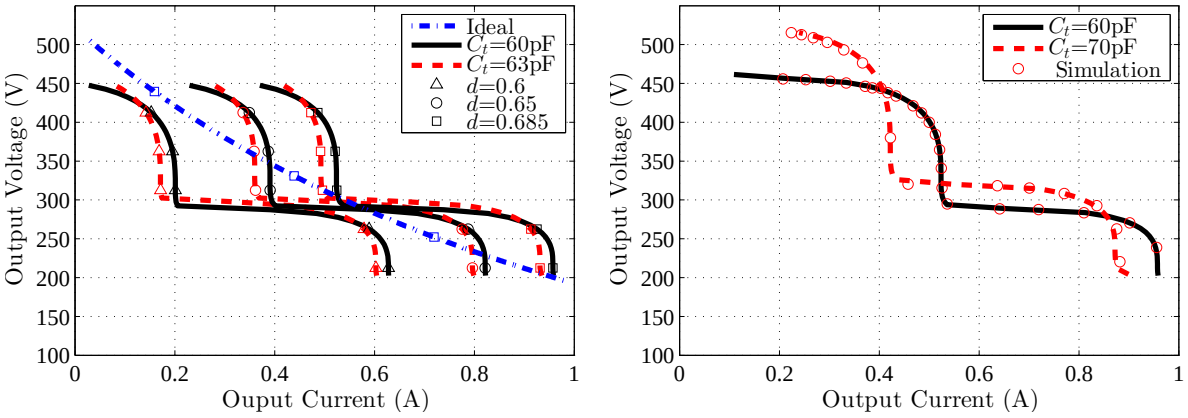


Figure 4. Output voltage to output current curves for the circuit in Figure 2: (**a**) ideal case (dash-dot line) and considering two values for parasitic capacitances (solid and dashed lines) when different duty cycles (triangle, circle and square markers) were used; (**b**) comparison between the numerical results and the data obtained from computer simulations for the two parasitic capacitances.

Another interesting phenomena was the high sensitivity to parasitic capacitances in the same duty cycle. As depicted in Figure 4, a five percent variation in C_t value was enough to cause a displacement in the output characteristics, while sustaining the output impedance trend. In this case, C_t was chosen but the same effects were observed when C_{D3} was selected.

3. Enhanced ACF Topology

The proposed solution in this paper employed an unique diode D_4 to eliminate the resonances. This diode was considered to be ideal with no voltage drops. It was placed on the primary side between node A and the ground, as shown by the dashed line in Figure 5. The whole topology was an enhanced active clamp flyback (EACF). The added junction capacitance C_{D4} had a minor influence on the new circuit, but the voltage was fixed at a constant value after S_1 was turned on and the output impedance had a similar variation to the ideal case in Section 2.3. This solution was feasible because the resonant inductor was included in the ACF topology. When L_r was not required, ringing between the parasitic capacitances and the leakage inductance could be mitigated, as exposed in [22].

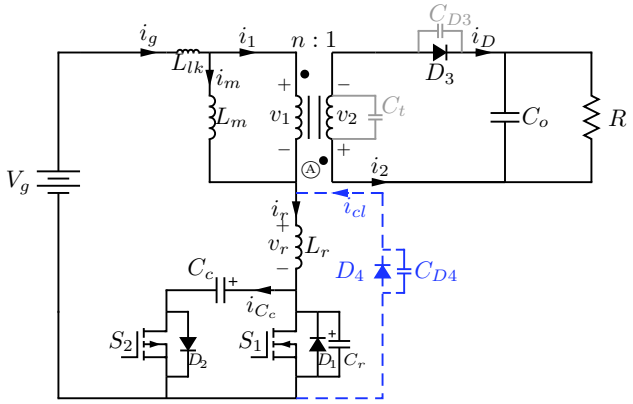


Figure 5. Enhaced ACF converter with parasitic elements and the proposed clamp (dashed line).

3.1. Operating Principles

Prior to the present operation of the EACF, the parasitic capacitances C_{D3} and C_t and the capacitance of the new diode C_{D4} were merged into C_{cl} and were fitted instead of C_4, which had a value of (15):

$$C_{cl} = C_{eq} + C_{D4} \tag{15}$$

One switching period was divided into ten time intervals and the equivalent circuits of the EACF during each time interval are shown in Figure 6. The converter operated in continuous conduction mode (CCM) and the magnetizing inductance was high enough to consider a ripple-free current with a value of $i_m(t) \approx I$. The leakage inductance L_{lk} was included into the resonant inductor L_r. The output and clamp capacitors were also high enough to have constant voltages V_o and V_c, respectively. The main and auxiliary switches were treated as ideal components. They operated in a complementary way with a constant duty cycle d.

The time intervals were detailed as follows:

- Time interval 1 $[t_0, t_0^{cc}]$ (Figure 6a): Prior to t_0, the same current flowed through L_r and S_1. It comprised the magnetizing current I and the current from the diode D_4 branch I_{D_c}. The main switch was turned off at t_0 and the resonant current rapidly charged C_r until its voltage reached V_c.
- Time interval 2 $[t_0^{cc}, t_0^e]$ (Figure 6b): After charging C_r, the resonant current was redirected to C_c through the auxiliary diode D_2. L_r exchanged energy with the clamp capacitor while the current decreased linearly to arrive at the value of I at t_0^e. At this point, the current through D_4 became zero and D_4 was off.
- Time interval 3 $[t_0^e, t_1^e]$ (Figure 6c): The resonant current decreased through capacitors C_c and C_{cl} until the voltage in C_{cl} reached $V_g + nV_o$ at t_1^e. At this moment, D_3 was forward biased.
- Time interval 4 $[t_1^e, t_{\text{neg}}^{ir}]$ (Figure 6d): Once D_3 started to conduct, energy was transferred to the output and the voltage that was applied to the resonant inductor became a negative value $V_g + nV_o - V_c$. Then, the resonant current was flowing through D_2 and decreased linearly until it reached zero value. To achieve the zero voltage switching of the auxiliary switch S_2, it was necessary to turn on the transistor before the end of this interval, i.e., while its body diode D_2 was conducting.
- Time interval 5 $[t_{\text{neg}}^{ir}, t_1]$ (Figure 6e): During this interval, $i_r(t)$ circulated through the main body of S_2 until S_2 was switched off at t_1. The resonant current decreased from zero to a negative value of $I_{r1} = i_r(t_1)$.
- Time interval 6 $[t_1, t_1^{dc}]$ (Figure 6f): During this short time interval, the resonant current helped to discharge C_r very quickly to zero voltage and $i_r(t)$ barely changed its value.
- Time interval 7 $[t_1^{dc}, t_{\text{pos}}^{ir}]$ (Figure 6g): During this interval, the resonant current initially flowed across D_1. It evolved from a negative value into a zero value under the constant voltage $V_g + nV_o$. To achieve the zero voltage switching of S_1, it was required to turn on the transistor before the end of this interval.
- Time interval 8 $[t_{\text{pos}}^{ir}, t_2^e]$ (Figure 6h): The resonant current evolved from a zero value into a positive value under the constant voltage $V_g + nV_o$ and it circulated through the main body of S_1 until t_2, at which point the resonant and magnetizing current equaled I. The output diode was reverse-biased.
- Time interval 9 $[t_2^e, t_3^e]$ (Figure 6i): The energy that was stored in C_{cl} during interval 3 was returned to L_r in a resonant form, which led to a current increment that was equal to I_{D_c} at the final instant t_3^e.
- Time interval 10 $[t_3^e, t_3]$ (Figure 6j): From t_3^e to the end of the switching period at $t_3 = t_0 + T_s$, the same current was passing through S_1 and L_r. The energy that was stored in L_m and L_r increased at the same time.

The expressions for the currents and voltages were obtained and the main theoretical curves are represented in Figure 7. It is worth noting that the point in time at which

the resonant current equaled the magnetizing current changed from t_2^r (or t_2 under ideal behavior) to t_2^e. The point at which the voltage in C_{cl} reached $V_g + nV_o$ was also stated at t_1^e. The output diode D_3 was forward-biased during these two instants.

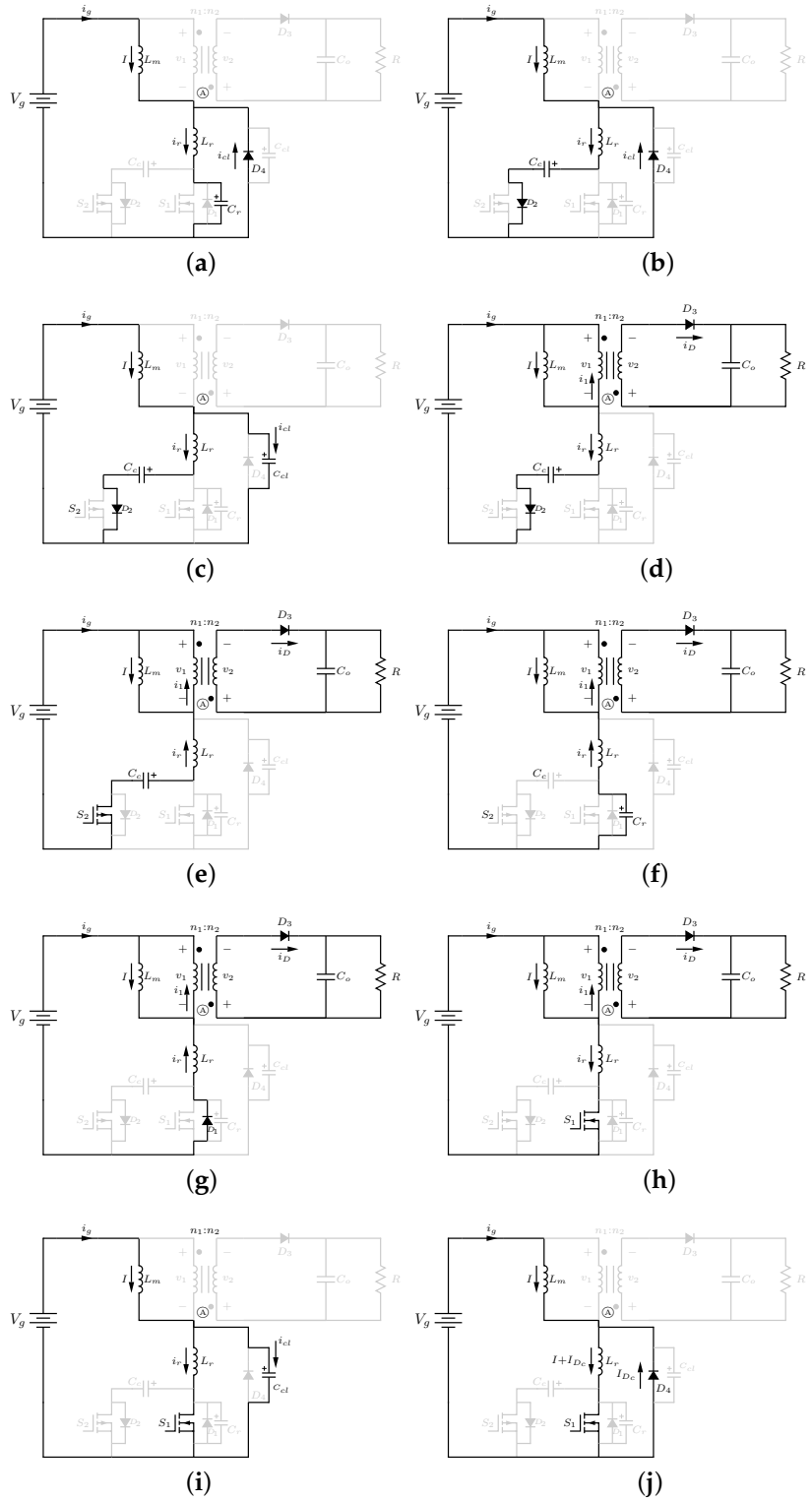


Figure 6. Equivalent circuits of the EACF during a switching period: (**a**) time interval 1; (**b**) time interval 2; (**c**) time interval 3; (**d**) time interval 4; (**e**) time interval 5; (**f**) time interval 6; (**g**) time interval 7; (**h**) time interval 8; (**i**) time interval 9; (**j**) time interval 10. The capacitance C_{cl} represents all of the parasitic capacitances.

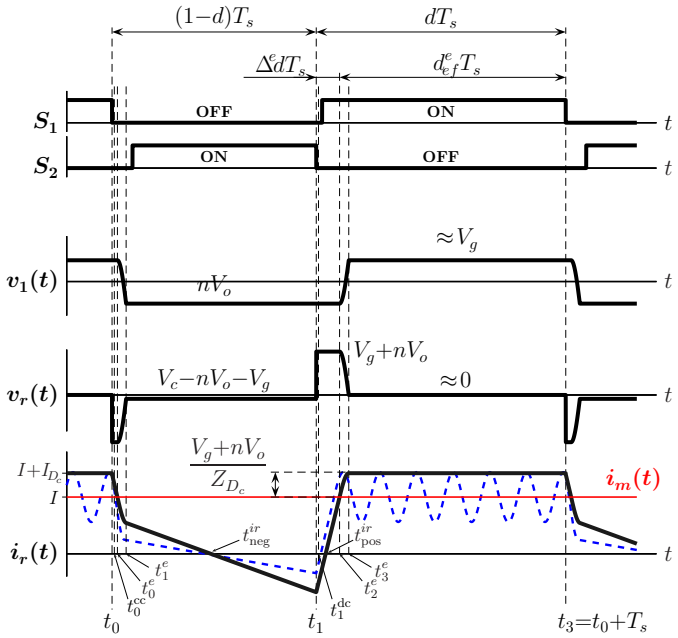


Figure 7. Main theoretical waveforms of the EACF topology. The resonant current $i_r(t)$ is plotted for the enhanced topology by the solid line and for the ACF with parasitics by the dashed line.

3.2. Steady-State Analysis

The relationship between the current and output voltage could be obtained from the steady-state analysis. Prior to that, it was necessary to calculate the duration the intervals. Time intervals 1 and 6 were neglected due to their short durations.

By using the volt-second balance in the magnetizing and resonant inductors, the clamp voltage in C_c was derived as:

$$V_c = \frac{V_g}{d^e_0 + d^e_{ch} + d^e_1} = \frac{V_g}{1-d} \tag{16}$$

where $d^e_0 T_s = (t^e_0 - t_0)$, $d^e_{ch} T_s = (t^e_1 - t^e_0)$ and $d^e_1 T_s = (t_1 - t^e_1)$ are the time durations for the second, third and fourth intervals, respectively.

From the equivalent circuit for the third interval, as shown in Figure 8a, the charging time of C_{cl} could be derived using the knowledge that the voltage at the end of this stage was $v_{C_{cl}}(d^e_{ch} T_s) = V_g + nV_o$. Then, the voltage expression was indicated as (17):

$$v_{C_{cl}}(t) = V_c(1 - \cos \omega_{D_c} t) \tag{17}$$

where

$$Z_{D_c} = \sqrt{L_r / C_{cl}} \quad \text{and} \quad \omega_{D_c} = 1/\sqrt{L_r C_{cl}} \tag{18}$$

Then:

$$\cos w_{D_c} d^e_{ch} T_s = 1 - \frac{V_g + nV_o}{V_c} \tag{19}$$

Alternatively, for the equivalent circuit in Figure 8b, the discharging time of C_{cl} and its final current could be derived.

The voltage and current were expressed by expressions (20) and (21), respectively.

$$v_{C_{cl}}(t) = (V_g + nV_o) \cos \omega_{D_c} t \tag{20}$$

$$i_{C_{cl}}(t) = -\frac{V_g + nV_o}{Z_{D_c}} \sin \omega_{D_c} t \tag{21}$$

Assuming that C_{cl} was discharged at the end of this interval, the duration time denoted by $d_d^e T_s$ became as in (22). The final current I_{D_c} was deduced using (23) when a zero initial current was considered at the beginning:

$$d_d^e T_s = \frac{\pi}{2\omega_{D_c}} \tag{22}$$

$$I_{D_c} = \frac{V_g + nV_o}{Z_{D_c}} \tag{23}$$

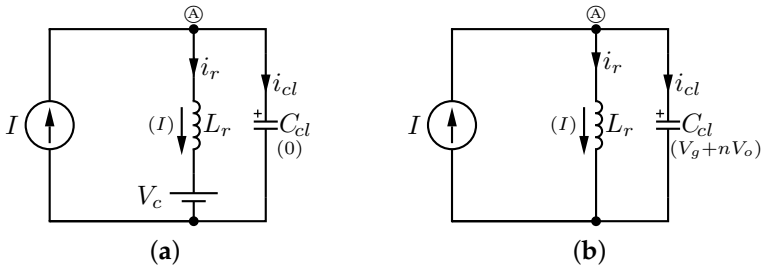


Figure 8. Equivalent circuits: (**a**) during time interval 3; (**b**) during time interval 9. The initial conditions are in parentheses.

During the second interval, variations in the resonant current under a constant voltage V_c was accorded to I_{D_c}. Then:

$$d_0^e T_s = \frac{I_{D_c}}{V_c} L_r = \frac{(V_g + nV_o)}{Z_{D_c} V_c} L_r \tag{24}$$

Knowing that $i_r(t_2^e)$ and $i_r(t_0^e)$ were both I, a relationship between d_{ch}^e, d_1^e and d_2^e was obtained:

$$\frac{V_c}{\omega_{D_c} T_s} \sin \omega_{D_c} d_{ch}^e T_s = (V_g + nV_o)(d_1^e + d_2^e) - V_c d_1^e \tag{25}$$

3.3. Output Characteristic Curves

The relationship between the output voltage and output current (26) was obtained by combining the charge balances in C_c and (4):

$$I_o = \left[-\frac{V_c}{2L_r f}(d_0^e)^2 + \frac{I_{D_c} f}{\omega_{D_c}} + d_1^e \frac{V_c}{Z_{D_c}} \sin \omega_{D_c} d_{ch}^e T_s - \frac{(V_g + nV_o - V_c)}{2L_r f}(d_1^e)^2 \right] \times \frac{nV_g}{(1-d)(V_g + nV_o)} \tag{26}$$

This curve is plotted in Figure 9 using the parameters that are included in Table 1 for a nominal output current of 0.25 A. The duty cycle was the solution for (26) after replacing the clamp voltage and time intervals as a function of d. The resulting value was $d = 0.6582$. Then, the output current values could be determined for every output voltage, while maintaining the duty cycle but recalculating the time intervals for the new output voltages.

In the same figure, the plot for a different value for C_t is shown, which employed the same procedure but preserved the duty cycle. This comparison was interesting because identical duty cycles are used in parallel connected modules. Both curves were validated by the computer simulations. On the other hand, the output characteristics for the ideal ACF in Figure 4 were also included in order to compare the curves. It could be observed that:

- Regarding the real ACF curves, there was an important difference when the clamp diode was employed. Horizontal zones did not appear for the EAC when the parasitics were considered, which was an advantage when equal load sharing was required;

- The EACF curves were slightly affected by substantial changes in the parasitic capacitances. Then, load sharing was feasible independently of the parasitics because of its minor influence;
- The EACF curves had similar trends to those of the ideal ACF. Nevertheless, the duty cycle was different, although the operation parameters were identical. Moreover, for the enhanced topology, a smaller duty cycle was required to reach the same output voltage and current.

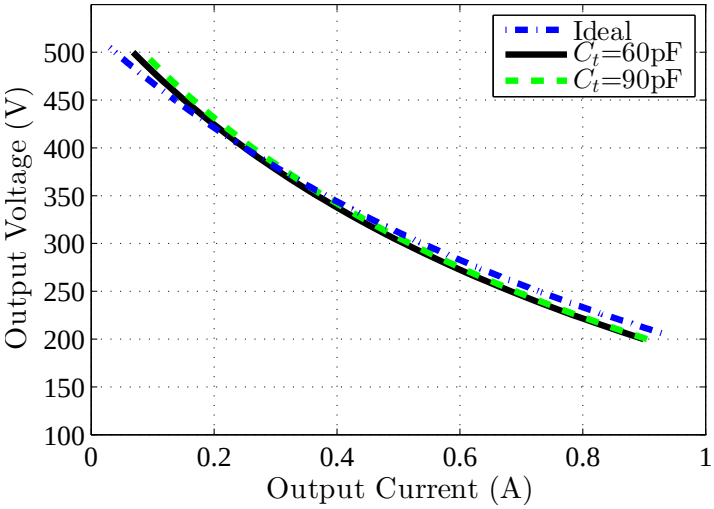


Figure 9. Output voltage to output current curve for EACF using the selected values for parasitic capacitance C_t ($d = 0.6582$) and ACF ($d = 0.685$).

4. Experimental Results

A laboratory prototype was built to verify the theoretical conclusions that were drawn in the previous sections. The prototype included two stages that were connected in parallel, as indicated in Figure 10, which shared the output capacitor. The prototype can be seen in Figure 11 and the main components are listed in Table 2. A TMS320F28027 microcontroller was employed to generate the PWM. Both stages were interleaved and shared the same duty cycle. Each stage was designed according to the specifications in Table 1. In order to check how the current sharing was affected by L_r, different values were tested.

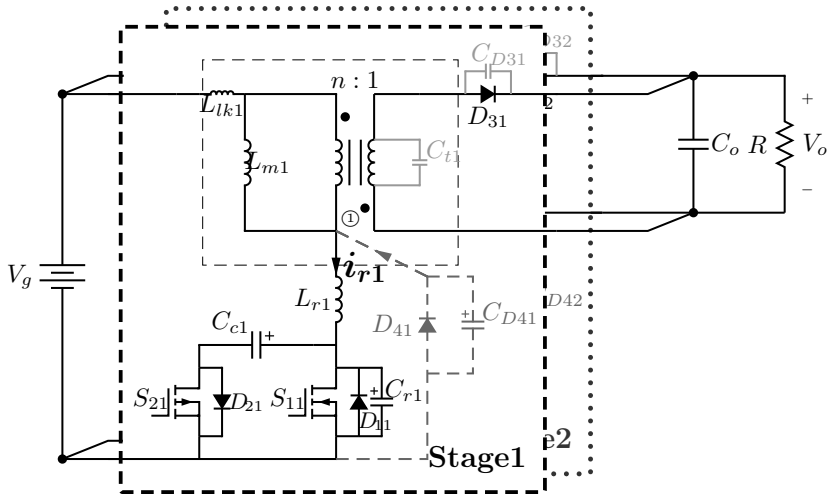


Figure 10. Connection diagram of the prototype that was formed of two stages in parallel.

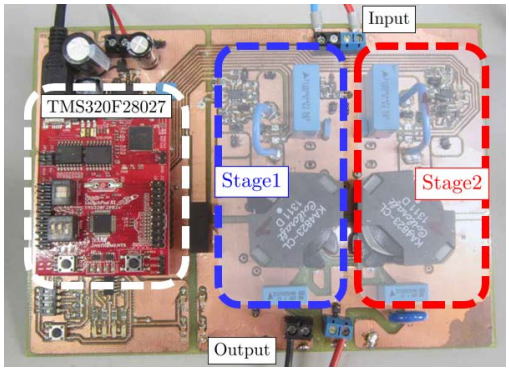


Figure 11. Prototype with two parallell connected (IPOP) ACFs and a microcontroller.

Table 2. Main components that were used in the prototype.

Components	Value-Reference	Description
MOSFET S_1	IRFS4321	N-channel 150 V; 11.7 mΩ@V_{GS} = 10 V
MOSFET S_2	IRF6218S	P-channel −150 V; 150 mΩ @V_{GS} = −10 V
MOSFET Driver	MCP14E4	4.0 A Dual H-Speed MOSFET Driver
Diode D_3	C4D05120E	SiC Schottky; 1200 V, 9 A
Diode *clamp* D_{cl}	MUR420	Ultrafast; 200 V, 4 A
Coupled Inductors	Coilcraft KA-4823CL	1:12; 28 µH; 8 mΩ DCR@L_{lk} = 0.115 µH
Resonant Inductor L_r	Coilcraft SER2010-102L	1 µH; 0.9 mΩ DCR
	Coilcraft SER2010-202L	2 µH; 0.9 mΩ DCR
Clamp Capacitor C_c	2.2 µF	250 V
Output Capacitor C_o	0.1 µF	630 V
Input Capacitor C_{in}	10 µF + 2.2 nF	63 V

It was stated that theoretically EACF topologies have nearly the same output characteristics, i.e., for the same output voltage, they have nearly the same output current. In the other way, converters without clamp diodes cannot follow the same trend and the current sharing becomes worse in some regions of the I–V curve. To check this hypothesis, the voltage and current at the output were measured for both stages of the prototype when D_4 was included and when it was not. The measurements are graphically represented and compared in Figure 12a,b.

It must be noted that neither selection of passive components to minimize mismatches nor the identical printed circuit board design for each stage had been developed during the implementation stage of the prototype.

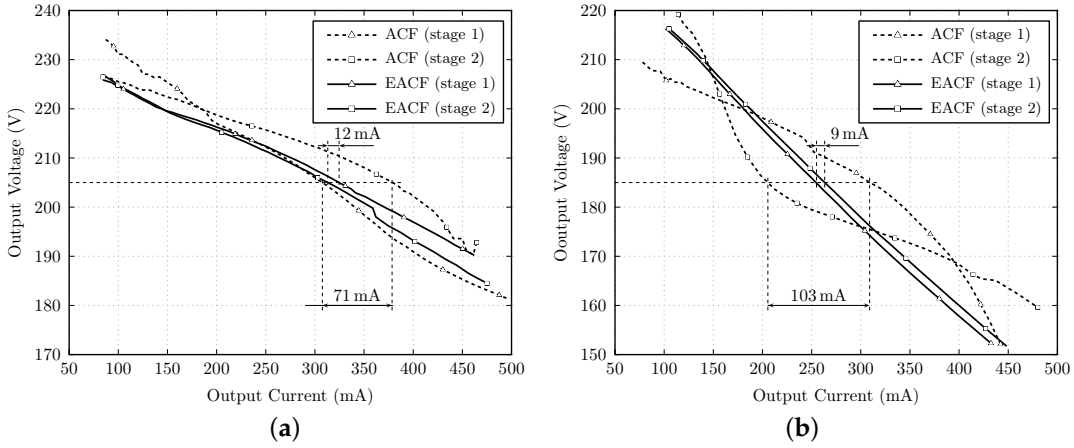
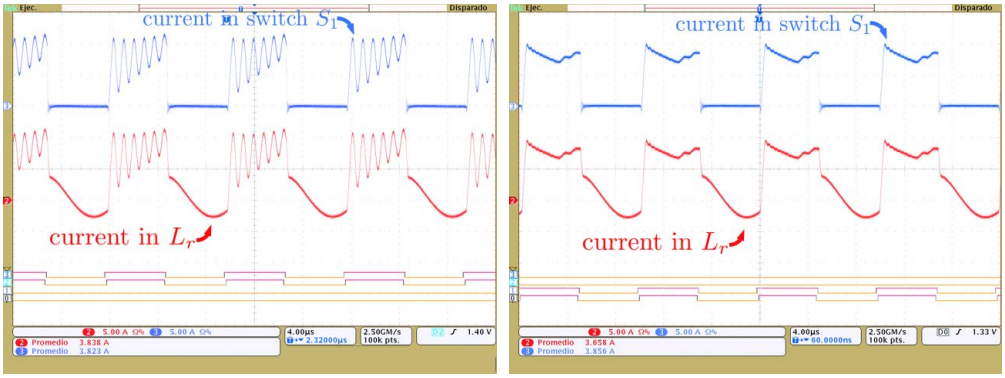


Figure 12. Experimental output voltage to output current curves for stages 1 and 2 in the ACF topology (dotted line) and EACF topology (solid line) for different values of the resonant inductor: (**a**) $L_r = 1$ µH; (**b**) $L_r = 2$ µH.

In all of the experiments, the output voltage decreased as the load increased, which implied that the converter exhibited an output impedance behavior. Nevertheless, the ACF stages presented substantial differences that could have led to a noticeable current imbalance. For example, the selection of $L_r = 1\,\mu H$ for the output voltage of 205 V led to a current imbalance, without the clamp diode, of 71 mA over a total current of 686 mA. The current imbalance decreased to 12 mA over 637 mA when the clamp diode was introduced.

When a higher value for the resonant inductor was selected, the output impedance increased, as established in (7), and the current sharing was improved. This was only true for the EACF topology, but it was not be true for the ACF topology because the resonances altered the converter behavior and the output impedance increased or decreased depending on the region. Again, the measurements validated these findings, as shown in Figure 12b, where L_r is 2 µH. A current difference of 9 mA was measured for the EACF but the difference for the ACF became worse, up to 103 mA. In this case, an output voltage of 185 V was chosen.

The resonances in $i_r(t)$ and $i_{S1}(t)$ appeared when no clamp diode was used, as can be seen in Figure 13a. When it was introduced, both resonances were mitigated, as can be seen in Figure 13b.



(**a**) (**b**)

Figure 13. Current in L_r and current in main switch S_1: (**a**) Ccurves for the real ACF; (**b**) curves for the EACF. The value for the resonant inductor was $L_r = 1\,\mu H$ in both experiments.

We noticed that when the main switch was closed (time interval 10), the currents did not evolve as expected. They resembled an inverted triangle. This difference was a consequence of the assumption of an ideal clamp diode in the theoretical analysis. In the laboratory, the forward voltage drop of the diode forced a slight decrease in the resonant current until $i_r(t)$ equaled $i_m(t)$. After that, the current increased again until the end of the time interval. Nevertheless, although the current in the resonant inductors could be seen for the two stages that the EACF interleaved, the load sharing was not affected, as can be seen in Figure 14. It could be checked both for similar shapes and values, according to a good current sharing in steady-state conditions.

As the ZVS condition stage depended on the managed power, the number of active stages could be a function of the output power. Then, the stages could be switched on or off to ensure zero voltage switching (ZVS) in a higher power range.

This mechanism was tested to check how the current sharing and converter behavior was affected. A good dynamic current balance was observed when stage2 was turned off, as shown in Figure 15, and when stage 2 was turned on, as shown in Figure 16. During both transients, the controller set up the converter in the new steady-state conditions without any additional mechanisms to preserve the individual currents in the stages. Finally, the efficiency was measured and was close to 94 % for a wide load range.

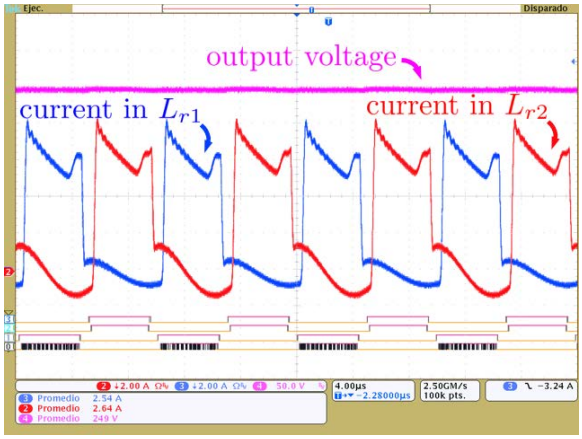
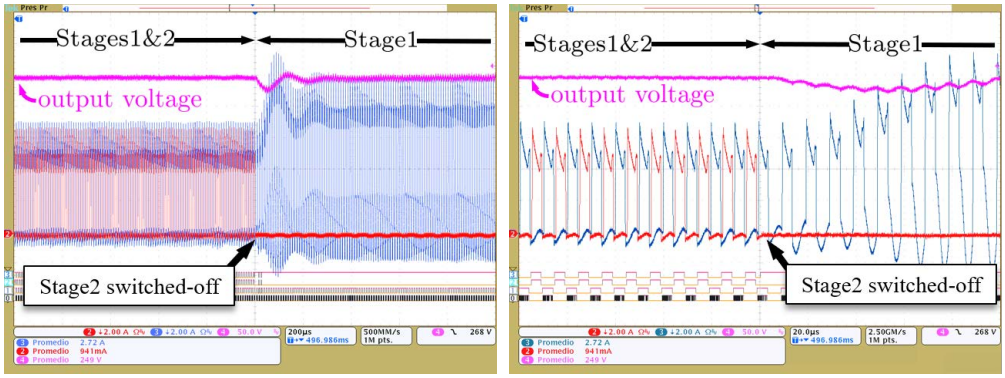
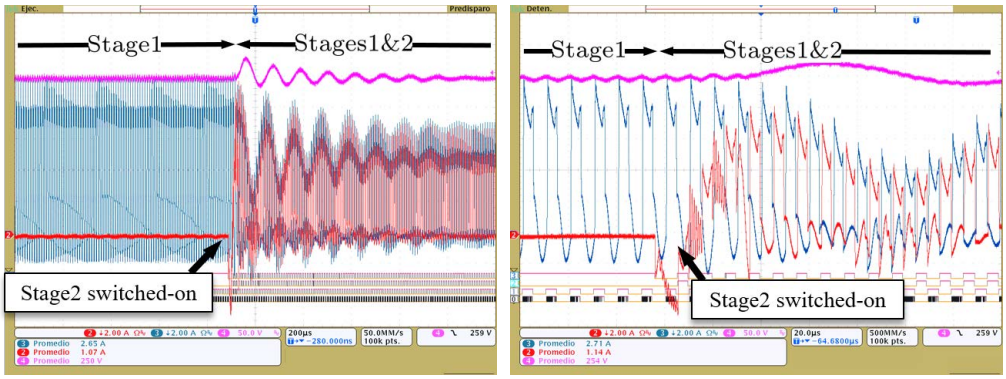


Figure 14. Measurement of the resonant inductor currents in both interleaving parallel connected EACF converters.



(**a**) (**b**)

Figure 15. Closed loop dynamic response of resonant currents and output voltage: (**a**) when one stage was switched off; (**b**) expanded curves.



(**a**) (**b**)

Figure 16. Closed loop dynamic response of resonant currents and output voltage: (**a**) when one stage was switched on; (**b**) expanded curves.

5. Conclusions

In this paper, a solution to improve the static load sharing of active clamp flyback modules when connected in parallel was proposed. It was necessary to alleviate the ringing between the parasitic capacitances of the output diode and coupled inductors and the resonant inductor of the active clamp network because the converter behavior was altered and compromised the load sharing between the connected modules.

In order to develop a solution to that problem, the effects of parasitics in steady-state current balancing was studied in depth within a theoretical framework. A solution that was based on the placement of an additional diode was also analyzed theoretically. It was concluded that the proposed solution was valid and could help to minimize resonances and, therefore, help to obtain a better current balance than without the diode.

The theoretical conclusions were checked with a laboratory prototype. The experimental measurements that were carried out using the two-stage prototype showed a good agreement with the theoretical analysis. Moreover, a good current sharing was achieved in open loop without any dedicated methods being used to assure the current sharing once the resonances disappeared due to the added diode. Finally, this solution suggested that the IPOP connection of multiple active clamp flyback modules did not need any additional mechanisms for current balancing in the converter control loop.

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