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A High Conversion Ratio DC–DC Boost Converter with Continuous Output Current Using Dual-Current Flows

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Abstract: Recently, the demand for small, low-cost electronics has increased the use of cost-effective tiny inductors in power-management ICs (PMICs). However, the conduction loss caused by the parasitic DC resistance (R_{DCR}) of a small inductor leads to low efficiency, which reduces the battery usage time and may also cause thermal problems in mobile devices. In particular, these issues become critical when a conventional boost converter (CBC) is used to achieve high-output voltage due to the large inductor current. In addition, as the output voltage increases, a number of issues become more serious, such as large output voltage ripple, conversion-ratio limit, and overlap loss. To solve these issues, this paper proposed a high-voltage boost converter with dual-current flows (HVDF). The proposed HVDF can achieve a higher efficiency than a CBC by reducing the total conduction loss in heavy load current conditions with a small inductor. Moreover, because in the HVDF, the current delivered to the output becomes continuous, unlike in the CBC with its discontinuous output delivery current, the output voltage ripple can be significantly reduced. Also, the conversion gain of the HVDF is less sensitive to R_{DCR} than that of the CBC. To further increase the conversion gain, a time-interleaved charge pump can be connected in series with the HVDF (HVDFCP) to achieve higher output voltage beyond the limit of the conversion gain in the HVDF while maintaining the advantages of a low inductor current and small output voltage ripple. Simulations using PSIM were performed along with a detailed numerical analysis of the conduction losses in the proposed structures. The simulation results were discussed and compared with those of the conventional structures.

Keywords: high-voltage application; boost converter; voltage ripple; efficiency; conduction loss; overlap loss; conversion gain; continuous output current

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1. Introduction

Power-management integrated DC–DC converters for high-supply voltages are widely used in industrial applications such as light-emitting diode (LED) drivers, liquid crystal display (LCD) bias circuits, energy-harvesting, power-factor correction, etc. [1–5]. However, some applications, such as SSDs and LED drivers, face certain limitations. These applications, which are resistive loads, are heavy loads requiring high conversion gains [6]. Among various DC–DC converters, a charge pump (CP) is capable of generating high-voltage gains using several capacitors. However, generating an output voltage that differs from a predetermined voltage gain can lead to rapid efficiency degradation [7–12]. Additionally, the capacitances need to become very large to use CP in heavy load applications. This means the capacitor should be an external component, which results in a bulky system that has a low power density [13]. On the other hand, there are isolated converters with coupled inductors or transformers for high-voltage gains [14–19], but they suffer from circuit complexity, low efficiency, and high costs. In contrast, a conventional boost converter (CBC) can achieve high-voltage gains using a single inductor and a simple circuit structure [20–23]. Due to the miniaturization of electronic devices, an inductor with a high-quality factor in a limited PCB area is not ideal because of its large volume. Thus,

the use of a small inductor with a low-quality factor is necessary due to size constraints; however, the parasitic DC resistance (R_{DCR}) of the small inductor, increasing in proportion to the temperature, causes large conduction losses, resulting in low efficiency and low conversion gains [24]. Also, since this large R_{DCR} limits the voltage-conversion gain (M), it is difficult to generate a high-voltage output. To overcome these limitations, the hybrid converter, which is a combination inductive converter and charge pump, was introduced. Among the hybrid converters, the multilevel converter makes large conduction losses with a large R_{DCR} because it cannot adjust the DC level of the inductor current [25]. Therefore, a dual-path hybrid converter is used to reduce the inductor current [26]. To apply the hybrid dual-path converter for high-voltage-gain SSDs and LED drivers, this paper proposed a dual-path hybrid converter with a charge pump.

To understand these limitations, the structure of the CBC is shown in Figure 1. The CBC uses a single inductor (L), two switches (S_1, S_2) and one output capacitor (C_O) to convert the input voltage (V_{IN}) to a high-voltage output (V_O), adopting a very simple structure.

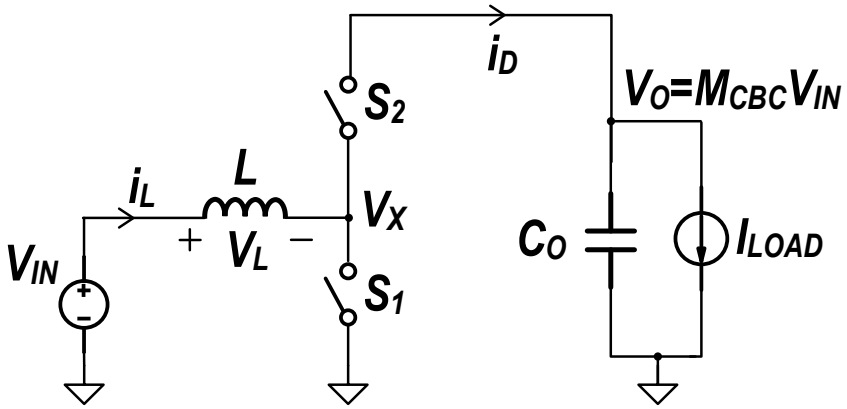


Figure 1. Conventional boost DC–DC converter.

Figure 2 shows the operating principle of the CBC and its voltage and current waveforms. In Φ_1, S_1 is turned on and S_2 is turned off while the inductor current (i_L) is built up with a slope of V_{IN}/L. At this time, the current cannot be delivered to the output; in other words, the output delivery current (i_D) is 0 while C_O is discharged by the load current (I_{LOAD}). In Φ_2, S_2 is turned on and S_1 is turned off while i_L is de-energized with a slope of $-(V_{IN} - V_O)/L$ and delivered to the output. Then Φ_1 and Φ_2 are repeated, and the output voltage can be regulated to a higher voltage than the input voltage V_{IN}.

To obtain the conversion gain of the CBC (M_{CBC}), applying the voltage sec balance to the inductor is expressed as below:

$$DV_{IN} + (1 - D)(V_{IN} - V_O) = 0 \tag{1}$$

where D is the duty cycle, which is the duration of Φ_1 in a single switching period.

Simplifying (1), M_{CBC} is given by

$$M_{CBC} = \frac{V_O}{V_{IN}} = \frac{1}{1 - D} \tag{2}$$

From Equation (2), we see that M_{CBC} is always larger than 1 as D varies from 0 to 1, thereby generating a high output voltage. However, when the CBC uses a small inductor with a large R_{DCR} for high output voltage, there are many issues, as described below.

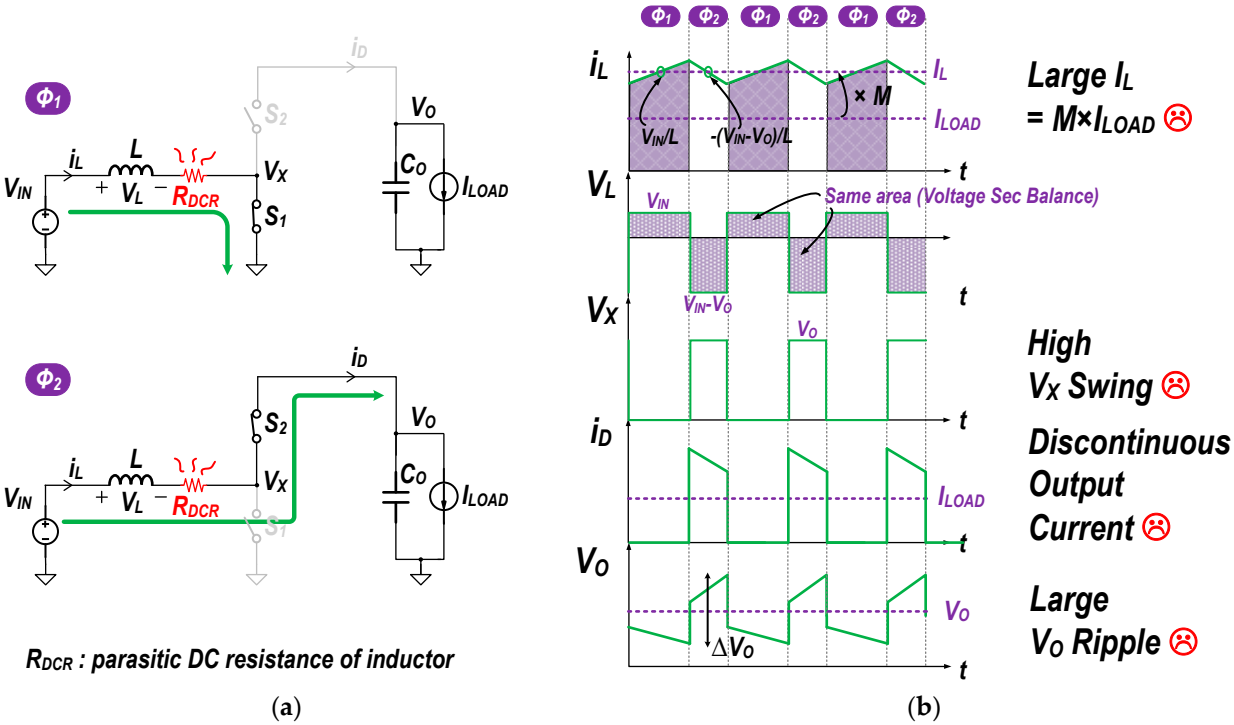


Figure 2. (**a**) Operation mode and (**b**) waveforms of a conventional boost converter.

1.1. Large Inductor Current

The use of a small inductor can cause significant conduction loss (P_{DCR}) in the R_{DCR} of the inductor, resulting in a drastic reduction in power efficiency. P_{DCR} is expressed by

$$P_{DCR} = {i_{L,RMS}}^2 R_{DCR} = ({I_L}^2 + \frac{{\Delta i_L}^2}{12}) R_{DCR} \tag{3}$$

where $i_{L,RMS}$, I_L, and Δi_L are the root-mean-square value, the average value, and the ripple of i_L, respectively. Because the small inductor has a large R_{DCR}, reducing $i_{L,RMS}$ is the only solution, as shown in Equation (3). Particularly, under a heavy load where I_{LOAD} is larger than hundreds of mA, since I_L is much larger than Δi_L, and reducing I_L is the most effective method to decrease P_{DCR}.

To obtain I_L of the CBC, the charge balance is applied to the output capacitor C_O:

$$D(-I_{LOAD}) + (1 - D)(I_L - I_{LOAD}) = 0 \tag{4}$$

Simplifying (4), I_L is given by

$$I_L = \frac{1}{1 - D} I_{LOAD} = M_{CBC} I_{LOAD} \tag{5}$$

Equation (5) shows that I_L is proportional to M_{CBC}. Therefore, as the high voltage is generated, P_{DCR} increases because of the large I_L. Unlike the case of a buck converter, where I_L is always the same as I_{LOAD}, this problem is much more critical for a boost converter [27].

Regarding the R_{DCR}, it cannot be adjusted by the designer, but it varies with temperature. The R_{DCR} is expressed as below [24].

$$R_{DCR}(T) = R_{L\_25C} \times [1 + TC_{Copper} \times (T - 25)] \tag{6}$$

T = temperature of the inductor
R_{L_25C} = inductor series resistance at room temperature (25 °C)
TC_{Copper} = temperature coefficient of copper that is equal to 0.00393

As shown in the Equation (6), R_{DCR} is proportional to the temperature. When the R_{DCR} in CBC increases at high temperatures, the loss increases rapidly by Equation (3) because the inductor current is large.

1.2. Pulsating Output Delivery Current

As shown in Figure 2, a CBC has discontinuous output delivery current i_D pulsating from 0 to I_L. From Equation (5), the larger the conversion gain, the larger the I_L, causing huge pulsating i_D. This results in a large ripple of the output voltage (ΔV_O). To reduce this large ΔV_O, the output capacitor C_O should be large, and the parasitic resistance of the capacitor (R_{ESR}) should be small. Therefore, a CBC requires a larger and more expensive output capacitor than a conventional buck converter, which has continuous i_D.

1.3. Limitation of Conversion Gain

As shown in Equation (2), in ideal conditions, the conversion gain for a CBC has no limit. However, since the small inductor has a large R_{DCR}, it limits the conversion gain in practical applications. Considering the R_{DCR}, the practical conversion gain M_{CBC} is modified as follows [27]:

$$M_{CBC} = \frac{1}{1-D}\frac{1}{(1+\frac{R_{DCR}}{(1-D)^2R})} \tag{7}$$

where R is the load resistance, V_O/I_{LOAD}. From Equation (7), the practical conversion gain M_{CBC} is limited by the ratio of R_{DCR} to R. Figure 3 shows the graph of the conversion gain for different values of R_{DCR}/R. When R is small, which means I_{LOAD} is large and R_{DCR} is large, the CBC cannot achieve a high conversion gain.

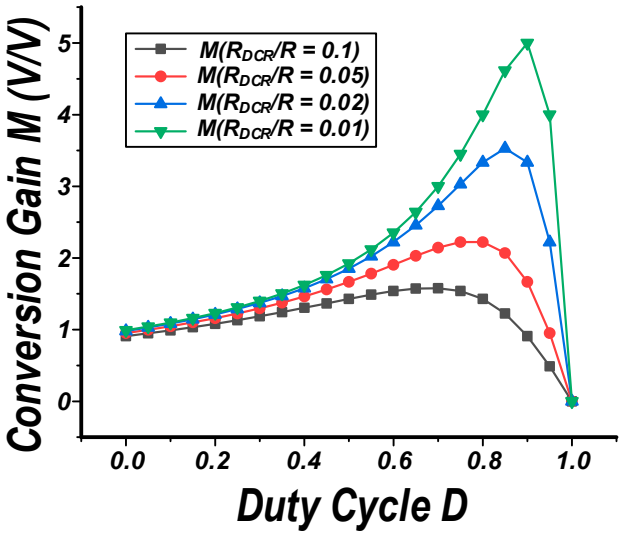


Figure 3. Practical conversion gain for different R_{DCR}/R.

1.4. Large Overlap Loss

As shown in Figure 2, when V_O is very high, the switching node V_X changes very rapidly in every cycle from 0 V at Φ_1 to V_O at Φ_2. Due to the hard switching of the switch, the current flowing through the switch and the voltage across the switch are multiplied, which creates an overlap loss (P_{OV}) as shown in Figure 4. P_{OV} is expressed as follows:

$$P_{OV} = \frac{V_O I_L}{2}(t_{rise} + t_{fall})f_{SW} = \frac{{M_{CBC}}^2 V_{IN} I_{LOAD}}{2}(t_{rise} + t_{fall})f_{SW} \tag{8}$$

where t_{rise}, t_{fall}, and f_{SW} are the turn-on transition time of the switch, the turn-off transition time of the switch, and the switching frequency, respectively. Equation (8) shows that as

the conversion gain increases, P_{OV} can become a substantial loss in a CBC in addition to the conduction loss.

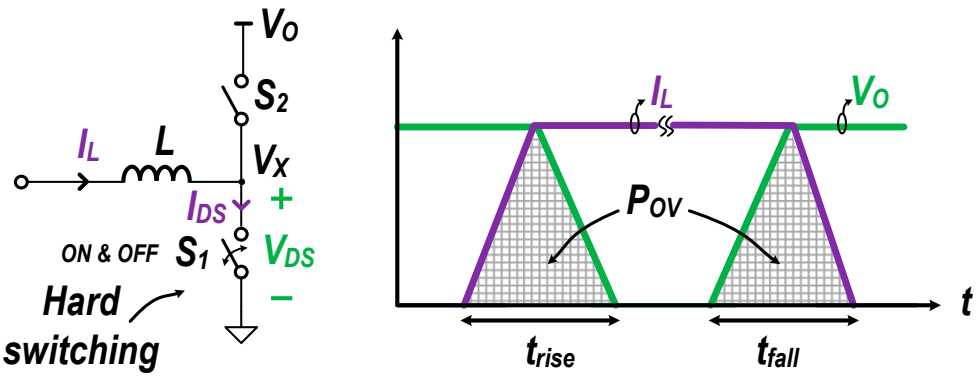


Figure 4. Overlap loss of conventional boost converter.

To resolve the abovementioned issues associated with CBCs, this paper proposed a new high-voltage boost converter with dual-current flows (HVDF). Section 2 describes the operating principle and the advantages of the HVDF. Section 3 introduces a modified structure that can further improve the conversion gain by using the HVDF with the time-interleaved charge pump. In Section 4, the proposed structures are simulated and quantitatively compared to a CBC. Finally, Section 5 gives a brief conclusion about the proposed structures.

2. High-Voltage Boost Converter with Dual-Current Flows

In order to solve the issues associated with a CBC with high-voltage gain and a small inductor, this paper proposes a new topology referred to as a high-voltage boost converter with dual-current flows (HVDF). A converter with dual-current flows was reported previously [26]; however, it is not suitable for high-voltage applications due to its low conversion ratio. The HVDF can be used in high-voltage applications while maintaining the advantages associated with a converter with dual-current flows. The HVDF consists of one inductor (L), six switches (S_1–S_6), two flying capacitors (C_{F1}, C_{F2}), and an output capacitor (C_O) as shown in Figure 5.

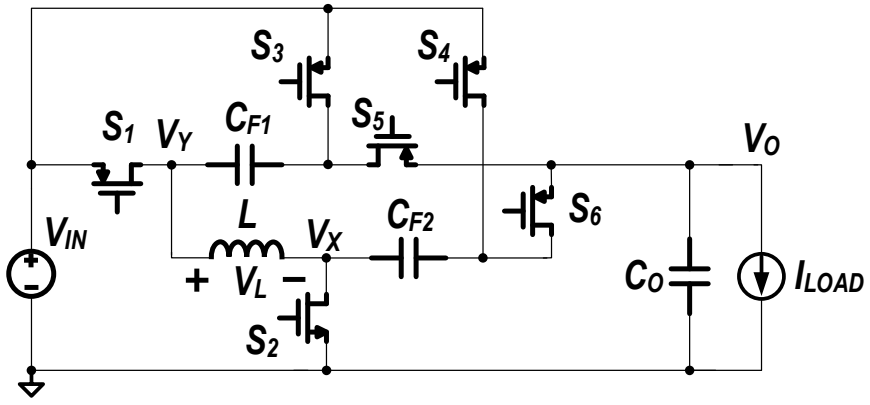


Figure 5. High-voltage boost converter with dual-current flows.

The HVDF has two operation modes (Φ_1, Φ_2) in a single switching cycle. Figure 6 shows the operation principle of the HVDF. In Φ_1, switches S_1, S_2, S_4 and S_5 are turned on, and S_3 and S_6 are turned off. As i_L is built up with a slope of V_{IN}/L, C_{F2} is charged to V_{IN}. At the same time, C_{F1} delivers the capacitor current i_{C1} to the output while being charged with $V_O - V_{IN}$. Unlike a CBC, which cannot transfer energy to the output during the i_L buildup time, the HVDF is capable of transferring energy to the output using the

capacitor current at Φ_1. In Φ_2, S_3 and S_6 are turned on, S_1, S_2, S_4 and S_5 are turned off, and i_L decreases with a slope of $-(2V_O - 3V_{IN})/L$. The dead time is required between Φ_1 and Φ_2 to prevent a large short-circuit current, which causes large conduction losses.

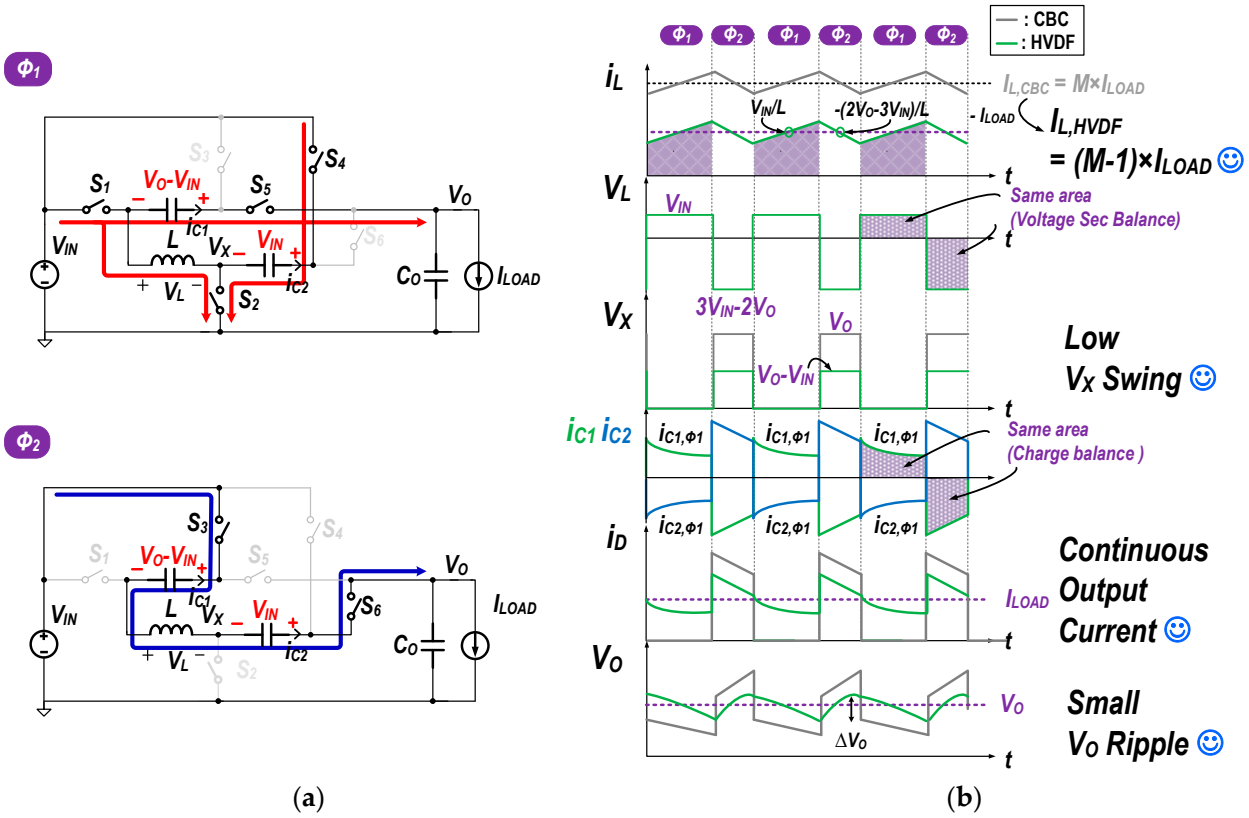


Figure 6. (**a**) Operation mode; and (**b**) waveforms of high-voltage boost converter with dual-current flows.

To obtain the conversion gain (M_{HVDF}) of the HVDF, applying the voltage sec balance to its inductor,

$$DV_{IN} + (1 - D)(3V_{IN} - 2V_O) = 0 \tag{9}$$

Simplifying (8), M_{HVDF} is given by

$$M_{HVDF} = \frac{V_O}{V_{IN}} = \frac{3 - 2D}{2(1 - D)} \tag{10}$$

From Equation (10), as D changes from 0 to 1, M_{HVDF} is always larger than 1.5, which means that the system can operate as a boost converter for high-voltage outputs. Owing to the two flying capacitors C_{F1} and C_{F2}, the HVDF avoids the problems associated with the CBC.

2.1. Reduced Inductor Current

The HVDF has the advantage that the capacitor current i_{C1} of C_{F1} can be delivered to the output even when i_L is not delivered to the output in Φ_1. Owing to this additional current flow, the HVDF can reduce the I_L. To determine the I_L in the HVDF, the average value of i_{C1} in Φ_1 ($I_{C1,\,\Phi1}$) delivered to the output must first be obtained. $I_{C1,\,\Phi1}$ is given by applying the charge balance to C_{F1} as shown below.

$$DI_{C1,\Phi1} - (1 - D)I_L = 0 \tag{11}$$

$$I_{C1,\Phi1} = \frac{1-D}{D} I_L \tag{12}$$

Similarly, applying the charge balance to C_{F2}, the average value of i_{C2} in Φ_1 ($I_{C2,\,\Phi1}$) flowing through C_{F2} is obtained as below.

$$-DI_{C2,\Phi1} + (1-D)I_L = 0 \tag{13}$$

$$I_{C2,\Phi1} = \frac{1-D}{D} I_L \tag{14}$$

Finally, applying the charge balance to the output capacitor C_O with Equations (12) and (14) gives the I_L of HVDF as below.

$$D(I_{C1,\Phi1} - I_{LOAD}) + (1-D)(I_L - I_{LOAD}) = 0 \tag{15}$$

$$I_L = \frac{1}{2(1-D)} I_{LOAD} = (M_{HVDF} - 1) I_{LOAD} \tag{16}$$

This shows that the I_L of the HVDF is always lower than that of CBC, which is MI_{LOAD} in the same M condition. Since this reduced I_L causes low conduction loss, the HVDF can achieve higher efficiency than a CBC. Equation (16) shows that this reduction will be especially significant with high M and heavy loads.

To determine the total conduction loss of the CBC ($P_{Con,CBC}$), the on-resistance of each switch is assumed to be the same as R_{ON}, and $P_{Con,CBC}$ is obtained as follows:

$$P_{Con,CBC} = D{I_L}^2 R_{ON} + (1-D){I_L}^2 R_{ON} + {I_L}^2 R_{DCR} = M^2 {I_{LOAD}}^2 (R_{ON} + R_{DCR}) \tag{17}$$

In contrast, the conduction loss of the proposed converter ($P_{Con,HVDF}$) is obtained as follows:

$$P_{Con,HVDF} = DR_{ON}[(I_L + I_{C1,F1})^2 + (I_L + I_{C2,F1})^2 + {I_{C1,F1}}^2 + {I_{C2,F1}}^2] + 2(1-D)R_{ON}\,{I_L}^2 + R_{DCR}\,{I_L}^2 \tag{18}$$

Substituting Equations (10), (12), (14), and (16) into Equation (18),

$$P_{Con,HVDF} = {I_L}^2 [2R_{ON}\frac{(2-D)}{D} + R_{DCR}] = (M-1)^2 {I_{LOAD}}^2 [2R_{ON}\frac{2M-1}{2M-3} + R_{DCR}] \tag{19}$$

To compare $P_{Con,HVDF}$ and $P_{Con,CBC}$, the ratio of $P_{Con,CBC}$ and $P_{Con,HVDF}$ is expressed as

$$\frac{P_{Con,HVSIC}}{P_{Con,CBC}} = \frac{(M-1)^2 (2R_{ON}\frac{2M-1}{2M-3} + R_{DCR})}{M^2 (R_{ON} + R_{DCR})} \tag{20}$$

Figure 7 is a graph of Equation (20) according to the conversion gain for different R_{DCR} values. The graph shows that the relative to a CBC, the HVDF has low overall conduction loss over a wide range of conversion gains. This is because I_L is reduced by dual-current flows due to the HVDF operating principle. It should be noted that the decrease in conduction loss is greater when a large R_{DCR} is used, which means a small inductor. On the other hand, when the load current is small, switching loss is dominant. This results in the proposed structure having lower efficiency than the CBC, as it requires more switches. When M becomes extremely small, which means short D, since the capacitor current $I_{C1,\,\Phi1}$ rapidly increases based on Equation (12), it leads to an increase in conduction loss. Therefore, we can see that the HVDF can be an effective solution for high gain and small inductor applications.

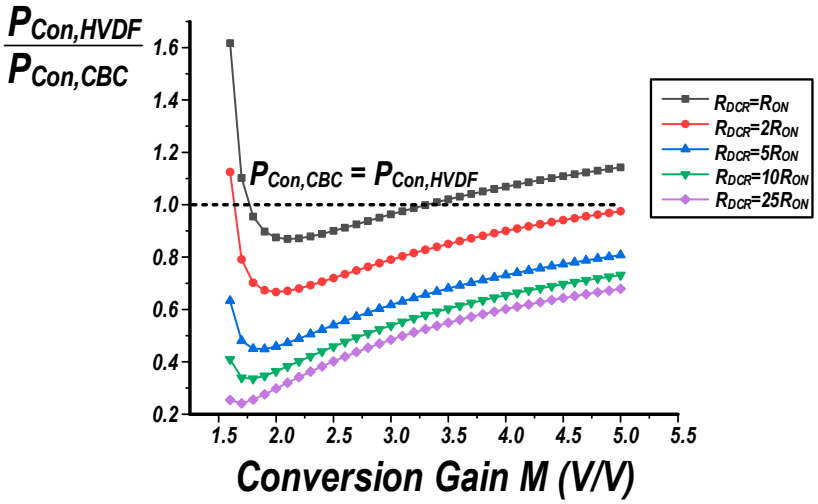


Figure 7. Conduction loss comparison of HVDF and CBC for different R_{DCR} values.

2.2. Alleviated Conversion Gain Limit

Ideally, when R_{DCR} is 0, it is possible to raise the voltage without limiting the conversion gain as shown in Equation (10). However, in practice applications, the conversion gain is limited due to R_{DCR}. To obtain the conversion gain by considering R_{DCR}, applying the voltage sec balance to the inductor,

$$D(V_{IN} - I_L R_{DCR}) + (1 - D)(3V_{IN} - 2V_O - I_L R_{DCR}) = 0 \tag{21}$$

The conversion gain with considering R_{DCR} can be obtained by substituting Equation (16) into (21) as below:

$$M_{HVDF} = \frac{V_O}{V_{IN}} = \frac{3 - 2D}{2(1 - D)} \frac{1}{1 + \frac{R_{DCR}}{4(1-D)^2 R}} \tag{22}$$

Although R_{DCR} limits the conversion gain in the HVDF, Equation (22) shows that the ratio of R_{DCR}/R is reduced to 1/4 compared to Equation (7) for the CBC. This means that the conversion gain of the HVDF is less sensitive to R_{DCR}. Figure 8 shows that the HVDF has a much higher the conversion gain than the CBC under the same operating conditions.

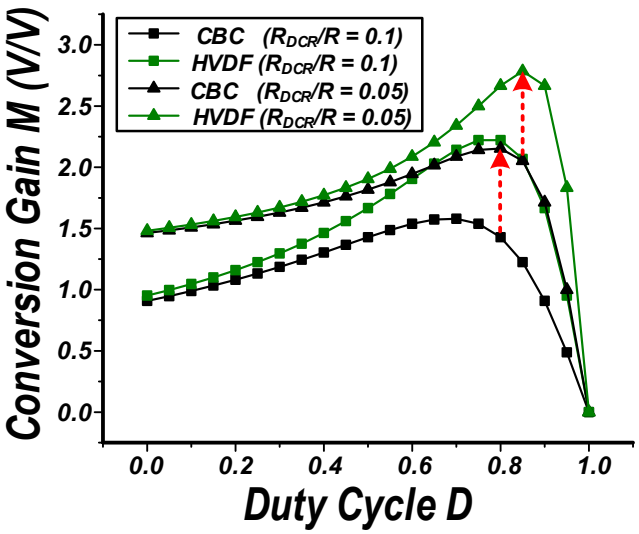


Figure 8. Practical conversion gain of HVDF and CBC for different R_{DCR}/R.

2.3. Reduced Overlap Loss

As shown in the switching node V_X waveform in Figure 6, while the swing of V_X in the CBC is V_O, the swing of V_X in the HVDF is reduced to $V_O - V_{IN}$ due to the flying capacitor C_{F2}. This reduced swing of V_X and reduced I_L can further decrease P_{OV} in the HVDF. The P_{OV} in the HVDF is expressed as

$$P_{OV} = \frac{(V_O - V_{IN})I_L}{2}(t_{rise} + t_{fall})f_{SW} = \frac{(M-1)^2 V_{IN} I_{LOAD}}{2}(t_{rise} + t_{fall})f_{SW} \quad (23)$$

Equation (23) shows that P_{OV} in the HVDF is proportional to the square of $(M - 1)$, while P_{OV} of the CBC is proportional to the square of M, as shown in Equation (8). Therefore, the HVDF can achieve a lower P_{OV} than the CBC.

2.4. Small Output Voltage Ripple

As shown in the i_D and V_O waveforms in Figure 6, since the HVDF always has a continuous output delivery current regardless of its operation mode, the output voltage ripple can be significantly reduced compared to that of the CBC, which has discontinuous i_D. Moreover, this continuous i_D not only alleviates the supply noise of the loading block but also can be an advantage for the output capacitor selection in terms of cost and size because it can relax the output capacitor specification.

3. High-Voltage Boost Converter with Dual-Current Flows and Time-Interleaved Charge Pump

As mentioned above, the voltage-conversion gain of the practical boost converter is limited by the R_{DCR}. Even though the HVDF can alleviate the conversion gain limit, Figure 8 shows that the HVDF still has difficultly achieving M over three. Therefore, when a high-voltage gain over three is required, a 1:2 charge pump with an additional flying capacitor (C_{CP}) can be cascaded with the boost-converter core topology [28,29].

When a buffering capacitor (C_{MID}) is placed between the boost-converter core and the charge pump, the boost-converter core only needs to generate 0.5 V_O for the high output voltage V_O. In other words, the conversion gain becomes two times larger because of the 1:2 charge pump.

In the operation of the 1:2 charge pump, in Φ_{C1}, switches S_{A1}, S_{A2} are turned on, S_{B1}, S_{B2} are turned off, and 0.5 V_O charged in C_{MID} is stored in the flying capacitor C_{CP}. In Φ_{C2}, S_{B1} and S_{B2} are turned on to transfer energy to the output.

Likewise, the HVDF can use a 1:2 charge pump to achieve a high output voltage above the conversion gain limit as shown in Figure 9.

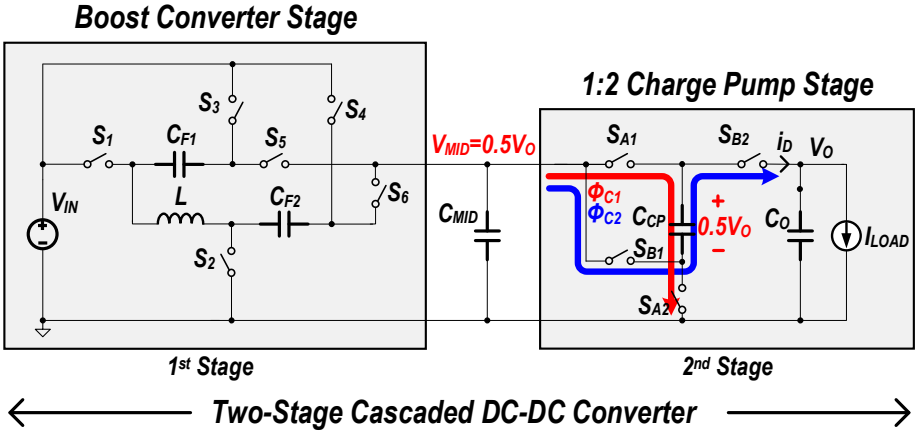


Figure 9. High-voltage boost converter with dual-current flows and cascaded 1:2 charge pump.

However, when C_{CP} is charged in Φ_{C1}, it cannot transfer energy to the output. Accordingly, the advantage of the small output voltage ripple in the HVDF disappears because of discontinuous output delivery current i_D. Therefore, if the charge pump operates in a time-interleaved manner, the energy can always be delivered to the output, which can reduce the output voltage ripple. Figure 10 shows a structure cascaded with a time-interleaved charge pump using two flying capacitors C_{CP1} and C_{CP2}. The charge-pump currents (i_{D1}, i_{D2}) in Φ_{C1} and Φ_{C2} create continuous output delivery current i_D.

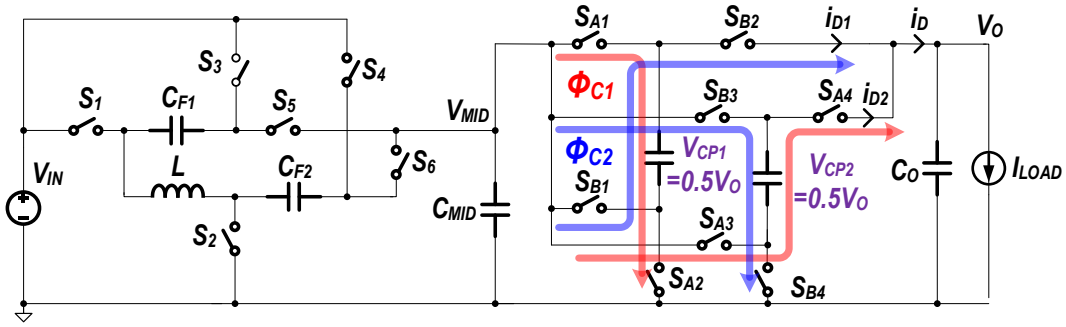


Figure 10. High-voltage boost converter with dual-current flows and time-interleaved 1:2 charge pump.

If the operation mode of the time-interleaved charge pump is synchronized with the HVDF, the buffering capacitor C_{MID} and two switches (S_5, S_6) can be eliminated. Figure 11 shows the final structure, which is referred to as the high-voltage boost converter with a time-interleaved charge pump (HVDFCP).

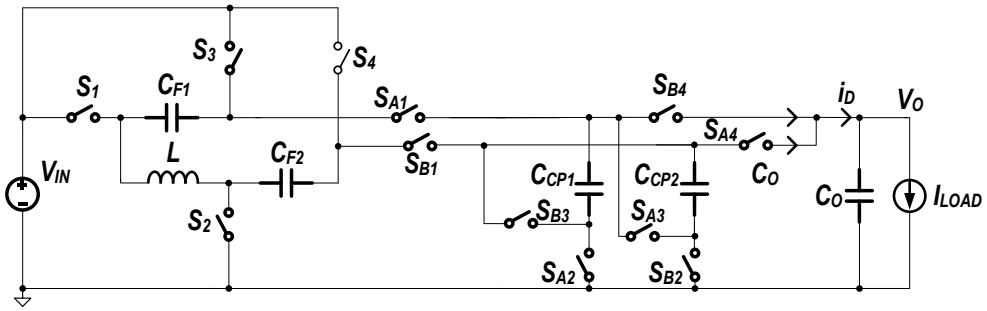


Figure 11. High-voltage boost converter with a time-interleaved charge pump.

The HVDFCP consists of the four flying capacitors (C_{F1}, C_{F2} and C_{CP1}, C_{CP2}) and four switches (S_1–S_4) of the HVDF structure and the charge pump switches (S_{A1}–S_{A4}, and S_{B1}–S_{B4}). The operation mode of the HVDFCP is shown in Figure 12. The operations of the charge pump and the HVDF are the same as described above, but they are synchronized with each other. As with the HVDF operation, the dual-current flows are maintained with high efficiency even though the conversion gain is very high due to the time-interleaved charge pump.

The conversion gain of the HVDFCP (M_{HVDFCP}) is obtained as follows:

$$M_{HVDFCP} = \frac{V_O}{V_{IN}} = \frac{3-2D}{1-D} \tag{24}$$

From Equation (24), the HVDFCP can be used in very high-voltage applications where the conversion gain is higher than three. Although the charge pump is cascaded with the HVDF, it can maintain a small output voltage ripple owing to the continuous output delivery current i_D. In addition, since the boost converter core only generates an output of 0.5 V_O, the overlap loss is further reduced.

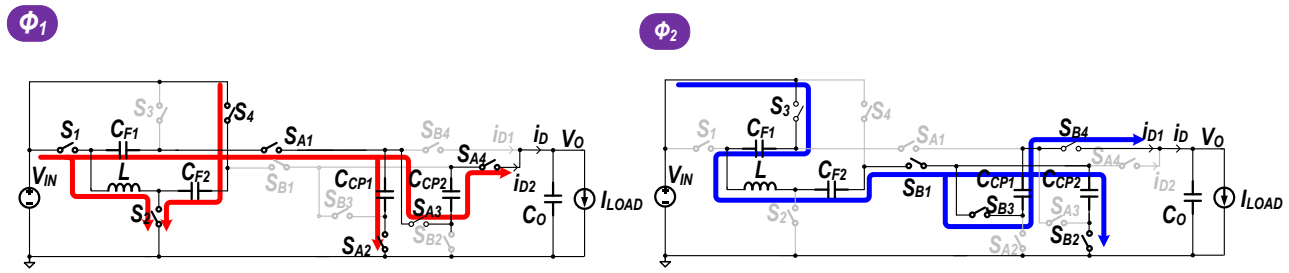


Figure 12. Operation principle of the high-voltage boost converter with dual-current flows and charge pump.

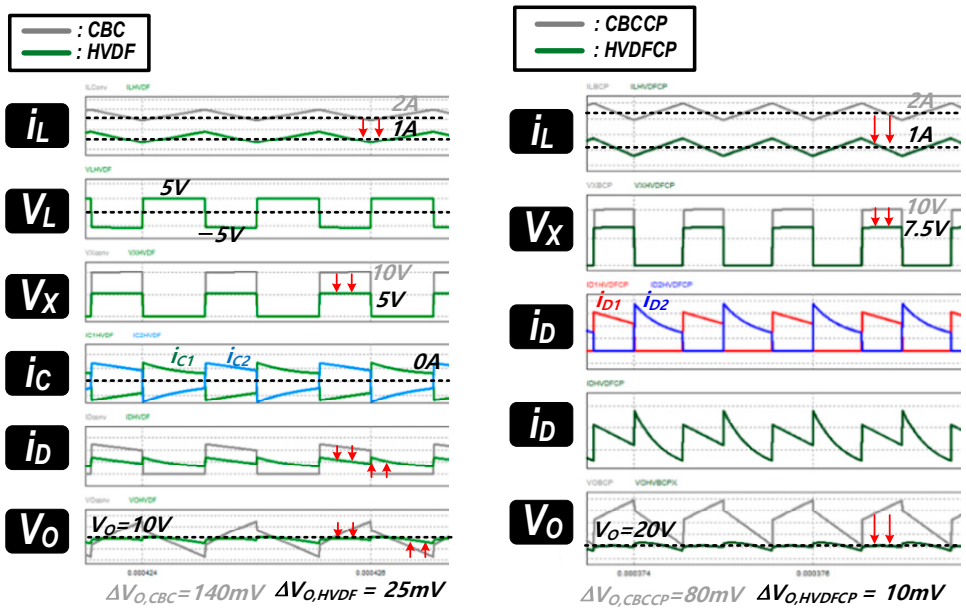
4. Simulation Results and Discussion

4.1. High-Voltage Boost Converter with Dual-Current Flows

Table 1 shows the simulation conditions of the HVDF and CBC for performance comparison. The BCDMOS 180 nm high-voltage process was adopted to prevent the breakdown of the switches in our simulations. Figure 13a shows the simulated waveforms to confirm the operation of the proposed converter. In our design, the dead time of 10 ns was applied to both HVDF and CBC by a non-overlapping clock generator.

Table 1. Simulation conditions for HVDF converter.

V_{IN}	V_{OUT}	I_{LOAD}	f_{SW}	L	R_{DCR}	C_{F1}/C_{F2}	C_O
5 V	10 V	1 A	1 MHz	4.7 µH	0.2 Ω	4.7 µF/4.7 µF	4.7 µF



(**a**) (**b**)

Figure 13. Simulation waveforms of the (**a**) HVDF; and (**b**) HVDFCP.

The simulation results showed that the HVDF has a lower I_L (1 A) than the CBC (2 A). The two capacitor currents (i_{C1} and i_{C2}) satisfy the charge balance, and the voltage V_L across the inductor satisfies the voltage sec balance. Additionally, the switching node V_X of the HVDF was $V_O - V_{IN}$ = 5 V, which is lower than the V_O = 10 V. V_X of the CBC, thus reducing overlap loss. Owing to the dual-current flows, the output current of the CBC is discontinuous because it only flows during phase 2. This causes the current to fluctuate between zero and the inductor current. On the other hand, the output current of HVDFCP

flows during both phases 1 and 2, so it fluctuates between i_{C1} and i_{C2}. Therefore, the ΔV_O of the HVDF is 25 mV, which is significantly lower than that of the CBC, 140 mV.

Figure 14a shows the efficiency plots for different I_{LOAD} values for the HVDF and CBC when M is 1.7 and 2.5. As I_{LOAD} increases, the HVDF reduction of I_L becomes larger than that of the CBC, which means that the efficiency is improved much more for the HVDF than for the CBC. However, since the switching loss is dominant under light loads where I_{LOAD} is small, the CBC shows better efficiency in light load conditions due to the larger number of power switches in the HVDF compared to the CBC. Therefore, the HVDF is more suitable for heavy load current conditions, where I_{LOAD} is larger, than light load conditions.

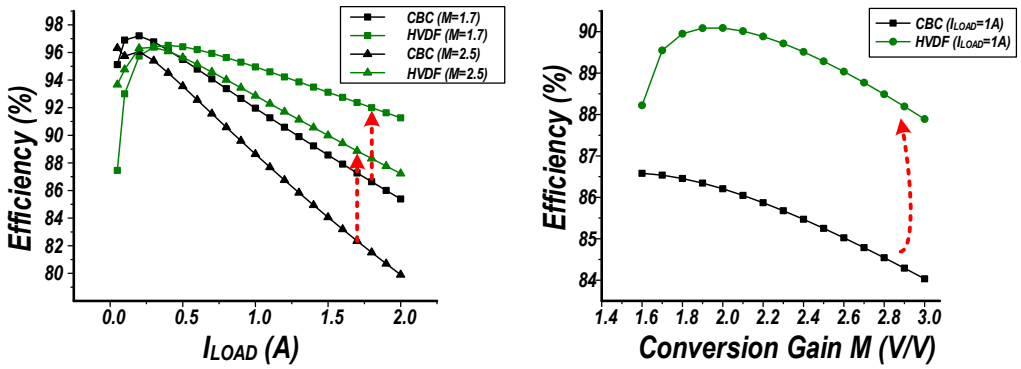


Figure 14. Simulated efficiency plot of HVDF and CBC with different (**a**) load currents; and (**b**) conversion gain.

Figure 14b shows the efficiency of both the CBC and the HVDF versus the conversion gain when I_{LOAD} is 1 A. The HVDF has a higher efficiency compared to the CBC across a wide range of M. As shown in Equation (20) and Figure 7, the peak efficiency of the HVDF is achieved when M is around 2, which is the minimized conduction-loss region.

4.2. High-Voltage Boost Converter with Dual-Current Flows and Time-Interleaved Charge Pump

Table 2 shows the simulation conditions of the HVDFCP and conventional boost converter with a charge pump (CBCCP) for performance comparison. Figure 13b shows the simulated waveforms to confirm the operation of the proposed converter.

Table 2. Simulation conditions for HVDFCP.

V_{IN}	V_{OUT}	I_{LOAD}	f_{SW}	L	R_{DCR}	C_{F1}–C_{F4}	C_O
5 V	20 V	0.5 A	1 MHz	4.7 µH	0.2 Ω	4.7 µF	4.7 µF

The simulation results showed that I_L of HVDFCP is 1 A, which is much smaller than the 2 A of the CBCCP. As a result, the overall conduction loss can be reduced in the HVDFCP. In addition, the switching node V_X was reduced to $0.5(V_O - V_{IN})$ = 7.5 V for the HVDFCP compared to 0.5 V_O = 10 V for the CBCCP, resulting in low overlap loss due to low V_X swing. Thus, higher efficiency can be achieved with the HVDFCP than with the CBCCP. Moreover, due to the time-interleaved charge pump in the HVDFCP, i_{D1} and i_{D2}, which are the charge-pump currents in each operation mode, can be delivered to the output. The i_D, which is the sum of i_{D1} and i_{D2}, allows the continuous current to flow to the output. Therefore, even though V_O is very high (20 V), the HVDFCP can achieve a smaller ΔV_O (10 mV) than the CBCCP (80 mV).

Figure 15a shows an efficiency plot versus I_{LOAD} when M is 3.5 and 5. Although the absolute efficiency of the HVDFCP is lower than that of the charge pump-free structure due to the large number of switches, the HVDFCP has the advantage that the efficiency is

further improved compared to that of the CBCCP because the reduction of I_L becomes large as I_{LOAD} increases. However, since the switching loss is dominant in light load conditions, where I_{LOAD} is small, the CBCCP shows better efficiency in these conditions than the HVDFCP with its numerous power switches. Therefore, the HVDFCP is a suitable structure for high-voltage gain in heavy load current conditions where I_{LOAD} is large.

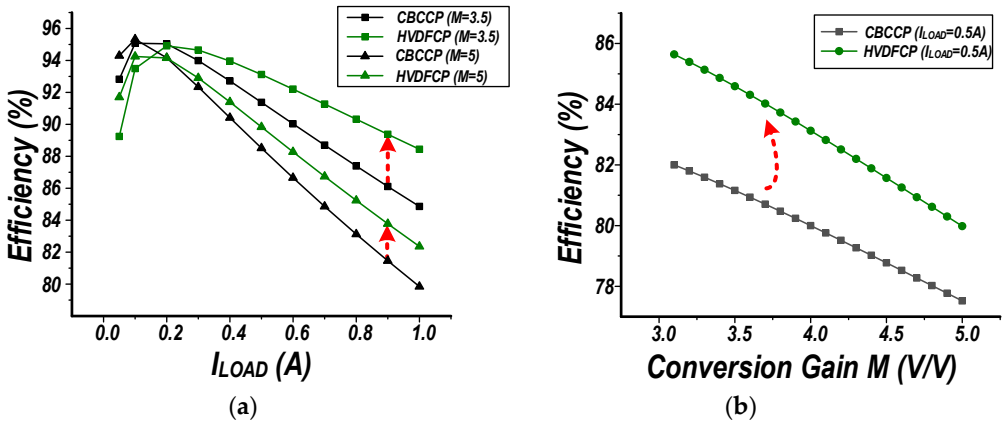


Figure 15. Simulated efficiency plot of HVDFCP and CBCCP at different (**a**) load currents and (**b**) conversion gain.

Figure 15b shows the efficiency graph of the CBCCP and HVDFCP according to M when I_{LOAD} is 0.5 A. The HVDFCP has higher efficiency characteristics than the CBCCP across a wide range of M.

Another advantage of the proposed converters for high V_O is the small ΔV_O. Figure 16 shows the ΔV_O of the CBC, HVDF, CBCCP, and HVDFCP when I_{LOAD} is 1 A. The proposed structures have a much smaller ΔV_O than the conventional structures because of the dual-current flows. More specifically, the HVDF has better ΔV_O characteristics in the region where M is smaller than three, and the HVDFCP has better performance when M is larger than three. Thus, despite the large load current of 1 A and the high-voltage gain, the proposed structures have a small output voltage ripple (less than 100 mV) across a wide range of M.

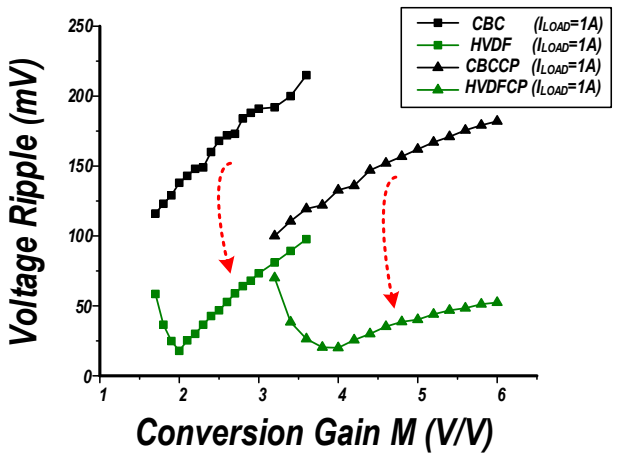


Figure 16. Simulated output voltage-ripple plot for different conversion ratios.

This can also be confirmed through FFT analysis. Figure 17 is a waveform showing the FFT analysis of the proposed structure and conventional boost converter. In this analysis, the simulation condition was the same as in Table 2. The switching frequency was set to 1 MHz, and the sampling frequency of the FFT was set to 200 MHz, which

was sufficient to capture the frequency component accurately. Figure 17a represents the harmonic components of the output voltage, while Figure 17b represents the harmonic components of the output current. Both Figure 17a,b show that the fundamental frequency component of the proposed structure is significantly lower, by 0.098 times, than that of the conventional boost converter. A decrease in the fundamental frequency component meant that the ripple was reduced. While the conventional boost converter has a large output voltage ripple due to the discontinuous current flowing through the output, the proposed structure has a smaller output ripple due to the continuous current flowing through the output. Figure 17 shows the reduction of the fundamental frequency and harmonic components in the proposed structure.

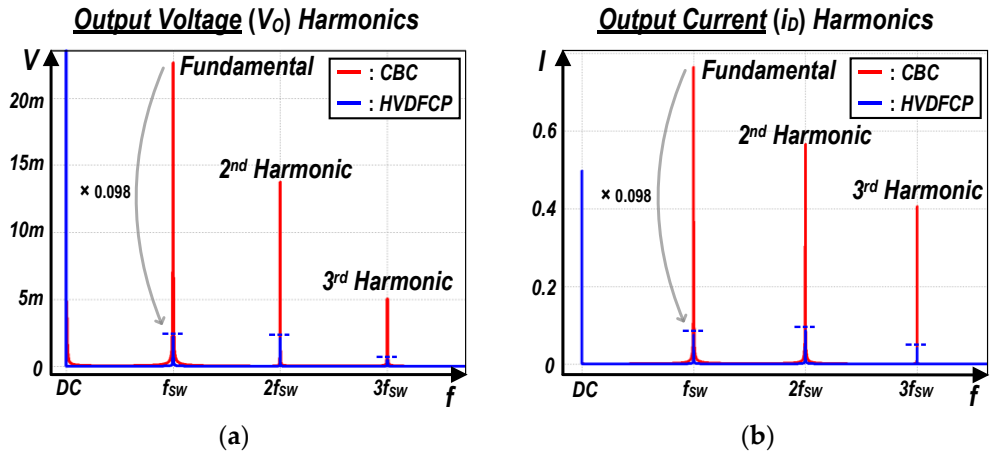


Figure 17. FFT analysis of (**a**) output voltage and (**b**) output current.

5. Conclusions

For high conversion gain, a conventional boost converter (CBC) has many issues, such as a large output voltage ripple, large inductor current, conversion ratio limit, and overlap loss in heavy load current conditions with a small inductor. To solve these issues, in this paper, we proposed a high-voltage boost converter with dual-current flows (HVDF). Owing to the dual-current flows in the HVDF, the inductor current was significantly reduced compared with that of the CBC, resulting in low overall conduction loss. Accordingly, the HVDF can achieve high efficiency and solve the thermal problems associated with mobile devices. Moreover, the continuous output delivery current offers the additional advantage of a small output voltage ripple. Furthermore, the conversion gain of the HVDF is less sensitive to R_{DCR} than that of the CBC. To further increase the conversion gain of the HVDF, a time-interleaved charge pump was cascaded with the HVDF (HVDFCP) using additional flying capacitors to generate high-voltage output beyond the limit of the conversion gain in the HVDF. The HVDFCP can generate two-times higher output voltage while maintaining the advantages of the HVDF. In summary, even when the proposed high-voltage converters operate in heavy load current conditions with small inductors, they can achieve a reduced inductor current, small output voltage ripple, less-sensitive conversion gain, and reduced overlap loss. Therefore, the proposed HVDF and HVDFCP are promising solutions for use in heavy load current conditions with a small inductor.

Author Contributions: S.-U.S. analyzed the characteristics, performed the simulations, and H.-S.K. wrote the paper. All authors have read and agreed to the published version of the manuscript.

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