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Improving the Stability and Accuracy of Power Hardware-in-the-Loop Simulation Using Virtual Impedance Method

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Abstract: Power hardware-in-the-loop (PHIL) systems are advanced, real-time platforms for combined software and hardware testing. Two paramount issues in PHIL simulations are the closed-loop stability and simulation accuracy. This paper presents a virtual impedance (VI) method for PHIL simulations that improves the simulation's stability and accuracy. Through the establishment of an impedance model for a PHIL simulation circuit, which is composed of a voltage-source converter and a simple network, the stability and accuracy of the PHIL system are analyzed. Then, the proposed VI method is implemented in a digital real-time simulator and used to correct the combined impedance in the impedance model, achieving higher stability and accuracy of the results. The validity of the VI method is verified through the PHIL simulation of two typical PHIL examples.

Keywords: power hardware-in-the-loop; impedance model; stability; accuracy; virtual impedance

1. Introduction

Power hardware-in-the-loop (PHIL) systems represent an emerging novel technique that is being increasingly applied in power systems for equipment testing and validation. The typical building blocks of a PHIL simulator are shown in Figure 1. Such a simulator is generally composed of three major parts: (I) the original power system (OPS), which is modeled in a real-time simulator; (II) the interface equipment (IE), which links the hardware and the simulated system [1]; and (III) the piece of hardware under test (HUT). The reference signal is obtained on the OPS side, and it is applied to the terminals of the actual hardware through the IE to establish a virtual exchange of power between the simulated virtual network and the power HUT. In a PHIL system, the simulated network and the HUT are both operating at a high power level [2–5]. Many simulation platforms that support PHIL simulations are commercially available [6–14], and such simulations have been extensively used for testing and design of distributed generation systems [15–18] and electric vehicles [19]. Moreover, PHIL systems offer several advantages over other analysis and testing methods. These systems minimize the cost and risk of examining various extreme conditions and maximize the likelihood of identifying hidden defects in an apparatus before their impacts are discovered in actual operations. Thus, the potentially serious consequences can be avoided.

The key element in a PHIL system is the simulation/hardware interface. Ideally, the IE between the HUT and the OPS should have an infinite bandwidth, unity gain, and zero time delay. However, an ideal IE in a PHIL system is neither achievable nor affordable. Moreover, some types of errors (IE bandwidth, sensor noise, time delay, and ripple of the IE) may cause severe stability issues or unacceptable accuracy issues in the results [20–25]. Therefore, these concerns are worth researching,

both theoretically and practically. To address the stability issues of PHIL systems, various interface algorithms (IAs), which are used to connect the virtually simulated system and physical hardware, have already been proposed [26]. In the ideal transformer and inductor model (ITM) [27], the voltage amplifier reproduces the simulated voltage and imposes it onto the hardware circuit. The actual current is measured in the hardware circuit and fed back into the simulated circuit. An interface method that is based on a first-order approximation linear system has been proposed in [28]; it is based on the historical data collected, and the model coefficients are calculated and updated. However, this method is often ill-conditioned and yields incorrect coefficients [29]. Another approach, called the transmission-line model (TLM) [30], represents the linking of reactive components (i.e., inductors and capacitors) between the physical and simulated networks as a transmission line. However, the method does require the introduction of an interface series resistor on the physical side. This resistor is not part of the original network. Hence, the power loss in the resistor is not part of the system solution. The reference [31] described the five different interface algorithms, along with discussions of their relative strengths and weaknesses, with the damping impedance method (DIM) providing the better stability and accuracy. However, it is difficult to achieve the value of the damping impedance, especially in a complicated simulation. Meanwhile, other commonly employed methods, which include the addition of hardware and software filters, are described in [32,33], but, these methods heavily effect the accuracy of PHIL systems. Therefore, the search for a better method to improve the stability and accuracy of the PHIL simulations remains a research topic of considerable interest.

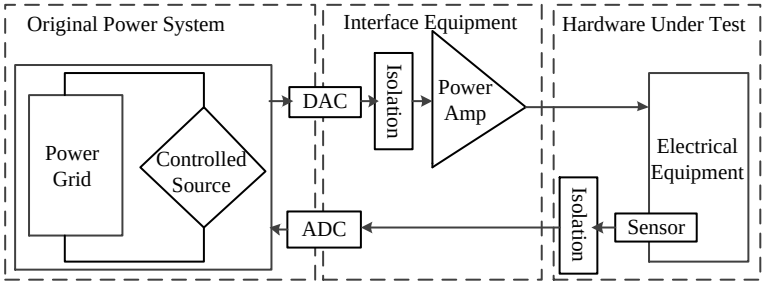

Figure 1. Basic building blocks of a power hardware-in-the-loop (PHIL) simulation.

The impedance method has been widely used in grid-connected systems. The impedance of a grid-connected voltage-source converter is critical to any analysis of the stability and resonance between the converter and the grid, including that with the filter of the converter [34]. Particularly, a grid-connected voltage-source converter can be modeled as a current source in parallel with an impedance [35], and the stability of the system is determined by the magnitude of the impedance that can be improved by increasing the output impedance at the harmonic frequencies [36]. Similarly, to improve the stability of a PHIL system [37,38], a virtual impedance (VI) method [39–41] can be introduced.

This paper is the first to describe the application of the VI method to improve the stability and accuracy of the PHIL simulations. This method can be conveniently implemented on the OPS side. The stability criterion for a PHIL simulation is based on the equivalent impedance model, which is a simple model including an OPS impedance and a combined impedance of the HUT and the IE. The VI method is used to correct the combined impedance in the impedance model. The accuracy of a PHIL system has also been investigated and is herein discussed. Through the PHIL simulations of two typical PHIL examples, it is revealed that the VI method obtains a higher stability and accuracy than another method.

The remainder of this paper is organized as follows. In Section 2, the impedance model of the PHIL simulation is established. The stability and accuracy of the PHIL simulation are analyzed. Then, the VI method and its design rules are presented in Section 3. In Section 4, PHIL simulation results are reported to verify the effectiveness of the proposed method. Finally, Section 5 presents the conclusions.

2. Modeling of a PHIL System

2.1. PHIL System Model

Figure 1 shows the overall architecture of a PHIL simulation. As mentioned in the introduction, the system consists of three fundamental subsystems: the original power system (OPS), the interface equipment (IE) and the hardware under test (HUT). As shown in Figure 1, the IE connects the real-time simulator and the real system. The most important components of the IE are the power amplifier (PA), a digital-to-analog converter (DAC) and an analog-to-digital converter (ADC).

The generic PHIL model, shown in Figure 2, is based on the ideal transformer method (ITM) [29]. The ITM is one of the most conventional and straightforward methods for implementing a PHIL simulation.

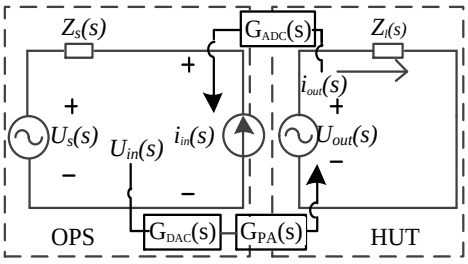

Figure 2. Structure diagram of a PHIL simulation system.

This paper focuses on the simulation of the power grid (OPS side). The majority of the grid impedance arises from long distribution wires and low-power transformers. This impedance can be modeled as an inductor in series with a resistor for simplicity. Therefore, this impedance can be modeled by its Thévenin equivalent. An ideal grid voltage source $U_s(s)$ is placed in series with a grid impedance $Z_s(s)$ on the OPS side. The load $Z_l(s)$ is the equivalent load on the HUT side. To facilitate the simulation, a voltage amplifier reproduces the simulated voltage $U_{in}(s)$ as a physical voltage $U_{out}(s)$ and imposes it on the load resistor. The actual current $i_{out}(s)$ drawn by the resistor is measured, and the measured signal is fed back into the simulated circuit by a current source producing a current $i_{in}(s)$. The main procedures for a PHIL simulation is described as follows.

To build an accurate and flexible PHIL system, a PA in the laboratory is applied. The schematic diagram of the PA, which employs a single-phase H-bridge converter connected to the HUT, is provided in Figure 3. An output filter is used to suppress high-frequency switching components to prevent them from entering the HUT.

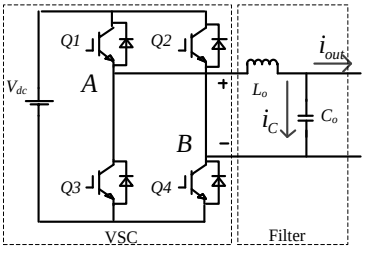

Figure 3. Switching power amplifier (PA) circuit.

As shown in Figure 4, a voltage controller $G_c(s)$ based on the Proportion Integration (PI) controller is proposed. $G_c(s)$ can be formulated as

$$G_c(s) = K_p + \frac{K_i}{s}. \quad (1)$$

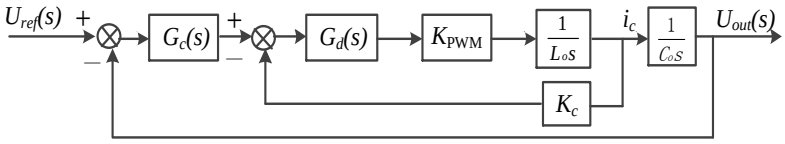

Figure 4. Transfer function block diagram of the switching PA.

To achieve a higher stability of the PA, an active damping factor K_c for the PA inverter is added to the system. The digital controller of the PA is subject to a computation delay, a pulse-width modulation (PWM) delay and other delay components, which can be represented by $G_d(s)$. K_{PWM} represents the transfer function of the inverter. Thus, the transfer function of the PA can be formulated as

$$G_{PA}(s) = \frac{K_{pwm}G_d(s)G_c(s)}{LCs^2 + K_{pwm}K_cG_d(s) + K_{pwm}G_d(s)G_c(s)}. \tag{2}$$

DAC and ADC interface cards are needed to exchange signals between the real-time simulator and the hardware. For simplicity, the DAC and ADC are considered as part of an approximate equivalent model of the interface subsystem. The transfer function of the DAC and ADC components of the interface $G_{DA}(s)$ includes a small time delay T_d, and it can be formulated as

$$G_{DA}(s) = e^{-T_d s}. \tag{3}$$

For mathematical analysis, a simpler and approximate equivalent circuit is adopted, where $G_{IE}(s)$ represents the combination of $G_{DA}(s)$ and $G_{PA}(s)$:

$$G_{IE}(s) = G_{PA}(s) \cdot G_{DA}(s). \tag{4}$$

Thus, the equivalent transfer function block diagram of the PHIL simulation model can be established as shown in Figure 5.

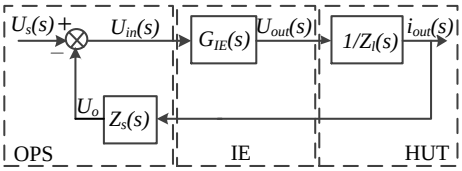

Figure 5. Transfer function block diagram of the PHIL simulation system.

To establish an equivalent impedance model, the equivalent circuit is formulated as

$$U_{in}(s) = U_s(s) - Z_s(s)i_{out}(s). \tag{5}$$

The reference signal $U_{in}(s)$ can be amplified into output voltage $U_{out}(s)$ through the IE. The output voltage $U_{out}(s)$ imposes on the HUT, which is formulated as

$$U_{out}(s) = U_{in}(s) \cdot G_{IE}(s). \tag{6}$$

According to Kirchhoff's law, the following two equations can be obtained:

$$Z_l(s) = U_{out}(s)/i_{out}(s) = U_{in}(s) \cdot G_{IE}(s)/i_{out}(s), \tag{7}$$

$$Z_{lc}(s) = U_{in}(s)/i_{out}(s) = Z_l(s)/G_{IE}(s). \tag{8}$$

According to Equations (5)–(8), $Z_l(s)$ can be converted into a combined impedance $Z_{lc}(s)$ that includes $G_{IE}(s)$. Thus, the impedance model illustrated in Figure 6 is obtained. The stability and accuracy analysis based on this model are described as followings.

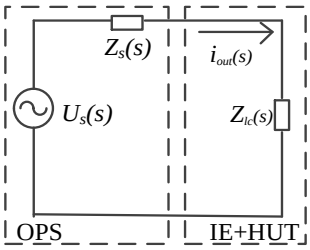

Figure 6. Equivalent circuit for the PHIL simulation system.

2.2. Stability Analysis

A PHIL simulation system can be represented by the equivalent circuit depicted in Figure 6, for which the output current can be written as

$$i_{out}(s) = \frac{U_s(s)}{Z_s(s) + Z_{lc}(s)}. \tag{9}$$

This can be rearranged to yield the following equation:

$$i_{out}(s) = \frac{U_s(s)}{Z_s(s)} \cdot \frac{1}{1 + Z_{lc}(s)/Z_s(s)}. \tag{10}$$

In this case, it is assumed that the source voltage is stable when the system is unloaded. Hence, both $U_s(s)$ and $1/Z_s(s)$ are stable; therefore, the stability of the current depends on the stability of the second term on the right-hand side of Equation (10). The stability of the system can be estimated from the following equation:

$$H(s) = \frac{1}{1 + Z_{lc}(s)/Z_s(s)}. \tag{11}$$

Therefore, $Z_{lc}(s)$ and $Z_s(s)$ determine the stability of the PHIL system. According to [42], if the frequency responses of $Z_s(s)$ and $Z_{lc}(s)$ intersect at f_i, then the phase margin (PM) must be positive ($PM > 0°$). Thus, PM is formulated as

$$PM = 180° - \{\arg[Z_s(s)] - \arg[Z_{lc}(s)]\}. \tag{12}$$

To improve the stability of the system, it is necessary to compensate and correct for the combined impedance $Z_{lc}(s)$. To this end, the magnitude and phase margin of the combined impedance $Z_{lc}(s)$ are increased near the intersection frequency.

2.3. Accuracy Evaluation

The accuracy of a PHIL simulation can be estimated by comparing the combined impedance $Z_{lc}(s)$ to the actual impedance $Z_l(s)$. Because most of the errors in such a system arise from the IE, the impedance error is calculated based on the HUT subsystem, where the combined impedance $Z_{lc}(s)$ is the most important component in terms of accuracy. The impedance error $E(s)$ can be evaluated as follows:

$$E(s) = \left| \frac{Z_l(s) - Z_{lc}(s)}{Z_l(s)} \right|. \tag{13}$$

3. Proposal to Improve the Stability and Accuracy of PHIL Simulations

Based on the impedance model, the combined impedance $Z_{lc}(s)$ can be shaped by means of the VI. Thus, the accuracy of a PHIL simulation can be enhanced by introducing a paralleling impedance to shape the combined impedance $Z_{lc}(s)$.

Figure 7 shows the equivalent circuit for the PHIL simulation system with a paralleling impedance $Z_{cp}(s)$.

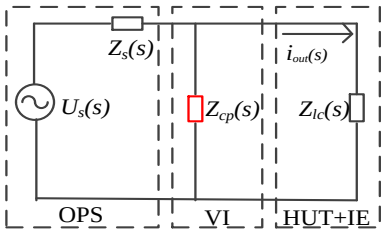

Figure 7. Equivalent circuit for the PHIL simulation system with a paralleling virtual impedance (VI).

The shaped impedance $Z_{eq}(s)$ becomes

$$Z_{eq}(s) = \frac{Z_{cp}(s)Z_{lc}(s)}{Z_{cp}(s) + Z_{lc}(s)} = \frac{Z_{cp}(s)Z_l(s)/G_{IE}(s)}{Z_{cp}(s) + Z_l(s)/G_{IE}(s)}. \quad (14)$$

As shown in Equation (14), to compensate the magnitude of impedance $Z_{lc}(s)$, it is necessary to make the impedance $Z_{eq}(s)$ equal to the impedance $Z_l(s)$. Thus, the impedance $Z_{cp}(s)$ can be derived as follows:

$$Z_{cp}(s) = \frac{Z_l(s)}{1 - G_{IE}(s)}. \quad (15)$$

In this way, the impedance error introduced by the IE can be eliminated.

Figure 8 shows the block structure of the equivalent transfer function of the PHIL system with equivalent impedance. The basic model depicted in Figure 8a can be transformed into the diagram shown in Figure 8b. The equivalent transformation presented in Figure 8c shows the equivalent model as it is implemented on the OPS side.

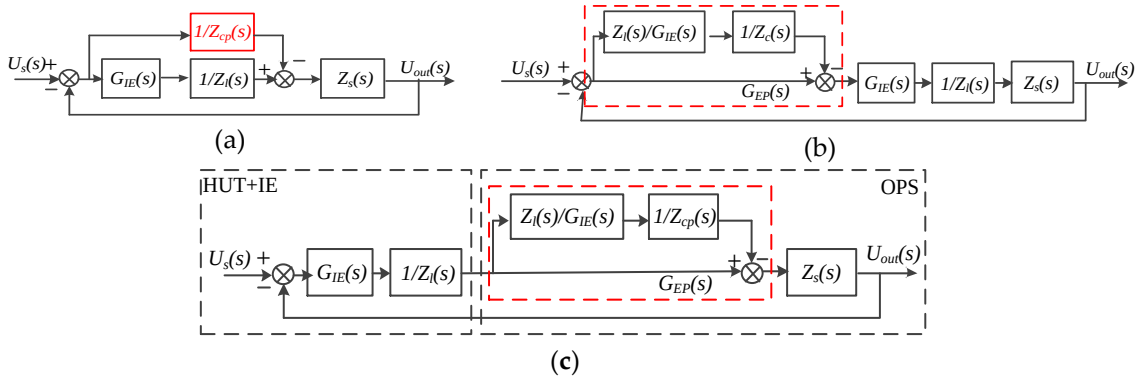

Figure 8. Transfer function diagram of the PHIL system: (**a**) s-domain model; (**b**) equivalent transformation I; (**c**) equivalent transformation II.

Figure 9 illustrates the implementation of the paralleling impedance. Moreover, because of the flexibility of the PHIL system provided by software simulation, various function blocks can be easily implemented in the simulation for a signal preprocessing. As shown in Figure 9, the introduction of the compensated block $G_{EP}(s)$ does not alter the PHIL system topology, it simply requires the insertion

of a function block in the path of the feedback current signal to compensate for the error in the PHIL system. The equivalent transfer function can be calculated as follows:

$$G_{EP}(s) = \frac{1}{G_{IE}(s)} = \frac{LCs^2 + K_{pwm}K_cG_d(s) + K_{pwm}G_c(s)G_d(s)}{K_{pwm}G_c(s)G_d(s)}. \quad (16)$$

The paralleling impedance improves the simulation performance of the PHIL system. However, the shaped impedance Z_{cp}(s) may still intersect with impedance Z_s(s) in the high-frequency range. Thus, an additional series virtual impedance is proposed. Figure 10 shows the structure of the PHIL system with the addition of a series impedance Z_{cs}(s).

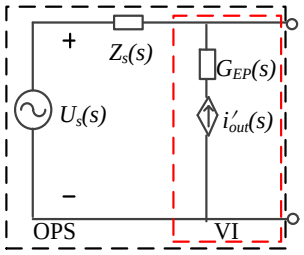

Figure 9. Implementation of a paralleling VI on the original power system (OPS) side.

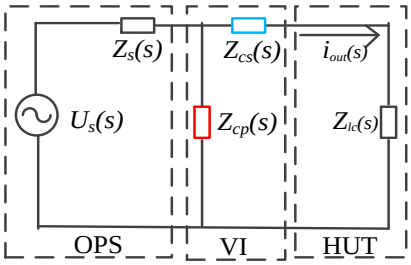

Figure 10. Equivalent circuit for the PHIL system based on the VI model.

This series impedance is equivalent to a low-pass filter, the purpose of which is to ensure system stability and to avoid high-frequency components arising from numerical computations. The equivalent series impedance can be obtained as follows:

$$G_{ES}(s) = \frac{5000}{s + 5000}. \quad (17)$$

The equivalent transformation is presented in Figure 11. The equivalent model is implemented on the OPS side.

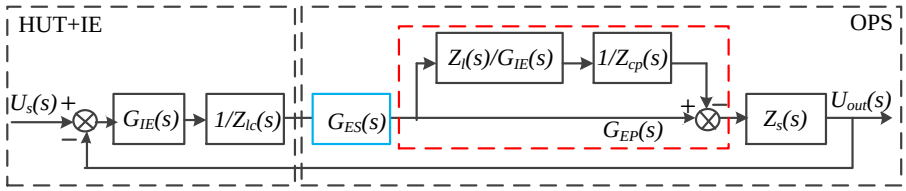

Figure 11. Transfer function block diagram for the PHIL system based on the VI model.

Figure 12 illustrates the implementation of the series impedance. This function block can be easily implemented on the OPS side.

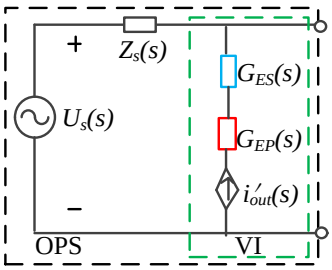

Figure 12. Implementation of the VI on the OPS side.

4. Experimental Verification

4.1. Description of the PHIL Platform

To verify the efficacy of the proposed method, two typical PHIL scenarios were simulated. Note that this paper focuses on the simulation of the power grid (OPS side). The majority of the grid impedance arises from long distribution wires and low-power transformers, and this impedance can be modeled as an inductor in series with a resistor for simplicity [42]. Firstly, a linear HUT scenario was theoretically analyzed. The impedance-based stability criterion was used to assess the stability of the PHIL system. The VI method was applied to this first scenario to improve the stability of the linear PHIL simulation. Then, a second scenario with a nonlinear HUT subsystem was established. A more complicated equivalent circuit was simulated to represent this scenario, and the validity of the VI method was again confirmed through this PHIL experiment.

Figure 13 shows the setup for the PHIL simulation platform. The platform included a real-time digital simulator (RTDS). The OPS was simulated in the RTDS using RTDS Technologies' RSCAD graphical user interface (GUI) with a circuit simulation time step of 50 µs. An RTDS Giga-Transceiver Analogue Input (GTAI) card was used to import the feedback current signal. The reference output voltage signal was measured and transferred by a Giga-Transceiver Analogue Output (GTAO) card.

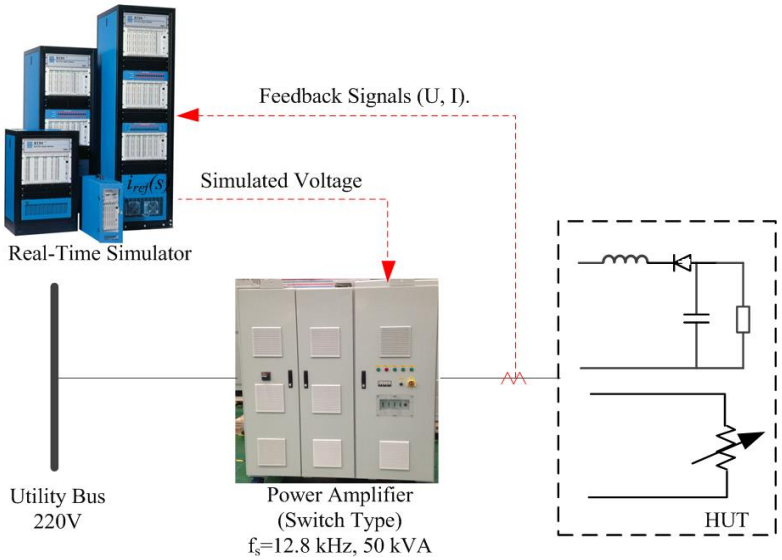

Figure 13. PHIL experimental setup.

A prototype of a three-phase switch-type PA was built and tested in the lab. It includes three independent H-inverters and possesses the ability to generate PWM voltages from a constant direct current (DC)-voltage source. Field-programmable gate array (FPGA; EP4C115F23I7N) and advanced RISC (reduced instruction set computer) machine (ARM; STM32F417ZGT6) processors are used to

control the PA. The switching frequency of the power amplifier is 12.8 kHz (with a sampling frequency of 25.6 kHz). The DC-link voltage is 450 V, and the output filter's parameters are equal to L_o = 0.2 mH and C_o = 60 μF. A PI controller is used as the output voltage regulator, with parameters of K_P = 6 and K_i = 200, and the active damping regulator applies a damping factor of K_c = 5. A total time delay of 100 μs is assumed for the IE. For further analysis and comparison, the voltages are represented as per-unit (p.u.) values.

Stability Analysis: The original circuit for the first scenario was simulated using the PHIL model as shown in Figure 14. It can be assumed that impedance Z_s is a combination of inductor L_s and resistor R_s and that impedance Z_l is a combination of inductor L_l and resistor R_l. The effects of different values of inductor L_s and inductor L_l on the simulation stability were investigated. Table 1 shows the simulation parameters used in the analysis.

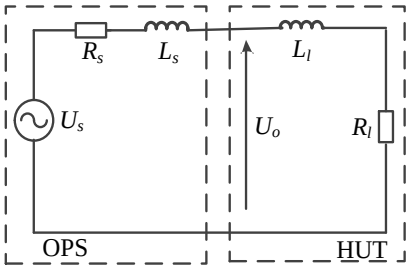

Figure 14. Topology used in the first PHIL simulation scenario, with a linear resistance/inductor (RL) load circuit.

Table 1. the value of the impedance Z_s and impedance Z_l.

Parameter	Value	Parameter	Value
R_s	2 Ω	R_l	2 Ω
L_s	Case (1): 2 mH Case (2): 4 mH Case (3): 2 mH	L_l	Case (1): 2 mH Case (2): 2 mH Case (3): 4 mH

The grid impedance Z_s(s) and the impedance Z_l(s) are set using the simulation parameters, which are shown in Table 1. The combined impedance Z_{lc}(s) and the compensated impedance $Z_{lc}{}'$(s) can be calculated using Equations (18) and (19):

$$Z_{lc}(s) = Z_l(s)/G_{IE}(s), \tag{18}$$

$$Z'_{lc}(s) = Z_{lc}(s)/G_{ES}(s) \cdot G_{EP}(s). \tag{19}$$

The frequency responses of the grid impedance $Z_s(s)$, the impedance Z_l(s), the combined impedance Z_{lc}(s), and the compensated impedance $Z_{lc}{}'$(s) are shown in Figure 15.

Figure 15a,b show that the phase difference between impedance $Z_s(s)$ and the uncompensated impedance Z_{lc}(s) approaches 180° when inductor L_s is greater than or equal to inductor L_l, indicating that the PM is negative ($PM < 0°$). Thus, the PHIL simulation is unstable. By contrast, when inductor L_s is smaller than inductor L_l, the simulation is stable. Figure 15c shows that in Case 3, there is no frequency intersection in the high-frequency range, as estimated using the impedance model. It is found that the compensated impedance $Z_{lc}{}'$(s) and impedance $Z_s(s)$ lead to critical stability. Thus, the stability of PHIL simulations can be improved using the VI method.

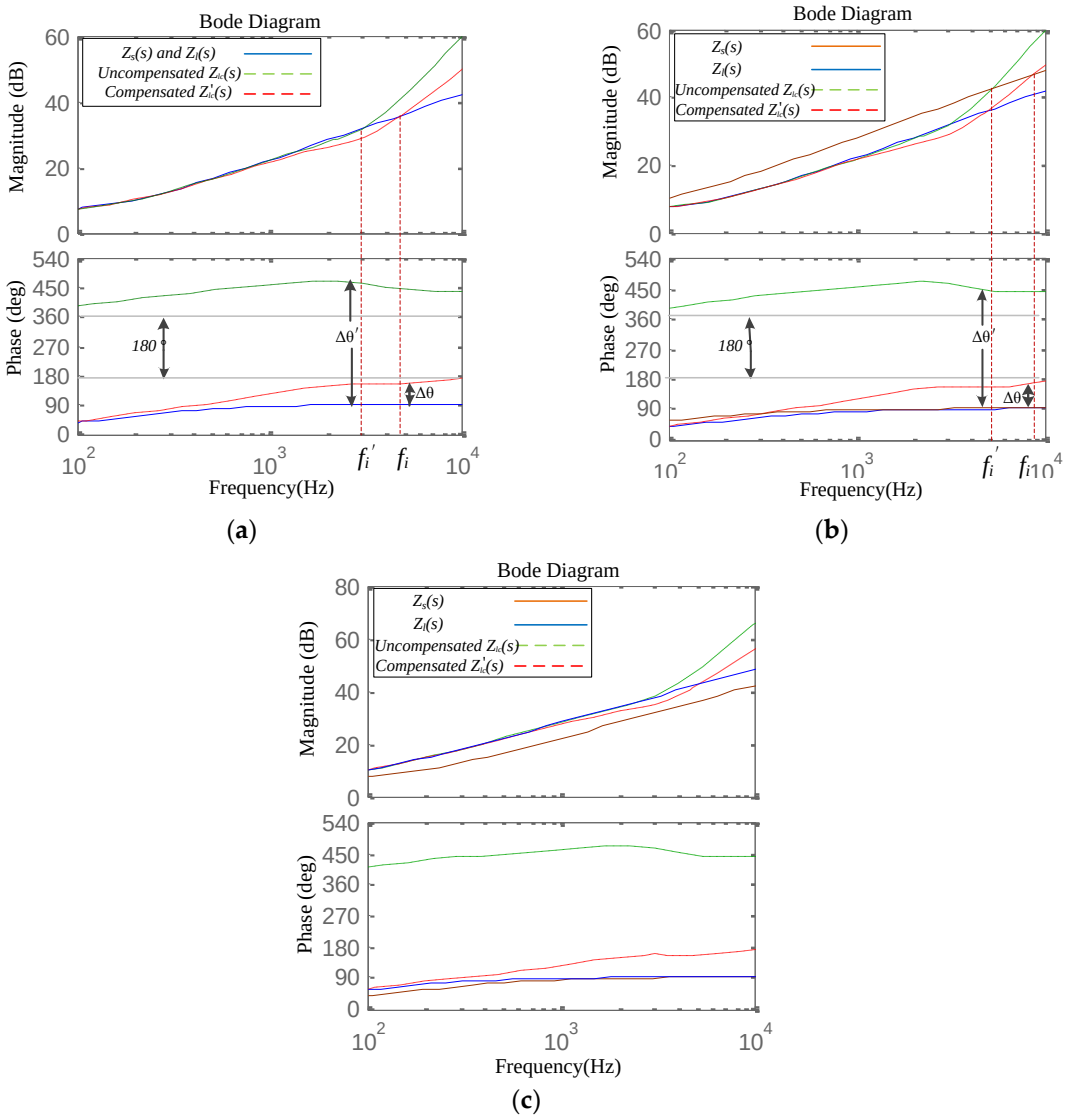

Figure 15. Frequency responses of different impedances Z_s(s) and Z_l(s), the combined impedance Z_{lc}(s), and the compensated impedance $Z_{lc}{}'$(s): (**a**) Case 1; (**b**) Case 2; and (**c**) Case 3.

Accuracy Analysis: To describe the accuracy of the PHIL simulation without compensation, Equation (13) can be simplified to

$$E(s) = \left| \frac{Z_l(s) - Z_{lc}(s)}{Z_l(s)} \right| = \left| 1 - \frac{1}{G_{IE}(s)} \right|. \tag{20}$$

The accuracy of the compensated PHIL system can be calculated as

$$E(s) = \left| \frac{Z_l(s) - Z_{lc}(s) G_{EP}(s)}{Z_l(s)} \right| = \left| 1 - \frac{G_{EP}(s)}{G_{IE}(s)} \right| \tag{21}$$

The impedance error of the PHIL simulation is illustrated in Figure 16. The compensated error that is calculated using Equation (21) is less than the uncompensated error calculated using Equation (20).

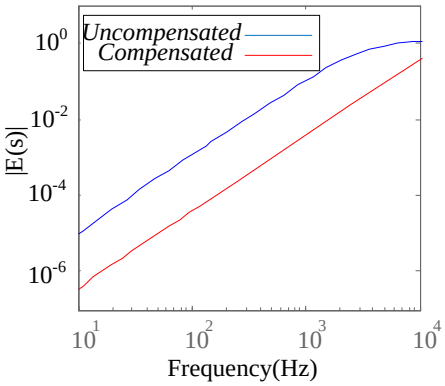

Figure 16. Diagram for evaluating the impedance accuracy of a PHIL simulation.

4.2. Experimental Results

To confirm the efficacy of the proposed method, two typical PHIL simulations were established and tested. The proposed method was compared with the typical ITM method [29], which is one of the most conventional and straightforward methods of implementing PHIL simulations.

Scenario 1: Hardware with Linear Behavior

As shown in Figure 14, the first considered scenario involved the resistor R and inductor L load circuit. The values of resistor R and inductor L are listed in Table 1. The simulation time step was set to 50 μs, and the parameters of the PA were designed as described in Section 4.1.

Simulations were operated with various values of inductor L_l and inductor L_s, and the output voltage waveforms and simulation errors for two cases are shown in Figures 17 and 18. Figures 17a and 18a show that the uncompensated PHIL simulation is unstable when inductor $L_s \geq L_l$, whereas Figures 17b and 18b show that the stability is significantly improved using the VI method.

Figure 19a,b show that when inductor $L_s < L_l$, the output voltage and the output voltage errors are improved, and Figure 19c shows that the accuracy is also improved. Thus, the effectiveness of the proposed method is confirmed.

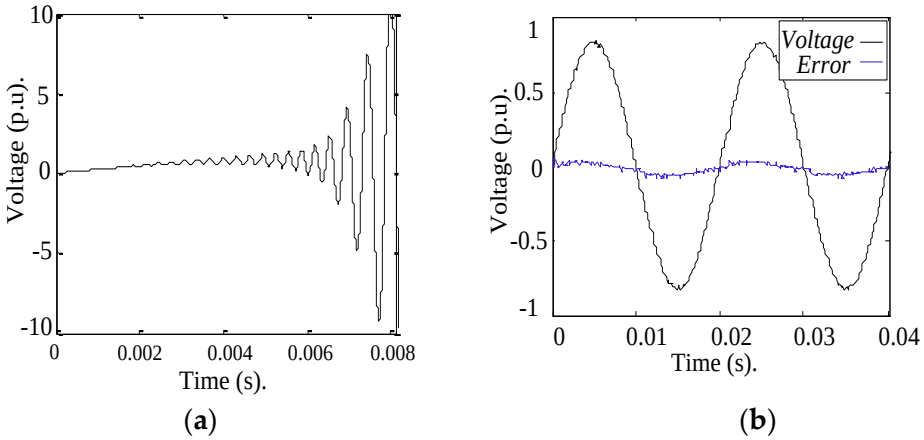

Figure 17. Scenario 1 simulation with L_s = 2 mH, R_s = 2 Ω, L_l = 2 mH, and R_l = 2 Ω: (**a**) uncompensated output voltage waveform and (**b**) compensated output voltage waveform.

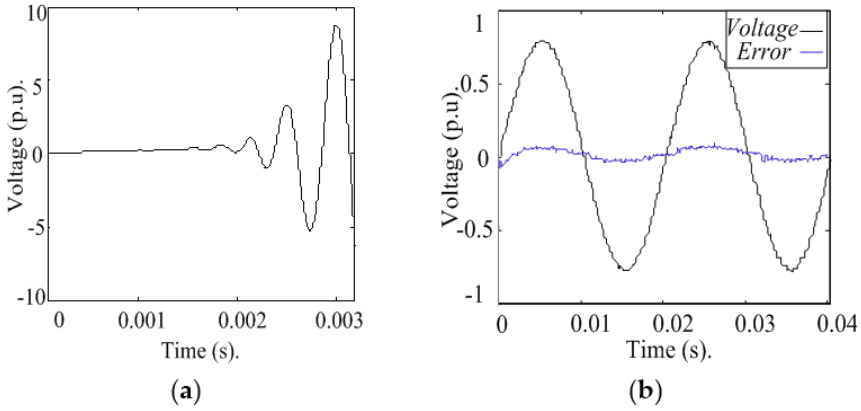

Figure 18. Scenario 1 simulation with L_s = 4 mH, R_s = 2 Ω, L_l = 2 mH, and R_l = 2 Ω: (**a**) uncompensated output voltage waveform; (**b**) compensated output voltage waveform.

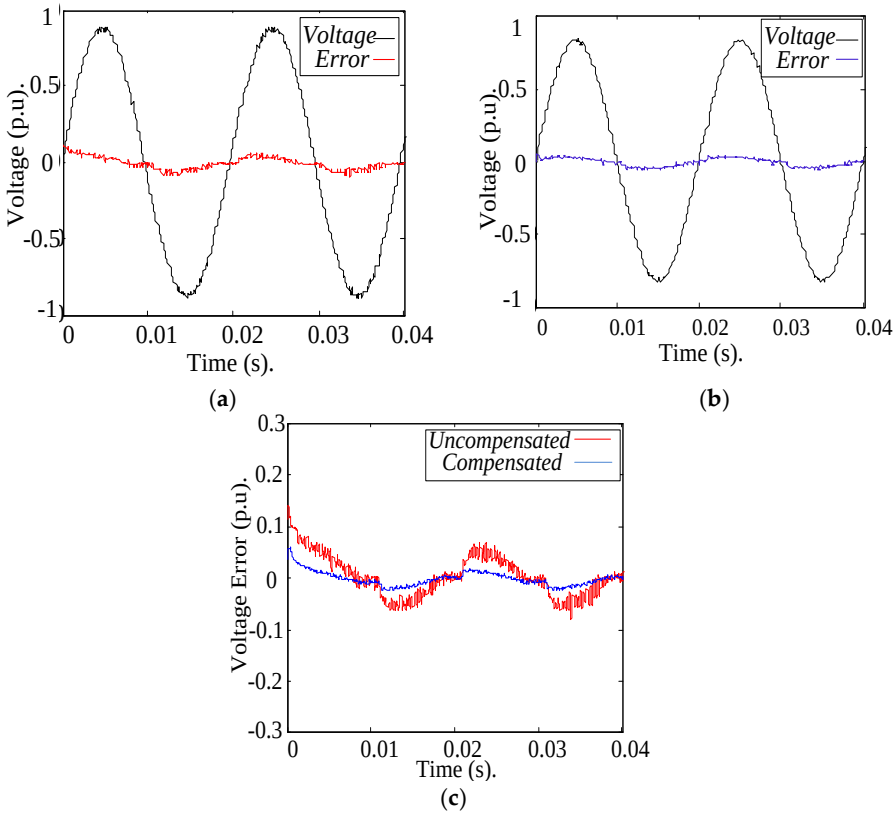

Figure 19. Scenario 1 simulation with L_s = 2 mH, R_s = 2 Ω, L_l = 4 mH, and R_l = 2 Ω: (**a**) uncompensated output voltage and error waveforms; (**b**) compensated output voltage and error waveforms; (**c**) magnified view of output voltage error waveforms.

Scenario 2: Hardware with Nonlinear Behavior

In practice, there are always nonlinear components on the HUT side. Thus, in the second considered PHIL scenario, a diode rectifier, which is a typical nonlinear device, is used. The circuit diagram is shown in Figure 20. In this case, the inductor is placed in series with a diode block, and a small capacitor is placed in parallel with the resistor. The parameters of the simulated circuit are shown in Figure 20. The simulation time step was set to 50 µs, and the parameters of the PA were designed as described in Section 4.1.

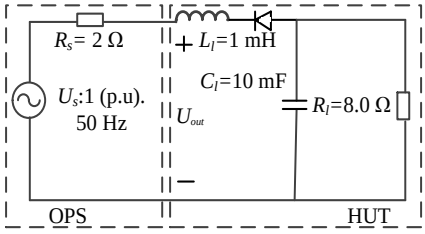

Figure 20. Topology used in the second PHIL simulation scenario, with a nonlinear load.

Figure 21 compares the experimental results for the uncompensated and compensated PHIL simulations. Better accuracy is achieved in the compensated PHIL simulation, confirming the effectiveness of the proposed compensation method.

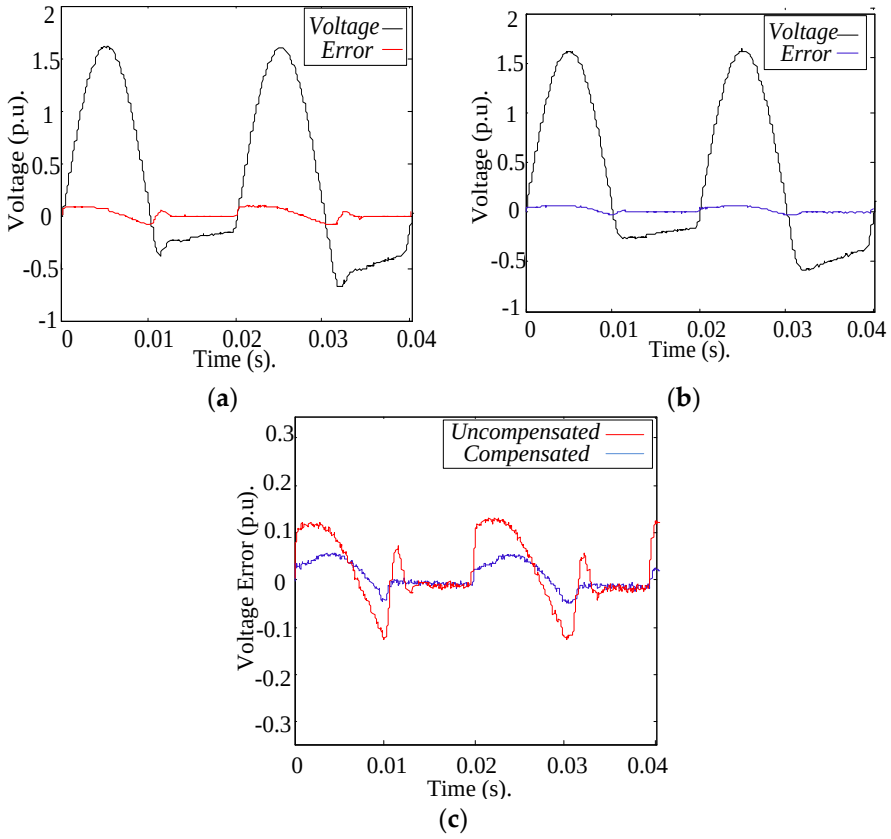

Figure 21. Scenario 2 simulation with R_s = 2Ω, L_l = 1 mH, C_l = 10 mF, and R_l = 8 Ω: (**a**) uncompensated output voltage and error waveforms; (**b**) compensated output voltage and error waveforms; and (**c**) view of output voltage error waveforms.

5. Conclusions

This paper presents an effective VI method for enhancing the stability and accuracy of PHIL simulations. The proposed VI method is easy to be implemented in a digital real-time simulator. The VI method offers greatly simplified implementation on the OPS side. Therefore, it is suitable for most practical PHIL simulations involving highly complex circuits and nonlinear components. Through the establishment of an impedance model for a PHIL simulation, the stability and accuracy of the system can be analyzed. Furthermore, the stability and accuracy of PHIL simulations can be improved using the VI method. Simulations of two typical PHIL cases (one linear HUT and one nonlinear HUT) are presented to demonstrate these improvements, thereby verifying the validity of the VI method.

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