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Design and Implementation of a GaN-Based Three-Phase Active Power Filter

Chao-Tsung Ma * and Zhen-Huang Gu

Department of Electrical Engineering, CEECS, National United University, Miaoli 36063, Taiwan;
M0621002@smail.nuu.edu.tw

* Correspondence: ctma@nuu.edu.tw; Tel.: +886-37-382482; Fax: +886-37-382488

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Abstract: Renewable energy (RE)-based power generation systems and modern manufacturing facilities utilize a wide variety of power converters based on high-frequency power electronic devices and complex switching technologies. This has resulted in a noticeable degradation in the power quality (PQ) of power systems. To solve the aforementioned problem, advanced active power filters (APFs) with improved system performance and properly designed switching devices and control algorithms can provide a promising solution because an APF can compensate for voltage sag, harmonic currents, current imbalance, and active and reactive powers individually or simultaneously. This paper demonstrates, for the first time, the detailed design procedure and performance of a digitally controlled 2 kVA three-phase shunt APF system using gallium nitride (GaN) high electron mobility transistors (HEMTs). The designed digital control scheme consists of three type II controllers with a digital signal processor (DSP) as the control core. Using the proposed APF and control algorithms, fast and accurate compensation for harmonics, imbalance, and reactive power is achieved in both simulation and hardware tests, demonstrating the feasibility and effectiveness of the proposed system. Moreover, GaN HEMTs allow the system to achieve up to 97.2% efficiency.

Keywords: gallium nitride (GaN); power switching device; active power filter (APF); power quality (PQ)

1. Introduction

In recent years, the rapid increase in the penetration level of renewable energy (RE)-based distributed power generation (DPG) has resulted in noticeable degradation in the voltage stability and power quality (PQ) of existing power systems. The intrinsic features of DPG systems include (1) intermittent power flow caused by the utilization of maximum power point tracking (MPPT) control functions and (2) harmonic current injections caused by various power converters using switching type control techniques. Moreover, modern technologies such as automatic manufacturing systems (AMS), Internet of Things (IoT), and Industry 4.0 require a large number of power converters based on high-switching frequency power electronic devices. It can be imagined that the combination of a variety of different harmonics in load currents and unbalanced active and reactive powers can negatively affect the PQ of power networks. In practice, there are a number of compensating schemes and devices commonly used for PQ improvement applications, such as capacitor banks, passive filters, series active power filters, shunt active power filters and their combinations. Of the reported methods, the active power filter (APF) is a very widely adopted solution because, with appropriate control strategy, it is capable of providing simultaneous compensation for voltage sag, harmonic current, imbalance, and active and reactive powers. Moreover, with an external energy source and/or energy storage devices, it can also be used as an uninterruptible power supply (UPS). The main unit of an APF system is a power converter that performs the desired PQ control functions through proper

switching control of power electronic devices. An APF is usually connected to the point of common coupling (PCC) in parallel or series to perform its designed functions; however, shunt APFs are more commonly used because they provide more flexible compensation functions through current-injecting control and require less auxiliary equipment. When a series APF and a shunt APF are connected with a common direct current (DC) link, they can be used simultaneously, known as a unified power quality conditioner (UPQC) [1–4].

In open literature, there are a lot of papers investigating the application of APF to the mitigation of PQ issues, such as the improvement of PCC voltage stability [5,6], compensation of harmonic currents [5–7] and unbalance load currents [7,8], injection of active power [8,9], regulation of reactive power [6,9], etc. In order to develop high-performance APFs, it is crucial to improve the switching performance of power converters. In other words, it is very desirable to achieve higher efficiency, shorter response time, and higher power density of power converters used in APFs. To realize the aforementioned objective, wide-bandgap (WBG)-based power switching devices offer a promising solution. Gallium nitride (GaN) is a widely discussed WBG semiconductor material that benefits power-switching device technology with higher voltage, higher switching frequency, higher power, and better high-temperature capability in power switches compared with conventional silicon (Si)-based technologies. It has been expected that GaN high electron-mobility transistors (HEMTs) can greatly enhance the performance of power converters with less than 1-kV power switching requirement [10–12]. However, in open literature, the published papers on GaN HEMTs mostly address the manufacturing, device characteristics, driving, and switching performances [13]. Only two papers regarding GaN-based single-phase APFs were found in the Institute of Electrical and Electronics Engineers (IEEE)/Institution of Engineering and Technology (IET) Electronic Library (IEL) and ScienceDirect OnSite (SDOS) databases [14,15]. In [14], a GaN-based single-phase APF with a modified sigma-delta modulator technique was proposed and verified with simulation studies. In [15], a 5kW single-phase hybrid APF with a new control system was proposed to improve the system performance. There are currently few papers addressing the design issues and reporting performances of GaN-based three-phase inverters in practical application cases. As a result, this paper presents the key design procedure and demonstrates for the first time the performance of a 2-kVA GaN-based three-phase shunt APF system.

Following the introduction in this section, the next section will briefly describe the features of GaN HEMTs and its driving requirements. The third section addresses the mathematical modeling and control strategy of the proposed GaN-based three-phase APF based on synchronous reference frame (SRF) theory. In the fourth section, the proposed APF and control system are simulated using a comprehensive PQ control scenario. Hardware implementation and a test of a 2 kVA prototype are carried out in the fifth section. The sixth section provides some discussions on key technical issues related to the proposed GaN based three-phase APF. Finally, this paper is concluded in the last section.

2. Gallium Nitride (GaN) High Electron-Mobility Transistor (HEMT) and Its Driving Requirements

GaN HEMTs are believed to be the most promising solution for low- to medium-power applications because of their advantages such as higher breakdown voltage, lower on-resistance, and higher switching speed compared with conventional Si-based switching devices; these advantages can increase system efficiency and power density significantly and thus lead to new opportunities for achieving power converters with improved performance. Commercially available GaN HEMTs now achieve up to 650 V/50 A and 900 V/15 A [13].

There are normally on and normally off GaN HEMTs. Normally on GaN HEMTs, also known as depletion mode (D mode) GaN HEMTs, are not popular because normally off switching devices are a common requirement for power converter applications. On the other hand, normally off GaN HEMTs such as enhancement mode (E mode) GaN HEMTs and cascode GaN HEMTs can be turned on with positive V_{GS} and turned off with zero or negative V_{GS} . Generally, the turn-on threshold and highest allowed driving voltages of a GaN HEMT are much smaller than those of conventional Si-based

switches. As a result, the careful design of driving circuit is necessary in order to avoid fault turn-on and high overshoot. Common suggestions include providing separate turn-on and turn-off driving paths, achieving minimized overlapping between driving and power loops, using Miller clamp and negative voltage sources to ensure reliable turn-offs, etc. [13].

3. Mathematical Modeling and Control Algorithms of GaN-Based Active Power Filter (APF)

3.1. GaN-Based Three-Phase Active Power Filter

The main power electronic circuit in a three-phase shunt APF system is a three-phase inverter. The main control functions in an APF are to adjust the DC link voltage of the three-phase inverter to the rated value and to compensate reactive power, unbalanced current and harmonic components of the load as required. The circuit architecture of the proposed three-phase inverter is shown in Figure 1. The DC link voltage control adopts dual-loop control schemes, where the inner loop controls inductor currents, and the outer loop controls DC link voltage. By controlling the inductor currents, the goals of regulating DC link voltage and compensating harmonics, unbalanced and reactive components of load currents can be achieved.

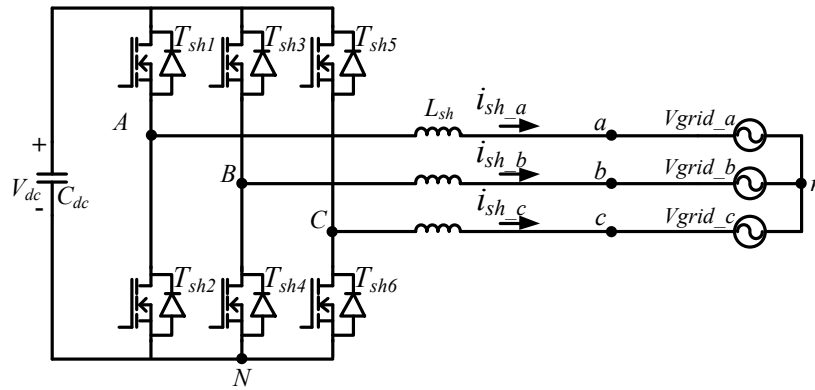


Figure 1. Shunt three-phase inverter.

The circuit specifications of the proposed three-phase inverter developed in this paper are the following: the three-phase line to line voltage of the grid = $110 V_{rms}$, grid frequency = 60 Hz, rated power = 2 kVA, DC link voltage = 200 V, switching frequency = 50–100 kHz, DC voltage sensing factor = 0.012, AC current sensing factor = 0.05, AC voltage sensing factor = 0.0062, and DC voltage variation limit = 1%.

3.2. Design of Direct Current (DC) Capacitor and Filter Inductors

The main function of the DC link capacitor is to stabilize DC link voltage. If the DC link capacitance is too large, the dynamic response of the DC link voltage will be slow, and the cost of the APF hardware system will be increased; if the DC capacitor is too small, it will be difficult to suppress the disturbance caused by external power flow. In order to design the appropriate size of the capacitor, we first define instantaneous power of the DC link:

$$P_{dc} = V_{dc}I_{dc} = (\bar{V}_{dc} + \tilde{V}_{dc})(\bar{I}_{dc} + \tilde{I}_{dc}), \quad (1)$$

where V_{dc} and I_{dc} represent DC voltage and current, respectively, which can both be separated into their respective DC components ($\bar{V}_{dc}$ and $\bar{I}_{dc}$) and AC components ($\tilde{V}_{dc}$ and $\tilde{I}_{dc}$). In order to simplify the analysis, we make three assumptions: the conversion efficiency of the three-phase inverter is 100%,

$\widetilde{V}_{dc}$ is considered zero, and $\bar{I}_{dc}$ is considered zero because $\widetilde{I}_{dc}$ is generally far larger than $\bar{I}_{dc}$. As a result, we obtain the following:

$$P_{dc} \cong \bar{V}_{dc} \widetilde{I}_{dc}(t) = \bar{V}_{dc} C_{dc} \frac{d\widetilde{V}_{dc}(t)}{dt}, \quad (2)$$

where C_{dc} represents DC link capacitance. Then, we obtain the voltage variation of the DC link capacitor:

$$\widetilde{V}_{dc}(t) = \frac{1}{C_{dc} \bar{V}_{dc}} \int_0^t P_{dc}(t) dt, \quad (3)$$

where $\int_0^t P_{dc}(t) dt$ represents the capacity of the three-phase inverter. Then, we obtain DC link capacitance:

$$\Delta V_{dc} = \frac{S}{f_{sw} C_{dc} \bar{V}_{dc}} \Rightarrow C_{dc} = \frac{S}{f_{sw} \Delta V_{dc} \bar{V}_{dc}}, \quad (4)$$

where f_{sw} represents the switching frequency. It should be noted that if an electrolytic capacitor were used for this APF design case, a higher capacitor specification will be required.

The function of the filter inductors is to filter out current ripples caused by the switching of the shunt three-phase inverter. Large inductances suppress the ripples of inductor currents but reduce the response speed of current controllers. On the other hand, although small inductances improve the response speed of the current controller, they cause large current ripples. Therefore, the inductances can be adjusted according to the actual situation. In order to design the filter inductances, we first need the following inductor voltage equation:

$$v(t) = L_{sh} \frac{di_{sh}(t)}{dt}, \quad (5)$$

where L_{sh} represents inductance value, and i_{sh} represents inductor current. According to the relationship between voltage and current on an inductor, (5) can be expressed as follows.

$$\Delta I_{sh} = \frac{\frac{D}{2} \times T_{sw} \times (V_{dc} - V_{grid})}{L_{sh}}, \quad (6)$$

where ΔI_{sh} represents shunt inductor current ripple, D represents duty cycle, T_{sw} represents switching period, and V_{grid} represents grid voltage. The duty cycle can be expressed the following:

$$D(\omega t) = m_a \sin(\omega t), \quad (7)$$

where m_a represents modulation factor and equals modulation signal divided by triangular wave amplitude (v_{con}/v_{tri}). Then, we get output AC voltage:

$$V_{sh}(\omega t) = V_{dc} m_a \sin(\omega t). \quad (8)$$

Substituting (7) and (8) into (6) yields the following:

$$\Delta I_{sh} = \frac{V_{dc} \times T_{sw}}{2L_{sh}} m_a \sin(\omega t) [1 - m_a \sin(\omega t)]. \quad (9)$$

Then, we differentiate (9) and let the result be zero in order to obtain the maximum value of inductor current ripple:

$$\frac{d\Delta I_{sh}(\omega t)}{d\omega t} = \frac{V_{dc} T_{sw}}{2L_{sh}} m_a [\cos(\omega t) - 2m_a \sin(\omega t) \cos(\omega t)] = 0. \quad (10)$$

As a result,

$$\sin(\omega t) = \frac{1}{2m_a}. \quad (11)$$

Lastly, substituting (11) into (9) yields the following equation:

$$L_{sh} = \frac{V_{dc}}{8f_{sw}\Delta I_{sh}}. \quad (12)$$

According to the circuit specifications of the three-phase inverter and commonly assumed inductor current ripple, 10% of output current, it is calculated that the required inductance should be at least larger than 500 μH .

3.3. Mathematical Modeling and Controller's Design for GaN-Based Shunt APF

3.3.1. Mathematical Modeling

The mathematical model of the shunt-connected three-phase inverter can be derived according to Figure 1. First, the following equations are obtained with Kirchhoff's voltage law:

$$L_{sh} \frac{di_{sh_a}}{dt} = v_{AN} - v_{grid_a} - v_{nN}, \quad (13)$$

$$L_{sh} \frac{di_{sh_b}}{dt} = v_{BN} - v_{grid_b} - v_{nN}, \quad (14)$$

$$L_{sh} \frac{di_{sh_c}}{dt} = v_{CN} - v_{grid_c} - v_{nN}, \quad (15)$$

where i_{sh_a} , i_{sh_b} , and i_{sh_c} represent three-phase inductor currents, v_{AN} , v_{BN} , and v_{CN} represent switching point voltages, v_{grid_a} , v_{grid_b} , and v_{grid_c} represent three-phase grid voltages, and v_{nN} represents the voltage between the grid ground and the inverter ground. Also, the three-phase three-wire system satisfies the following condition:

$$i_{sh_a} + i_{sh_b} + i_{sh_c} = 0. \quad (16)$$

As a result, v_{nN} can be expressed as the following:

$$v_{nN} = \frac{(v_{AN} + v_{BN} + v_{CN}) - (v_{grid_a} + v_{grid_b} + v_{grid_c})}{3}. \quad (17)$$

Substituting Equation (17) into Equations (13)–(15) yields the following:

$$\begin{bmatrix} L_{sh} \frac{di_{sh_a}}{dt} \\ L_{sh} \frac{di_{sh_b}}{dt} \\ L_{sh} \frac{di_{sh_c}}{dt} \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ -\frac{1}{2} & 1 & -\frac{1}{2} \\ -\frac{1}{2} & -\frac{1}{2} & 1 \end{bmatrix} \begin{bmatrix} v_{AN} \\ v_{BN} \\ v_{CN} \end{bmatrix} - \begin{bmatrix} v_{grid_a} \\ v_{grid_b} \\ v_{grid_c} \end{bmatrix}. \quad (18)$$

In this study, pulse width modulation (PWM) is used in the control, where the three-phase modulation signals v_{cona} , v_{conb} , and v_{conc} are compared with v_{tri} respectively to trigger the switches of all three switching legs. The output voltages of the switching legs can be expressed as follows:

$$v_{aN} = \left(\frac{1}{2} + \frac{v_{cona}}{2v_{tri}}\right)V_{dc}; \quad (19)$$

$$v_{bN} = \left(\frac{1}{2} + \frac{v_{conb}}{2v_{tri}}\right)V_{dc}; \quad (20)$$

$$v_{cN} = \left(\frac{1}{2} + \frac{v_{conc}}{2v_{tri}}\right)V_{dc}. \quad (21)$$

Substituting Equations (19)–(21) into Equation (18) and letting $V_{dc}/2V_{tri} = K_{pwm}$ yield the following:

$$\begin{bmatrix} L_{sh} \frac{di_{sh_a}}{dt} \\ L_{sh} \frac{di_{sh_b}}{dt} \\ L_{sh} \frac{di_{sh_c}}{dt} \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ -\frac{1}{2} & 1 & -\frac{1}{2} \\ -\frac{1}{2} & -\frac{1}{2} & 1 \end{bmatrix} (K_{pwm} \begin{bmatrix} v_{cona} \\ v_{conb} \\ v_{conc} \end{bmatrix} - \begin{bmatrix} v_{grid_a} \\ v_{grid_b} \\ v_{grid_c} \end{bmatrix}). \quad (22)$$

Using SRF theory, Equation (22) can be converted into the following:

$$\begin{bmatrix} L_{sh} \frac{di_{sh_d}}{dt} \\ L_{sh} \frac{di_{sh_q}}{dt} \\ L_{sh} \frac{di_{sh_0}}{dt} \end{bmatrix} = K_{pwm} \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} v_{cond} \\ v_{conq} \\ v_{con0} \end{bmatrix} - \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} V_{grid_d} \\ V_{grid_q} \\ V_{grid_0} \end{bmatrix} - \begin{bmatrix} 0 & \omega L_{sh} & 0 \\ -\omega L_{sh} & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_{sh_d} \\ I_{sh_q} \\ I_{sh_0} \end{bmatrix}. \quad (23)$$

3.3.2. Design of Current Controllers

According to Equation (23), we can obtain block diagrams of direct-quadrature axis (d-q axis) current loops with type-II controllers as shown in Figures 2 and 3, where k_s and k_v represent AC current and voltage-sensing factors, respectively. Under ideal feed-forward conditions, the transfer function of current loop (d-axis or q-axis) is as follows:

$$H_i(s) = \frac{k_s K_{pwm}}{s L_{sh}}. \quad (24)$$

The transfer function of the adopted type II controller, which consists of a proportional-integral (PI) controller and a low pass filter (LPF), is as follows:

$$G_i(s) = \frac{k(s+z)}{s(s+p)}. \quad (25)$$

The loop gain can be expressed as follows:

$$L_i(s) = G_i(s)H_i(s) = \frac{k(s+z)}{s(s+p)} \frac{k_s K_{pwm}}{s L_{sh}}. \quad (26)$$

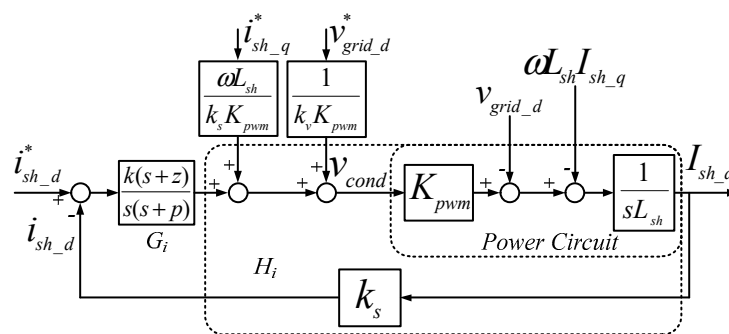


Figure 2. Block diagram of d-axis current controller.

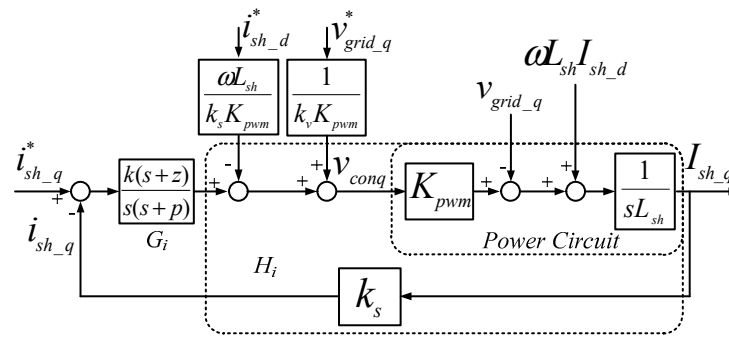


Figure 3. Block diagram of q-axis current controller.

In this application case, the crossover frequency of a Type II controller is designed within the range of 1/4 to 1/10 of the switching frequency. This paper chooses the controller crossover frequency to be 1/10 of the switching frequency, the zero is designed at 1/4 of the crossover frequency, and the cut-off frequency of the LPF is designed to be 15 kHz:

$$\omega_i = 0.1 \times 50k \times 2\pi = 31416 \text{ rad/s.} \quad (27)$$

$$z = \omega_i / 4 = 7854 \text{ rad/s.} \quad (28)$$

$$p = 2\pi \times 15k = 94248 \text{ rad/s.} \quad (29)$$

It follows that the gain of the plant at crossover frequency (Gain_{Hi}) is as follows:

$$\begin{aligned} \text{Gain}_{\text{Hi}} &= \frac{k_s K_{\text{pwm}}}{s L_{\text{sh}}} = \frac{2000}{j\omega} = 0 - j0.0637 \\ \Rightarrow |\text{Gain}_{\text{Hi}}| &= 0.0637 \end{aligned} \quad (30)$$

The gain of the controller at crossover frequency (Gain_{Gi1}) is as follows:

$$\begin{aligned} \text{Gain}_{\text{Gi1}} &= \frac{(s+z)}{s(s+p)} = \frac{j\omega_i + 7854}{j\omega_i(j\omega_i + 94248)} = 8.7535 \times 10^{-6} - j5.5704 \times 10^{-6} \\ \Rightarrow |\text{Gain}_{\text{Gi1}}| &= 1.0376 \times 10^{-5} \end{aligned} \quad (31)$$

Then, the required gain for compensation at crossover frequency can be calculated:

$$k = \frac{1}{|\text{Gain}_{\text{Hi}}| \times |\text{Gain}_{\text{Gi1}}|} = 1.5139 \times 10^6. \quad (32)$$

Finally, the transfer function is obtained as follows:

$$G_i(s) = \frac{1.5139 \times 10^6 (s + 7854)}{s(s + 94248)}. \quad (33)$$

The designed k_p and k_i are 16.0633 and 2.5232956, respectively. Figure 4 shows the Bode plot of the controller and plant, where the designed phase margin is 58 degrees.

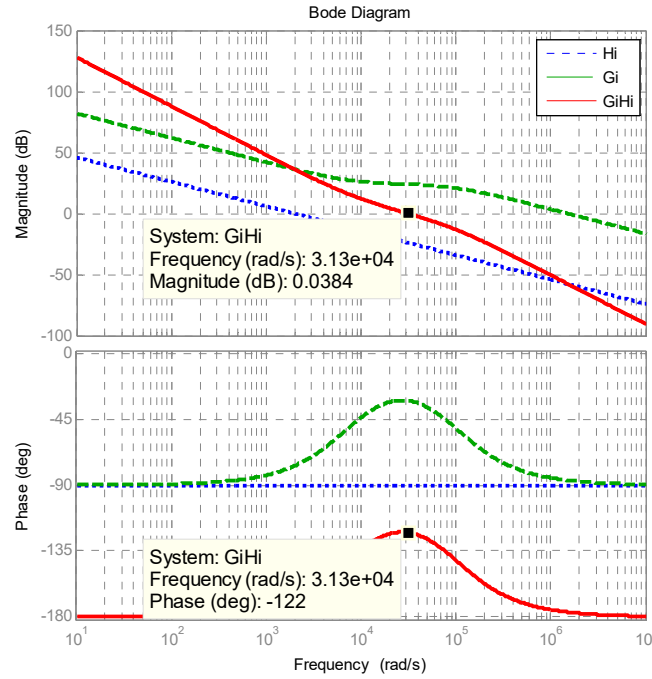


Figure 4. Bode plot of shunt active power filter (APF) inductor current control loop.

3.3.3. Design of DC Link Voltage Controller

The DC link voltage control loop regulates the real power balancing between the alternating current (AC) and DC terminals of the three-phase inverter. By ignoring steady-state operating point, we can obtain equivalent small signal model of the voltage loop as shown in Figure 5.

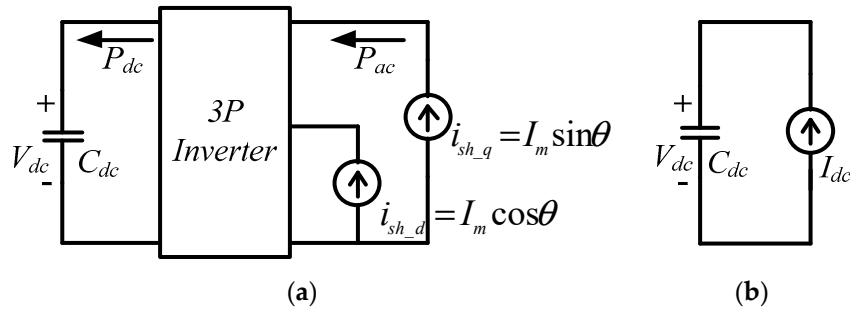


Figure 5. Equivalent circuits of the voltage control loop: (a) equivalent circuit under synchronous reference frame; (b) equivalent circuit on direct current (DC) side.

The instantaneous AC power at the AC side can be defined as follows:

$$P_{ac} = V_m \sin \theta * I_m \sin \theta + V_m \cos \theta * I_m \cos \theta, \quad (34)$$

where V_m and I_m represent the maximum voltage and current under dq axes, respectively. According to trigonometric functions, Equation (34) can be simplified as follows:

$$P_{ac} = V_m I_m. \quad (35)$$

Mapping the AC side signals onto the DC side and assuming that the inverter is lossless, we obtain the following:

$$P_{ac} = P_{dc}; \quad (36)$$

$$V_m I_m = V_{dc} I_{dc}. \quad (37)$$

Then, we can obtain the relationship between the DC side current and the AC side current:

$$I_{dc} = \frac{V_m}{V_{dc}} I_m = k_{dc} I_m; \quad (38)$$

$$C_{dc} \frac{dV_{dc}}{dt} = I_{dc} \Rightarrow V_{dc} = I_{dc} \frac{1}{sC_{dc}}, \quad (39)$$

where k_{dc} represents the conversion factor from AC side to DC side. According to Equations (38) and (39), we can obtain the transfer function of DC side voltage:

$$\frac{V_{dc}}{I_m} = \frac{k_{dc}}{sC_{dc}}, k_{dc} = \frac{V_m}{V_{dc}}. \quad (40)$$

According to the above derivations, we can obtain the block diagram of a DC link voltage control loop with a type-II controller as shown in Figure 6, where k_{vd} and k_s represent the sensing factors of DC voltage and AC current, respectively. Therefore, the transfer function of the DC voltage loop is as follows:

$$H_{dc}(s) = \frac{k_{vd}k_{dc}}{k_s C_{dc} s}. \quad (41)$$

The transfer function of the Type II controller is defined as follows:

$$G_v(s) = \frac{k(s+z)}{s(s+p)}. \quad (42)$$

It follows that the loop gain can be expressed as follows:

$$L_v(s) = G_v(s)H_{dc}(s) = \frac{k(s+z)}{s(s+p)} \frac{k_{vd}k_{dc}}{k_s C_{dc} s}. \quad (43)$$

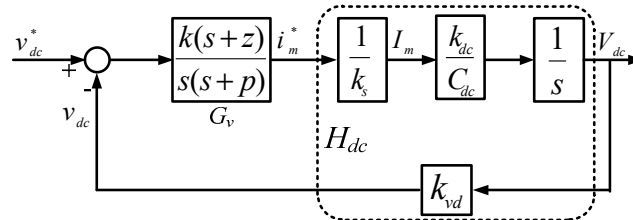


Figure 6. Block diagram of DC voltage loop type II controller.

The main purpose of the Type II controller is to use an LPF to reduce possible interference affecting the DC link when the APF system compensates for PQ problems such as imbalance and harmonics in three-phase load currents. The crossover frequency is set at 1/500 of that of the current loop, the cut-off frequency of the LPF is set at 49 Hz, and the zero is designed at 1/5 of the crossover frequency of the DC loop:

$$\omega_v = \omega_i \times 0.002 = 62.832 \text{ rad/s}; \quad (44)$$

$$p = 2\pi \times 49 = 307.8768 \text{ rad/s}; \quad (45)$$

$$z = \omega_v/5 = 12.5664 \text{ rad/s}. \quad (46)$$

The gain of the plant at crossover frequency ($\text{Gain}_{H_{dc}}$) can be calculated as follows:

$$\begin{aligned} \text{Gain}_{H_{dc}} &= \frac{k_{vd}k_{dc}}{k_s C_{dc} s} = \frac{118.9}{j\omega_v} \\ &= 0 - j1.8917 \Rightarrow |\text{Gain}_{H_{dc}}| = 1.8917 \end{aligned} \quad (47)$$

The gain of the controller at the crossover frequency (Gain_{Gv1}) is as follows:

$$\begin{aligned}\text{Gain}_{\text{Gv1}} &= \frac{(s+z)}{s(s+p)} = \frac{j\omega_v + 12.57}{j\omega_v(j\omega_v + 307.88)} \\ &= 0.003 - j0.0013 \\ \Rightarrow |\text{Gain}_{\text{Gv1}}| &= 0.0032\end{aligned}\quad (48)$$

Then, the required gain compensation at the designed crossover frequency can be calculated by:

$$k = \frac{1}{|\text{Gain}_{\text{Hdc}}| \times |\text{Gain}_{\text{Gv1}}|} = 165.1953. \quad (49)$$

Finally, the transfer function of the voltage controller is obtained:

$$G_v(s) = \frac{165.1953(s + 12.5664)}{s(s + 307.8768)}. \quad (50)$$

The designed k_p and k_i are 0.5286 and 0.0001329397, respectively. Figure 7 shows the Bode plot of the controller and plant, where phase margin is 67 degrees.

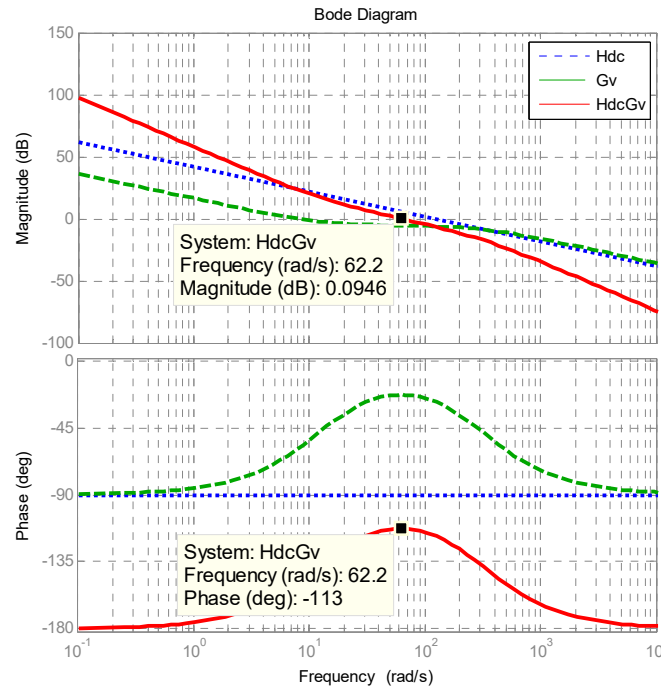


Figure 7. Bode plot of shunt APF inductor DC link voltage control loop.

3.3.4. Load Current Compensation Signals of APF

Using the SRF conversion technique, distorted and unbalanced three-phase load currents can be expressed as follows:

$$\begin{bmatrix} i_{Ld} \\ i_{Lq} \end{bmatrix} = \begin{bmatrix} \bar{i}_{Ld} \\ \bar{i}_{Lq} \end{bmatrix} + \begin{bmatrix} \tilde{i}_{Ld} \\ \tilde{i}_{Lq} \end{bmatrix}, \quad (51)$$

where i_{Ld} and i_{Lq} represent dq-axis load currents, $\bar{i}_{Ld}$ and $\bar{i}_{Lq}$ represent dq-axis load currents with the fundamental frequency, and $\tilde{i}_{Ld}$ and $\tilde{i}_{Lq}$ represent the dq-axis components that require compensation. In order to obtain the compensation signals of the active current (q axis) i_{Lq}^* , i_{Lq} is firstly filtered with an LPF and then subtracted from q-axis current feedback signal (i_{Lq}), while the compensation signals of the reactive current (d axis) i_{Ld}^* equals the whole d-axis current feedback signal (i_{Ld}), as shown in Figure 8.

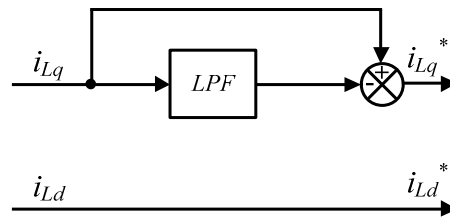


Figure 8. The direct-quadrature axis currents compensation signals of the APF.

3.4. Complete System of GaN-Based Shunt APF

According to Figure 8, DC link voltage controller, and inductor current controllers, we can obtain the circuit configuration of the proposed GaN based three-phase APF system with the block diagram of complete control architecture, as shown in Figure 9.

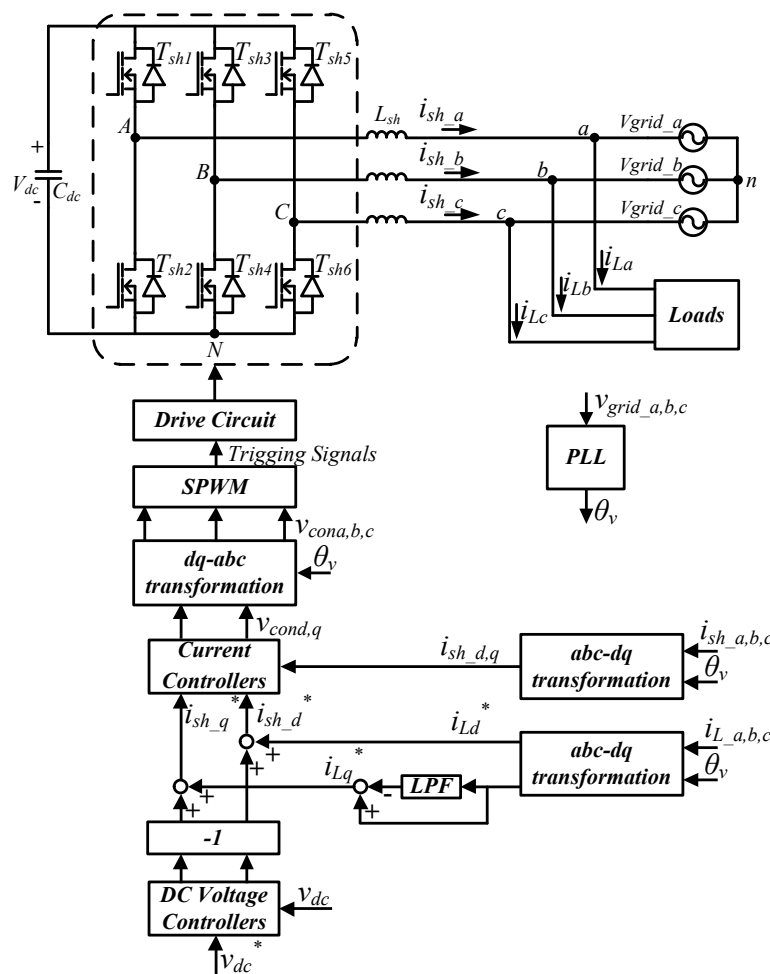


Figure 9. The circuit configuration of gallium nitride (GaN)-based shunt APF system and the block diagram of the control scheme.

4. Simulation Study and Results

With the design presented in the previous section, the proposed Gan-based shunt-type APF is tested for an integrated compensation of multiple power quality problems, including current harmonics, load current imbalance, and reactive currents. Powersim (PSIM) software is used to perform the simulation case of the abovementioned comparison tasks. The PSIM simulation model is shown in Figure 10.

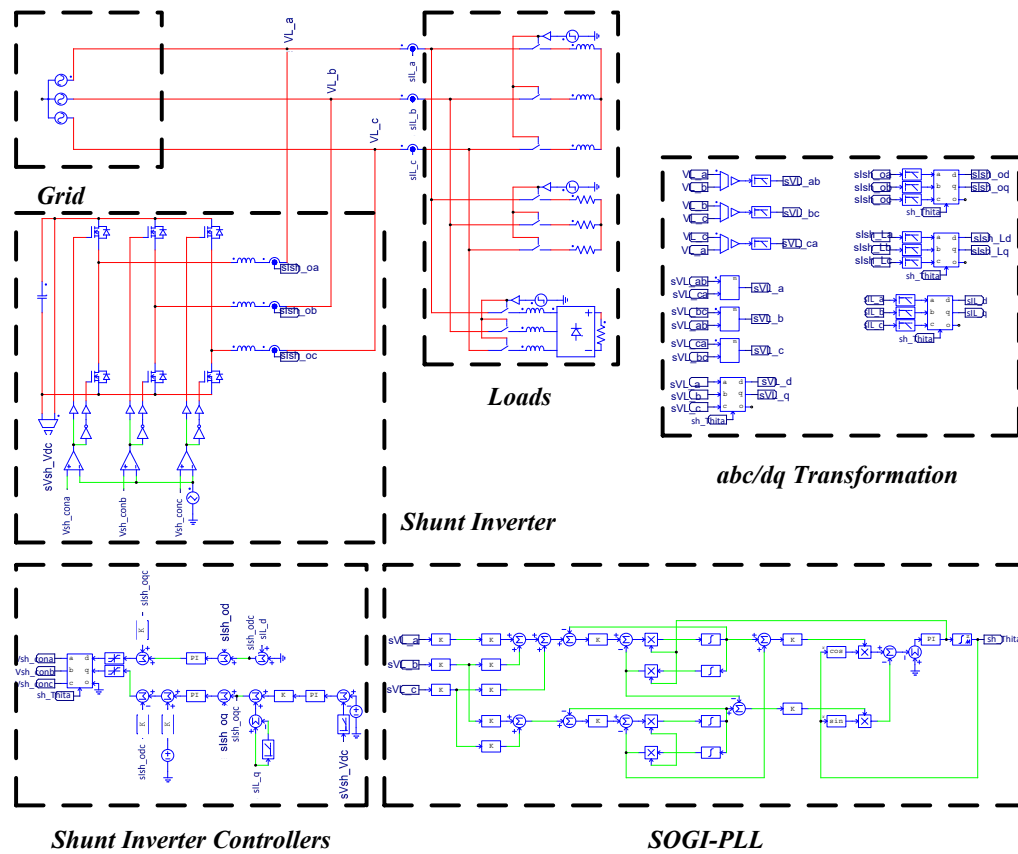


Figure 10. Powersim (PSIM) simulation model of the proposed APF system.

4.1. Simulation Scenario

To demonstrate the performance of the proposed controllers, the integrated compensation for multiple load current quality problems with APF is simulated. In this case, the three-phase load bank consists of a balanced reactive load, an unbalance resistive load, and a non-linear load, as shown in Figure 11. Table 1 shows the detailed values of the loads used. At first (t_0 – t_1), the shunt APF, connected to a three-phase power grid with the line to line voltage of 110 V, 60 Hz, adjusts the DC link voltage to 200 V and the compensation function is not activated; at t_1 , compensation is activated to achieve a set of balanced grid currents, zero distortion, and unit power factor (PF), as shown in Figure 12. Figures 13–17 show the corresponding simulation results, and Table 2 shows root-mean-square (RMS) currents and total harmonic distortion (THD) data before and after compensation.

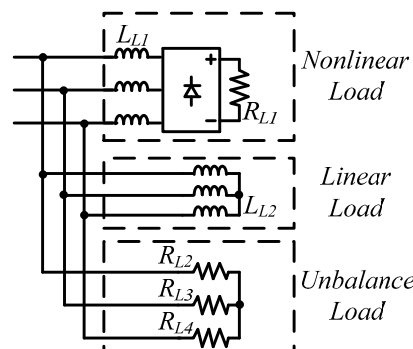
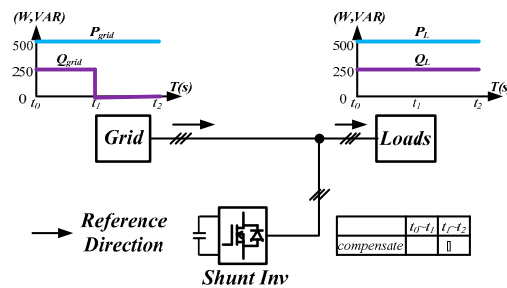
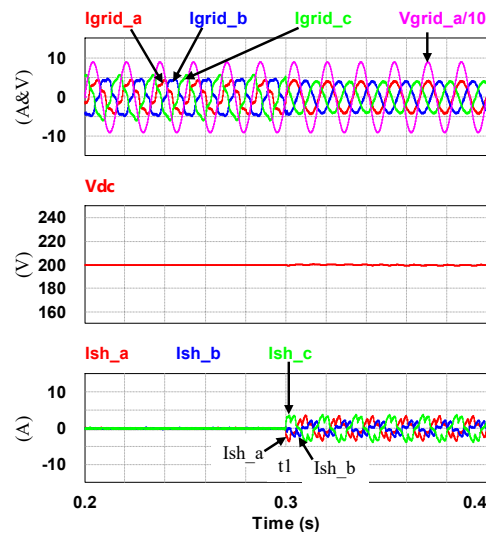
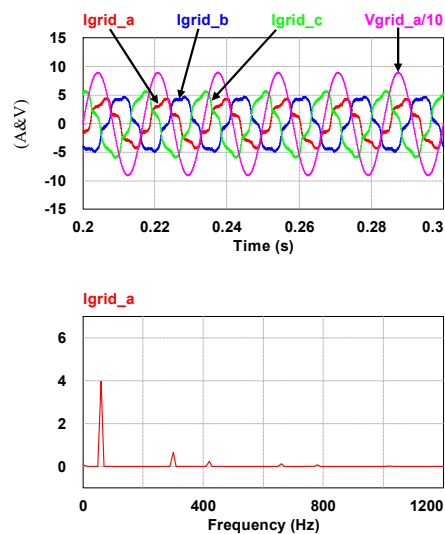


Figure 11. Load condition in simulated scenario.

Table 1. Load parameters for simulation scenario.

Nonlinear Load		Linear Load	Unbalanced Load	
R_{L1}	L_{L1}	L_{L2}	R_{L2}	R_{L3}, R_{L4}
$50\ \Omega$	$6\text{ mH} \times 3$	$152\text{ mH} \times 3$	$\infty\ \Omega$	$50\ \Omega$

**Figure 12.** Schematic diagram of simulated scenario.**Figure 13.** The grid-side phase-a voltage and three-phase currents/DC link voltage/shunt APF three-phase currents (t_0 – t_2).**Figure 14.** Before t_1 : the grid phase-a voltage and three-phase currents/the fast Fourier transform (FFT) waveform of the grid phase-a current.

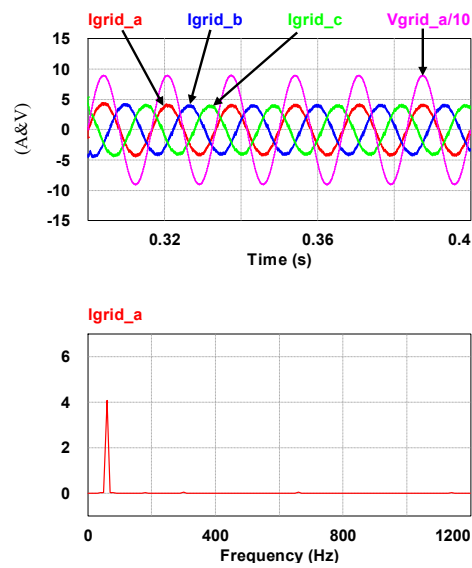


Figure 15. After t_1 : the grid phase-a voltage and three-phase currents/FFT waveform of the grid phase-a current.

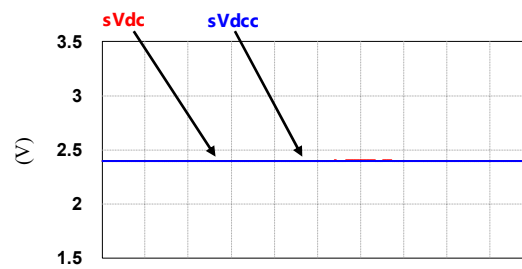


Figure 16. Shunt APF DC link voltage command and feedback signals (t_0 – t_2).

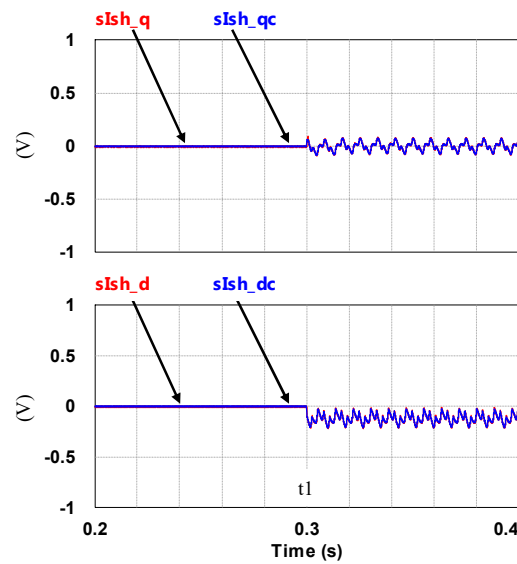


Figure 17. Shunt APF dq-axis current commands and feedbacks (t_0 – t_2).

Table 2. Root-mean-square (RMS) currents and total harmonic distortion (THD).

Power Grid Currents and Unbalance Ratio (UR)		
Item	Without APF (t_0 – t_1)	With APF (t_1 – t_2)
$i_{\text{grid_a}}$ (A)	2.9	2.84
$i_{\text{grid_b}}$ (A)	3.42	2.87
$i_{\text{grid_c}}$ (A)	3.87	2.89
UR (%)	14.91	0.94
THD		
Item	Without APF (t_0 – t_1)	With APF (t_1 – t_2)
THD ($i_{\text{grid_a}}$) (%)	19.18	3.91
THD ($i_{\text{grid_b}}$) (%)	15.56	3.94
THD ($i_{\text{grid_c}}$) (%)	13.89	3.94

5. Hardware Implementation and Test Results

To verify the performance of the proposed GaN-based APF, this section presents the implementation of APF hardware prototype for verification and analysis based on the scenario arranged in the simulation case stated in the previous section. The photograph of the constructed GaN-based APF prototype is shown in Figure 18, where the numbered devices are listed in Table 3. A programmable three-phase AC power supply is adopted to emulate the grid voltage. The Texas Instruments (TI) microcontroller, TMS320F28335 (Texas Instruments, Dallas, TX, USA), is used to provide efficiency and flexibility in controller design. The system parameters and conditions of the experimental tests and measurement scenarios are the same as that used in the previous simulation case presented in Section 4.1. Figures 19–24 show a set of test results; Figure 19 shows the waveforms of measured phase-a voltage and three-phase currents of the grid from t_0 to t_2 . Figure 20 shows the DC link voltage and the output three-phase currents of the shunt APF from t_0 to t_2 . The related waveforms of grid phase-a voltage and three-phase currents and the fast Fourier transform (FFT) of the grid phase-a current before and after the APF is activated are shown in Figures 21 and 22, respectively. As can be seen in Figure 22, after the APF is activated the unbalanced and distorted currents have been well compensated and the current is in phase with the grid voltage achieving the control objective of unity power factor. To demonstrate the performance of the designed controllers, Figure 23 shows the command and feedback signals of DC link voltage and the PI controller output signals. The dq-axis current commands and feedback signals are shown in Figure 24. To provide a set of quantitative results, Table 4 shows the measured RMS currents and calculated THD data before and after compensation. In the stage of hardware construction and tests, the system efficiencies at different switching frequencies are also explored. The arrangement of the test scenario and the detailed results are presented in the next section.

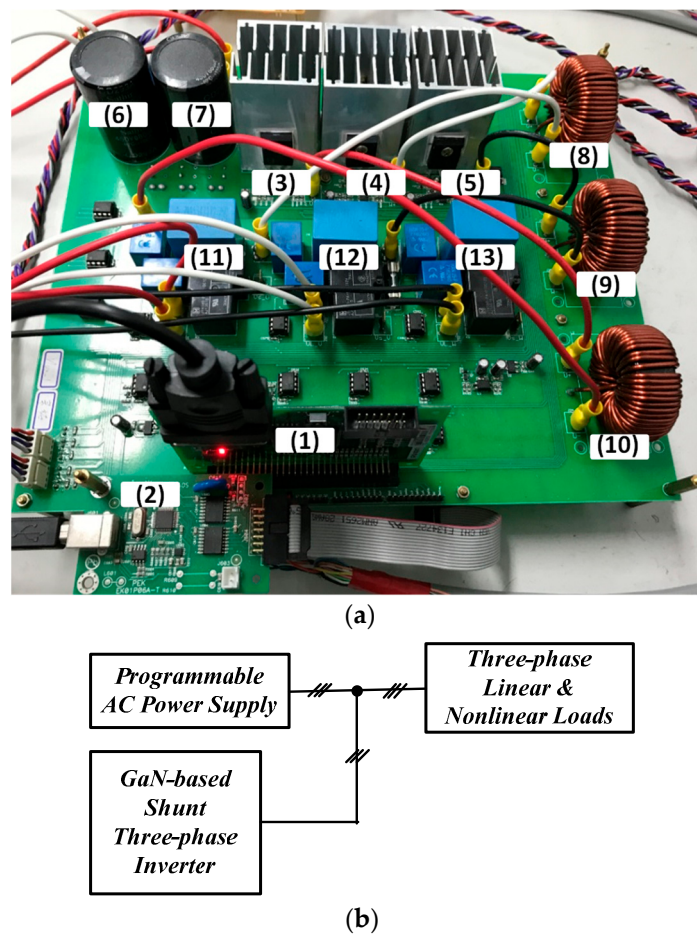


Figure 18. (a) Photo of GaN-based three-phase APF hardware; (b) schematic of the hardware test and system.

Table 3. Devices in Figure 18a.

Number	Device	Value/Part Number
(1)	Microcontroller	TMS320F28335
(2)	Interface circuit of the microcontroller	N/A
(3)–(5)	GaN HEMT pairs	TPH3207
(6) and (7)	DC link capacitors	680 mF/450 V
(8)–(10)	Filter inductors	0.5 mH
(11)–(13)	Filter capacitors	10 μ F/300 V

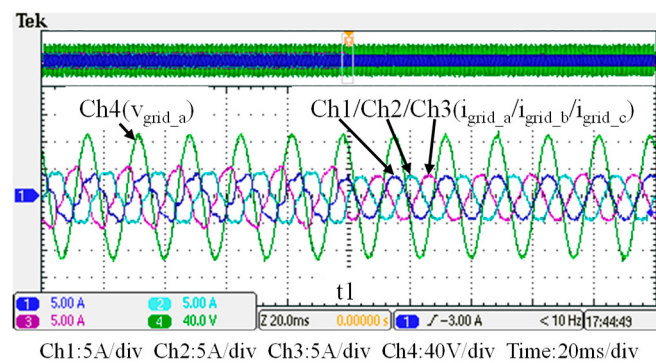


Figure 19. Grid phase-a voltage and three-phase currents (t_0 – t_2).

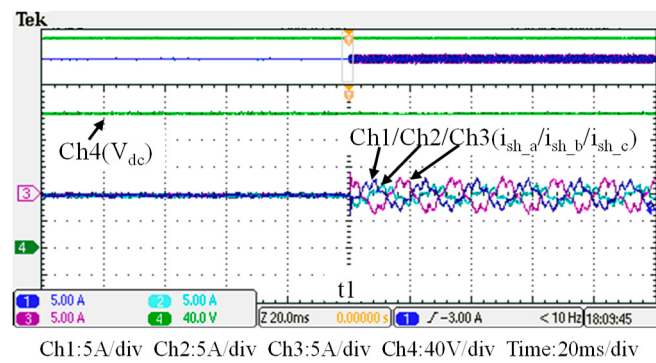


Figure 20. DC link voltage and the shunt APF three-phase currents (t_0 – t_2).

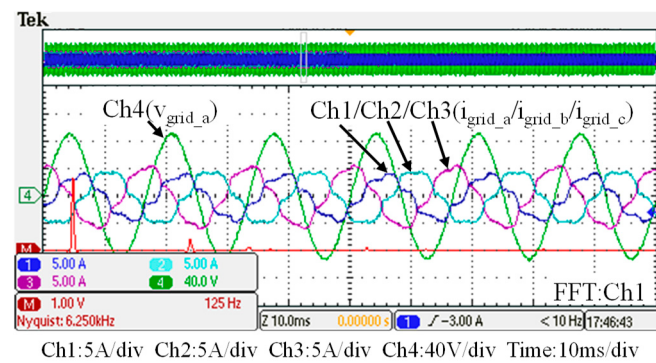


Figure 21. Before t_1 : the grid phase-a voltage and three-phase currents and the fast Fourier transform (FFT) waveform of the grid phase-a current.

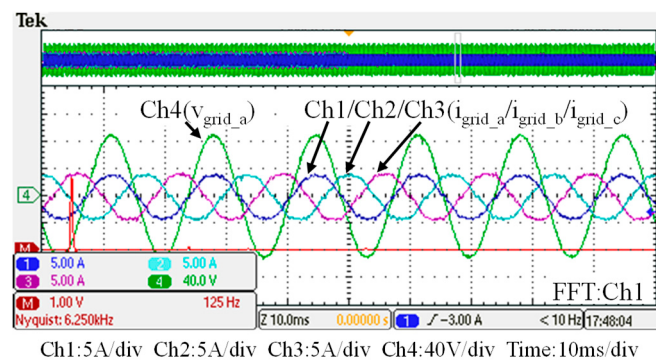


Figure 22. After t_1 : the grid phase-a voltage and three-phase currents and FFT waveform of the grid phase-a current.

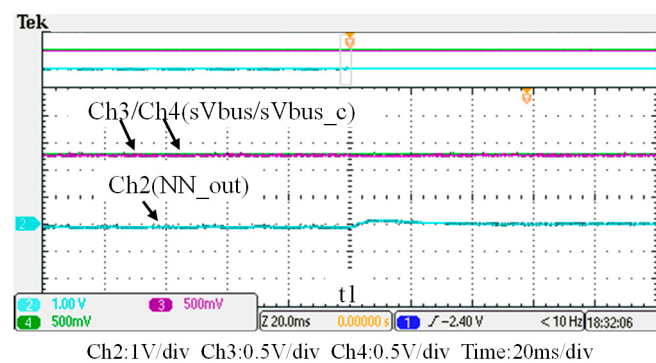


Figure 23. The command and feedback signals of DC link voltage and the proportional-integral (PI) controller output signal (t_0 – t_2).

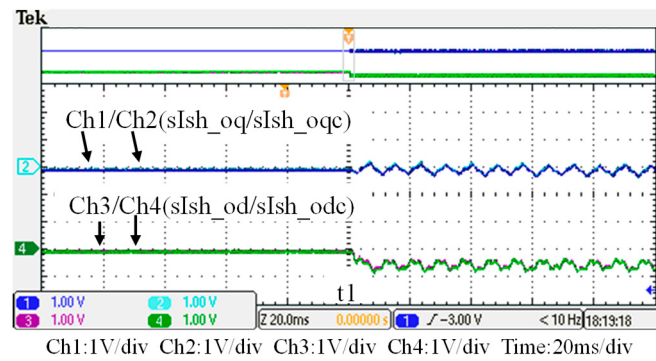


Figure 24. The shunt APF dq-axis current commands and feedbacks (t_0 – t_2).

Table 4. RMS currents and THD.

Power Grid Currents and Unbalance Ratio (UR)		
Item	Without APF (t_0 – t_1)	With APF (t_1 – t_2)
$i_{\text{grid_a}}$ (A)	2.93	2.91
$i_{\text{grid_b}}$ (A)	3.43	2.94
$i_{\text{grid_c}}$ (A)	3.95	3.02
UR (%)	14.83	2.13
THD		
Item	Without APF (t_0 – t_1)	With APF (t_1 – t_2)
THD ($i_{\text{grid_a}}$) (%)	20.23	4.15
THD ($i_{\text{grid_b}}$) (%)	16.57	4.08
THD ($i_{\text{grid_c}}$) (%)	15.48	4.05

6. Discussion

6.1. The Analysis of System Efficiency

In this paper, the system efficiencies at different switching frequencies (50 kHz, 80 kHz, and 100 kHz) and under different load levels are explored. Figure 25 shows the system block diagram of the efficiency tests. In this test, the AC terminals of the proposed three-phase GaN-based APF are connected to the three-phase power grid having the line to line voltage of 110 V and its DC terminal voltage is regulated at the designed 200 V by the proposed voltage controller of the APF. For testing the APF efficiencies under different load levels, a programmable electronic load is connected to the DC terminal of the APF. By setting different P_{dc} and measuring the corresponding P_{ac} , the efficiency at a specific power level and switching frequency can be readily calculated. In this paper, three switching frequencies, i.e., 50, 80, and 100 kHz were tested. The calculated results are graphically shown in Figure 26. As can be seen in Figure 26, the maximum efficiency appears at about 50% of the rated load and it is found that when the switching frequency increases the efficiency decreases. This is mainly due to the increase in switching losses.

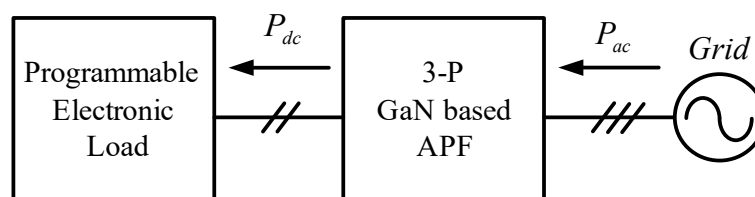


Figure 25. The system block diagram of the efficiency tests.

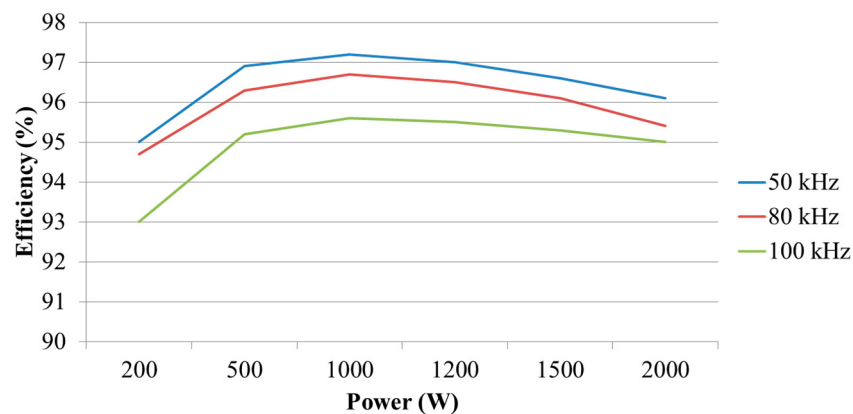


Figure 26. Efficiencies of GaN-based shunt APF system at different switching frequencies.

In the aspect of the efficiency comparison with different technologies, it is indeed difficult to establish a fair comparative basis due to some system constraints, e.g., the switching technique used, system capacities, quality of components used, and the control functions designed for the circuits. To provide a set comparative result, three recently published technical papers [16–18] using different technologies are summarized in Table 5.

Table 5. Performance comparison of different technologies.

Paper	Switching Device	Function	Power	Switching Frequency	Efficiency
[16]	IGBT	Motor drive	8 kW	20 kHz	95.5%
[17]	MOSFET	Motor drive	1.5kW	15 kHz	92%
[18]	SiC	Electric vehicle	8.8 kW	50 kHz	97%
proposed	GaN	Active power filter	2 kVA	50 kHz	97.2%
				80 kHz	96.7%
				100 kHz	95.6%

6.2. The Thermographic Analysis of the System

Figure 27 shows a set of thermographic photos (using FLIER-E63900, T198547, E4) of the proposed GaN-based three-phase APF prototype operating under the rated capacity of 2 kW with different switching frequencies. As can be seen in the photos, the temperature of the switching devices increases as the switching frequency increases and the temperature of capacitors and the circuit board remain under 25 °C. Table 6 shows the summary of the recorded temperature data gathered from the presented thermographic photos. Based on the results of thermographic analysis, it has been found that the greatest losses are located at the six power-switching devices and the three relays which are designed for ensuring a successful synchronizing control with the power grid to which the proposed APF is connected. It should be noted that in practice, these relays can be removed after the overall control system of the APF has been properly tuned. This means that the maximum efficiency of the proposed GaN-based APF can be further improved.

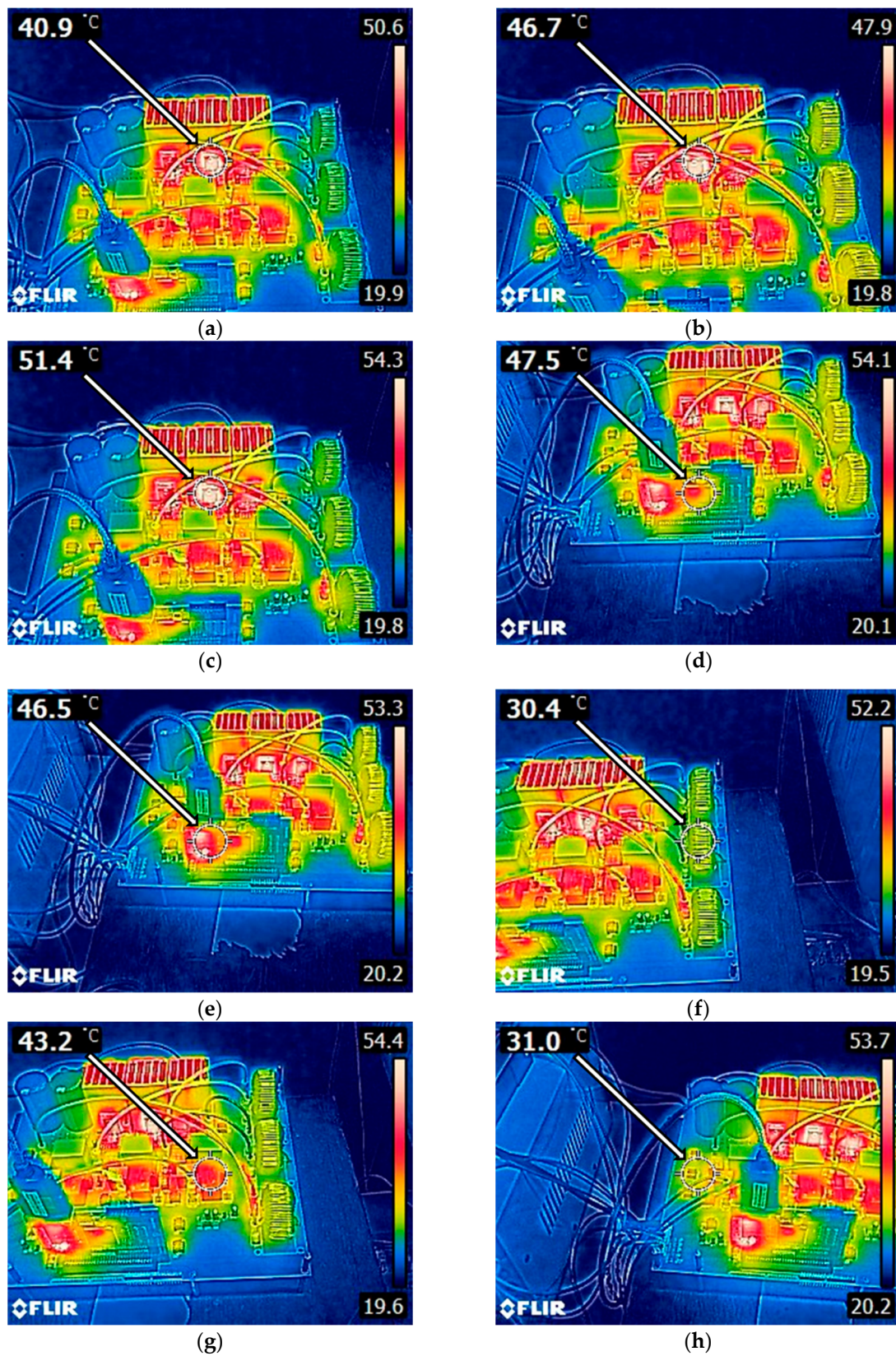


Figure 27. Thermographic photos of the proposed GaN-based three-phase APF prototype: (a) TPH3207 device switching at 50 kHz; (b) TPH3207 device switching at 80 kHz; (c) TPH3207 device switching at 100 kHz; (d) DSP; (e) communication interface; (f) inductors; (g) relay; (h) signal processing integrated circuits (ICs).

Table 6. Summary of operating temperatures of individual devices.

Sensed Object	Operating Temperature (°C)
TPH3207 @ 50kHz switching frequency	40.9
TPH3207 @ 80kHz switching frequency	46.7
TPH3207 @ 100kHz switching frequency	51.4
DSP	47.5
Communication interface	46.5
Inductors	30.4
Relays	43.2
Signal processing integrated circuits (ICs)	31.0

6.3. Related Technical Issues

As mentioned previously, the proposed GaN-based three-phase APF circuit prototype is demonstrated for the first time. There are some technical issues to be further improved. These include: (1) the driving circuits can be improved to achieve higher switching frequency and to reduce the size of inductors; (2) the three relays can be removed or replaced with new devices having better quality in conduction losses to increase the overall system efficiency; (3) the layout of the circuit can be improved to reduce the noise level in current- and voltage-sensing mechanisms. It is important to note that the noise level in sensing signals constitutes the operating limits of the switching frequency of the proposed GaN-based APF circuit.

7. Conclusions

It has been expected that the mass application of RE-based distributed generation (DG) microgrids or smart grids, and various static and dynamic nonlinear loads is the future trend of development in power systems. To ensure an acceptable PQ level, the development of advanced PQ compensation schemes using new technologies in terms of power-switching devices and state-of-the-art control algorithms is a significant task. In this aspect, this paper has demonstrated, for the first time, a shunt-type GaN HEMTs-based three-phase APF controlled by DSP systems and type II controllers to achieve simultaneous compensation for current harmonics, load imbalance, and reactive currents. Based on the results obtained from simulation and the hardware tests, the proposed 2-kVA GaN-based three-phase shunt APF prototype with digitally integrated control scheme is able to achieve satisfactory compensation results in improving system-wide load current quality of a complex load network consisting of distorted, non-linear and unbalanced loads. In this study, the TPH3207 power switching devices and Si8271 driving integrated circuits (ICs) are successfully adopted. It has been found that GaN HEMTs provide superior performance to conventional Si-based power switches in terms of switching frequency, temperature feature and system efficiency. To further evaluate the system performance of the constructed GaN-based circuit prototype, in terms of efficiency, hotspot distribution and power losses in components, a thermographic analysis has been carried out. Results and discussions for improving the proposed implementation scheme have been presented. With the proposed APF operating at 50 kHz switching frequency, the THD and UR of the three-phase grid currents can be greatly reduced. The best THD improvement recorded is from 20.23% to 4.15% and UR is from 14.83% to 2.13% and the highest system efficiency of 97.2% has been achieved. For future research works, better circuit components and GaN HEMT driving methods based on a bootstrap design can be used for achieving higher switching frequency and better system performance.

Author Contributions: The corresponding author, C.-T.M. conducted the research work, proposed the design methods, designed the simulation and hardware test scenarios, verified the technical contents and polished the final manuscript. Z.-H.G., a postgraduate student in the department of electrical engineering, national united university, performed the paper search, managed figures and checked the related data. All authors have read and agreed to the published version of the manuscript.

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