Supplementary Material

Structural and Electronic Properties of Polycrystalline InAs Thin Films Deposited on Silicon Dioxide and Glass at Temperatures below 500°C

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Table S1 shows room temperature Hall-effect measurement results for Zn-doped InAs(P) films ranging in thickness from 10 to 100nm. The three samples are grown on an Si/SiO_2 substrate, with a poly GaAs seed layer (nominal thickness of 25nm) deposited before growth. Mobility and sheet carrier concentration both increase with increasing thickness. The increase in sheet carrier concentration is evidence that these films do not have only a surface charge as was expected from the literature.

Table S1: Room temperature Hall effect measurement results for different thicknesses of Zn-doped InAs(P) grown on Si/SiO_2 with 25nm poly GaAs seed layer

Sample Thickness	**Carrier type**	**Carrier mobility ($cm^2/V{\cdot}s$)**	**Carrier concentration (cm^{-3})**	**Sheet carrier concentration (cm^{-2})**
10nm	electrons	24.6	$2.5x10^{16}$	$2.5x10^{10}$
25nm	electrons	61.6	$5.22x10^{16}$	$1.3x10^{11}$
100nm	electrons	103.4	$4.5x10^{16}$	$4.5x10^{11}$

Figure S1 shows further information relating to Figure 2 in the main paper. This includes the layout of the cTLM structures which were measured, an example of the measured IVs from which the results were extracted, and resistivity of 25nm poly InAs film. Taking the Hall results for 25nm poly InAs in Table 1 in main paper, mobility is $73cm^2/V{\cdot}s$ and carrier concentration is $7x10^{18}cm^{-3}$. Resistivity of the film should be equal to:

$$Resistivity = \frac{1}{\sigma} = \frac{1}{q \times \mu \times n} = \frac{1}{q \times 73 \times (7 \times 10^{18})} \qquad 1$$

Here σ represents the conductivity of the semiconductor. This comes out to be $0.01\Omega{\cdot}cm$, which is in good agreement with the results shown in Figure S1(c) of ~9-10m$\Omega{\cdot}$cm. These results are from a large area (Hall) and small area (cTLM) technique, so this agreement is good verification of results.

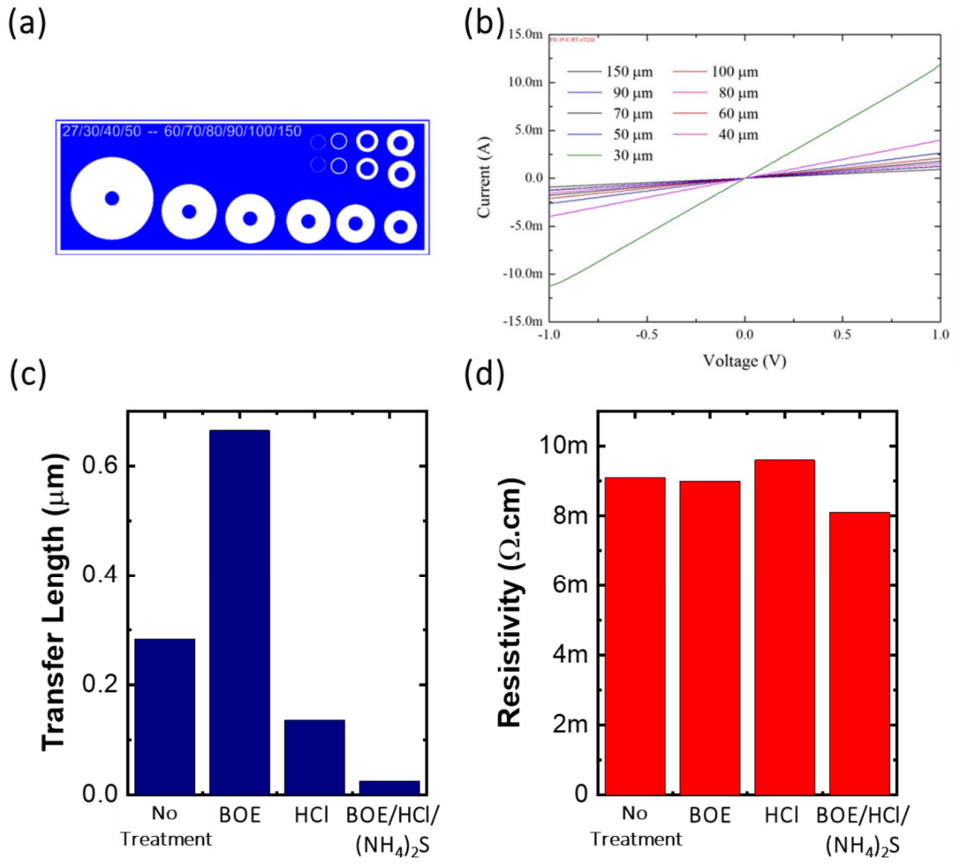

FIG S1: (a) cTLM structure layout from which measurements were taken for Figure 2 in the main paper. **(b)** Linear IVs from which the parameters in Figure 2 in main paper were extracted. **(c)** Transfer length, and **(d)** resistivity results for 25nm poly InAs film which received each of the surface treatments, and reference sample which received no surface treatment.

Figure S2 shows the clockwise hysteresis observed for sample shown in Figure 4 in the main paper, consistent with electron trapping and de-trapping in the Al_2O_3 gate oxide. Similar clockwise hysteresis observed for samples of different thicknesses, and for samples with or without poly GaAs seed layer as shown in figure S3 below. Field effect mobility and carrier concentration are extracted from transfer characteristics as shown in Figure 3(e & f) in the main paper. Field effect mobility is calculated using the transconductance from:

$$g_m = \frac{W}{L} \times \mu \times C_{ox} \times V_{DS} \qquad 2$$

Then resistance, $\frac{V_{DS}}{I_{DS}}$, is extracted as a function of V_{GS}. From resistance and channel dimensions, resistivity and hence conductivity is calculated. Using the formula for conductivity:

$$Conductivity = n \times q \times \mu, \qquad 3$$

the carrier concentration (n) can be calculated. As the parameters from which it is extracted are functions of V_{GS}, carrier concentration is also V_{GS} dependent.

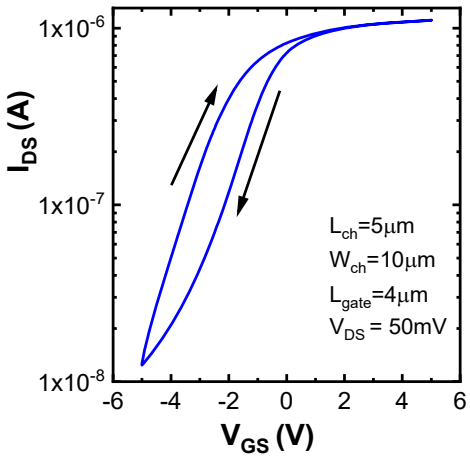

FIG S2: Clockwise hysteresis observed for transfer characteristics of 10nm Zn-doped poly InAs(P) with 25nm poly GaAs seed layer grown on a glass substrate with junctionless transistor device structure.

Figure S3 demonstrates that different substrates and absence or presence of poly GaAs layer did not significantly change the electrical properties of the films when implemented in a transistor test structure. Figures S3(a & b) indicate that the poly GaAs seed layer is not the source of the relatively high off-currents exhibited by the structures.

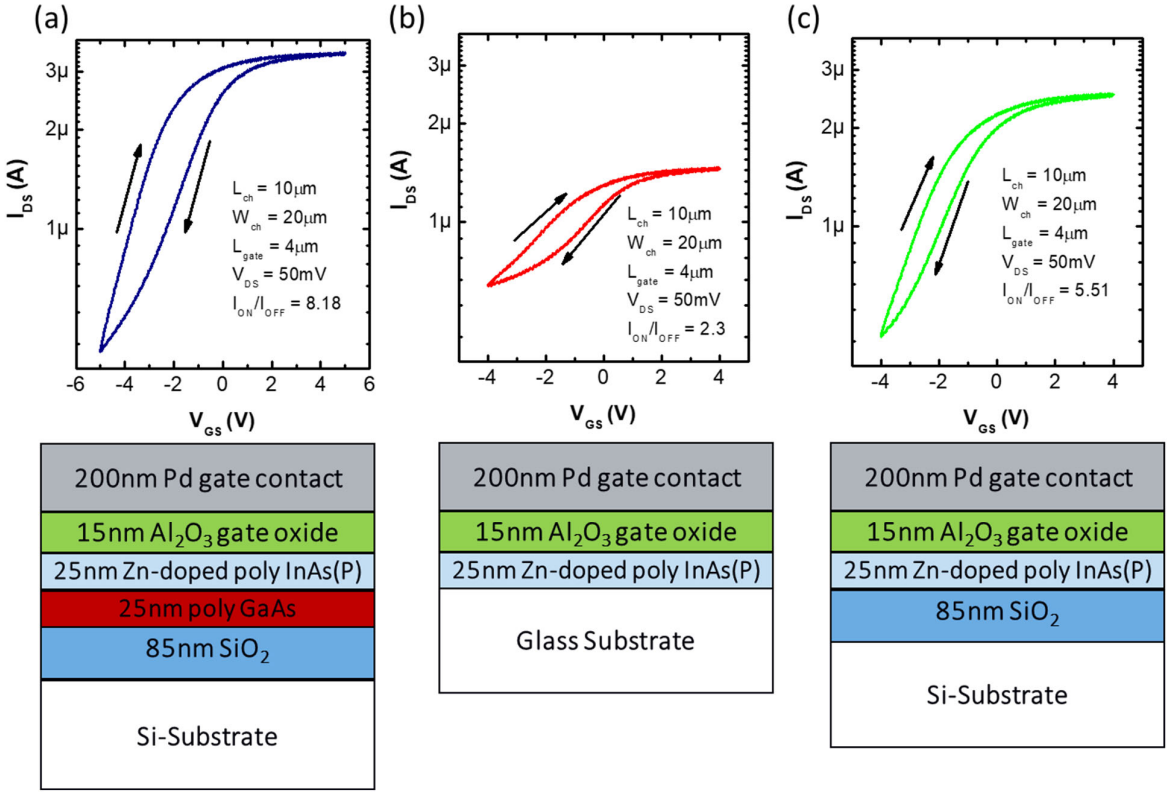

FIG S3: Transfer characteristics of **(a)** 25nm Zn-doped InAs(P) with 25nm poly GaAs seed layer grown on Si/SiO_2 substrate **(b)** 25nm Zn-doped InAs(P) grown directly on glass substrate, and **(c)** 25nm Zn-doped InAs(P) grown directly on Si/SiO_2 substrate. Structures through channel region shown below each corresponding IV.

Figure S4 shows time of flight secondary ion mass spectrometry (TOF-SIMS) results for sample shown in Figure 4(a) of the main paper. These results confirm the presence of a low level of Ga in the poly InAs layer. The resulting widening of the energy gap (due to the larger bandgap of GaAs (1.4eV) compared to InAs(0.36eV)), is a possible explanation for the lower I_{OFF} achieved for this sample in comparison to the sample without a poly GaAs layer (Figure 4(b) in the main paper).

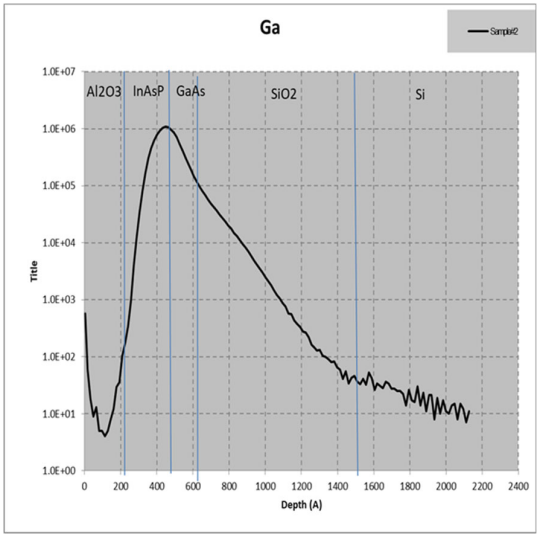

FIG S4: TOF-SIMS results showing level of Ga present vs depth from surface, for sample consisting of nominally 25nm poly GaAs buffer layer + 25nm Zn-doped poly InAs(P).