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MOCVD-grown β-Ga_2O_3 as a Gate Dielectric on AlGaN/GaN-Based Heterojunction Field Effect Transistor

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Abstract: We report the electrical properties of $Al_{0.3}Ga_{0.7}N$/GaN heterojunction field effect transistor (HFET) structures with a Ga_2O_3 passivation layer grown by metal–organic chemical vapor deposition (MOCVD). In this study, three different thicknesses of β-Ga_2O_3 dielectric layers were grown on $Al_{0.3}Ga_{0.7}N$/GaN structures leading to metal-oxide-semiconductor-HFET or MOSHFET structures. X-ray diffraction (XRD) showed the $(\bar{2}01)$ orientation peaks of β-Ga_2O_3 in the device structure. The van der Pauw and Hall measurements yield the electron density of ~ 4×10^{18} cm^{-3} and mobility of ~770 $cm^2V^{-1}s^{-1}$ in the 2-dimensional electron gas (2DEG) channel at room temperature. Capacitance–voltage (*C-V*) measurement for the on-state 2DEG density for the MOSHFET structure was found to be of the order of ~1.5×10^{13} cm^{-2}. The thickness of the Ga_2O_3 layer was inversely related to the threshold voltage and the on-state capacitance. The interface charge density between the oxide and $Al_{0.3}Ga_{0.7}N$ barrier layer was found to be of the order of ~10^{12} cm^2eV^{-1}. A significant reduction in leakage current from ~10^{-4} A/cm^2 for HFET to ~10^{-6} A/cm^2 for MOSHFET was observed well beyond pinch-off in the off-stage at -20 V applied gate voltage. The annealing at 900 °C of the MOSHFET structures revealed that the Ga_2O_3 layer was thermally stable at high temperatures resulting in insignificant threshold voltage shifts for annealed samples with respect to as-deposited (unannealed) structures. Our results show that the MOCVD-gown Ga_2O_3 dielectric layers can be a strong candidate for stable high-power devices.

Keywords: GaN; MOSHFET; Ga_2O_3; MOCVD; gate dielectric

Citation: Hasan, S.; Jewel, M.U.; Crittenden, S.R.; Lee, D.; Avrutin, V.; Özgür, Ü.; Morkoç, H.; Ahmad, I. MOCVD-grown β-Ga_2O_3 as a Gate Dielectric on AlGaN/GaN-Based Heterojunction Field Effect Transistor. *Crystals* **2023**, *13*, 231. https://doi.org/10.3390/cryst13020231

Academic Editors: Peng Chen and Zhizhong Chen

Received: 6 January 2023
Revised: 21 January 2023
Accepted: 23 January 2023
Published: 28 January 2023

1. Introduction

GaN-based heterojunction field effect transistors (HFETs) have excellent properties such as high critical breakdown field, high current, and superior thermal/chemical stability, which are coveted for high power, both RF and high-frequency switching applications under harsh environments [1–4]. The high-frequency performance of HFETs is limited by a series of effects associated with charge leakage, trapping/de-trapping, and conduction characteristics at different locations of the devices [5]. One of the most significant performance-limiting phenomena is the injection of electrons from the gate electrode to the surface region of the semiconductor on the drain side of the gate electrode, which results in reliability issues as well as limitations on the input drive in power applications [6,7]. For high drain and gate bias, the magnitude of the electric field under the gate region can cause tunneling/leakage of electrons from the gate metal to the semiconductor. Thus, the tunneling/gate leakage effect becomes critical for radio frequency (RF) applications because the electric field oscillates with the total terminal (dc+RF) voltage [8]. During the high voltage portion of the RF cycle, a pulse of electrons will tunnel from the gate by acquiring sufficient energy and can cause gate breakdown [9,10]. The electron transport

on the surface is sluggish due to high effective mass, and dispersion is introduced due to the charging/discharging time constant [11]. The electrons escaping from the gate metal gather on the surface, creating a "virtual gate" effect that functions as an effective increase in gate length on the drain side can result in leakage current [7]. As a result, the conducting channel depletes of free electrons, and the device dc current and RF power decreases [7]. To overcome this problem, a dielectric material, often an oxide layer, is introduced between the metal gate and the semiconductor, creating metal-oxide-semiconductor-HFET (MOSHET) for high-frequency applications. Thus, the gate tunneling is reduced or eliminated with improved surface charge modulation by an insulating oxide layer under the gate [7,12].

The incorporation of the oxide layer improves the GaN-based HFET performance by minimizing the gate leakage current, maximizing the output power (as the input can be driven harder), improving the breakdown voltage, etc [13]. The interface between the semiconductor and oxide layer, however, plays an important role in transistor performance [14]. Chemically and thermally stable oxides with low density of interface states between the insulator (oxide) and semiconductor are required [15]. Several groups have reported the use of different dielectrics, such as aluminum oxide (Al_2O_3) [16], hafnium dioxide (HfO_2) [17], zirconium dioxide (ZrO_2) [18], silicon dioxide (SiO_2) [19], silicon nitride (Si_3N_4), and hexagonal boron nitride (h-BN) [20], fabricated by several deposition methods, including atomic layer deposition (ALD) [14], pulsed laser deposition (PLD) [21], and plasma enhanced chemical vapor deposition (PECVD) [21]. SiO_2/hBN has also been reported to be used as a substrate material for field effect transistors [22].

Ga_2O_3 is a promising material with potential dielectric applications for high-power devices because of its wide bandgap (4.4–5.3 eV) and high breakdown voltage (8 $MVcm^{-1}$) [23,24]. It has a moderate dielectric constant (k = 10.6), which is higher than those of traditional dielectrics such as SiO_2 (k = 3.9), and Si_3N_4 (k = 7.4) [16]. This dielectric-constant value allows gate scaling and a smaller voltage for the same charge. The feasibility of using Ga_2O_3 as a gate dielectric was demonstrated by employing ALD with compounds such as trimethylgallium, and triethylgallium as a Ga precursor and ozone or oxygen (O_2) plasma as an oxygen precursor [23,25,26]. The Ga_2O_3 layers grown by ALD for MOSHFETs are amorphous and prone to change their properties, especially threshold voltage, with annealing due to crystallization [27]. The use of crystalline metal–organic chemical vapor deposition (MOCVD) grown β-Ga_2O_3 as a gate dielectric has so far not been reported. A comprehensive study of the electrical properties is necessary to determine the feasibility of MOCVD Ga_2O_3 as a gate dielectric.

In this work, we study the electrical properties of $Al_{0.3}Ga_{0.7}N$/GaN HFET with MOCVD-grown β-Ga_2O_3 as a passivation/dielectric layer. β-Ga_2O_3 layers of three different thicknesses of 10 nm, 20 nm, and 30 nm were grown on top of $Al_{0.3}Ga_{0.7}N$/GaN creating MOSHFET structures. Furthermore, the variations in electrical properties, particularly the shift in threshold voltage, are studied for annealed and as-deposited MOSHFET structures with MOCVD-grown β-Ga_2O_3.

2. Experimental Methods

The epilayers used for devices studied in this paper were deposited in a vertical cold wall metal–organic chemical vapor deposition (MOCVD) system using nitrogen (N_2) as a carrier gas on a 2-inch diameter c-axis sapphire substrate with 0.2° offcut. Trimethylaluminum (TMAl), triethylgallium (TEG), ammonia (NH_3), and ultra-high purity oxygen were used as aluminum (Al), gallium (Ga), N_2, and oxygen (O_2) precursors, respectively. First, a thin 150 nm aluminum nitride (AlN) buffer layer was grown on the sapphire substrate using the process described in [28,29]. Then, on top of the AlN layer, a 500 nm thick gallium nitride (GaN) channel layer with a V/III ratio of 8000 at a temperature of 960 °C, a 2 nm AlN spacer, and a 25 nm thick barrier aluminum gallium nitride ($Al_{0.3}Ga_{0.7}N$) layers with V/III ratio of 5000 at a temperature of 1020 °C were grown at 100 Torr chamber pressure, creating heterojunction field effect transistor (HFET) structure [30–32]. The van der Pauw and Hall effect measurements show that the GaN layers used for our device structures

were highly resistive. Figure 1 shows the schematic of the FET epilayer structures used in this paper where, Figure 1a exhibits the schematic of the HFET structure. For this study, the β-Ga_2O_3 layers were grown on top of the HFET structure using the MOCVD process at 700 °C, 50 Torr chamber pressure, and a VI/III ratio of ~900. The details of the Ga_2O_3 growth can be found elsewhere [33]. This creates a MOSHFET structure with the dielectric layer thickness varying from 10 nm to 30 nm, as shown in Figure 1b. The MOSHFET structure with 30 nm oxide thickness was annealed to gauge its electrical and thermal stability. Annealing was performed at 900 °C for 30 min in a 50/50 O_2/N_2 (nitrogen was used as carrier gas) environment to avoid desorption from the Ga_2O_3 layer.

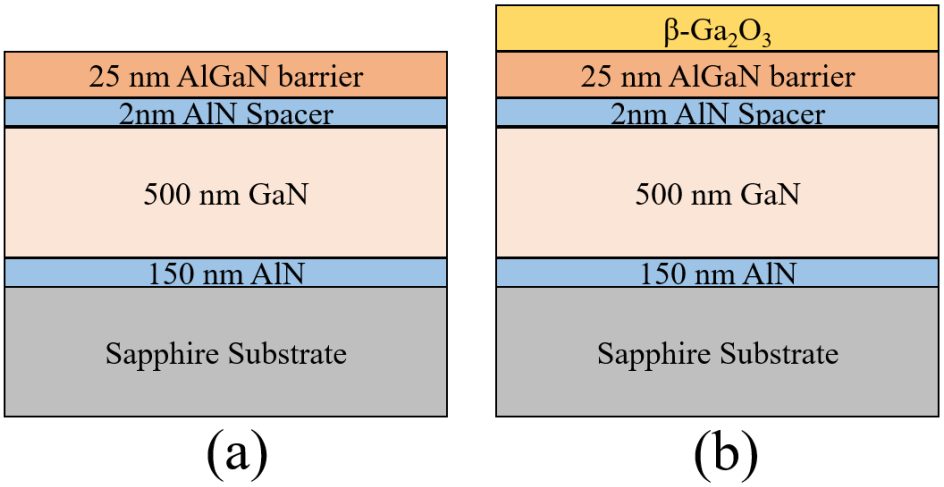

Figure 1. The epilayer structure of the (**a**) $Al_{0.3}Ga_{0.7}N/GaN$ HFET, (**b**) Ga_2O_3 MOSHFET.

We characterized the structural quality and electrical properties of all the device structures obtained in this work. A Rigaku Miniflex II Desktop X-ray diffractometer with Cu-K*α1* x-ray source (λ = 1.5406 Å) operated at 30 mA current and 15 kV voltage was used to evaluate the structural properties of the epilayers. The capacitance–voltage *(C-V)* measurements were performed using a mercury probe controller model 802B connected with a HP 4284A Precision LCR Meter capable of measuring the impedance as a function of frequency. Gate leakage current was measured in the same mercury probe set up with Keysight B2910 Precision Source/Measure Units (SMU). The gate diameter of the mercury probe was 797 µm with 0.1 pF stray capacitance. The van der Pauw/Hall effect measurements were performed on the samples using the MMR Technologies Inc. H-50 controller and MPS-50 programmable power supply with indium contacts.

3. Results and Discussions

Figure 2 shows the X-ray diffraction (XRD) 2θ scan of the MOSHFET structure (before and after annealing). The peaks at 18.8° and 38.2° are related to the $(\bar{2}01)$ and $(\bar{4}02)$ Ga_2O_3 of the β phase [34]. The peak at 34.5° and the adjacent higher angle shoulder are consistent with the (002) and (002) reflection from the GaN channel and AlGaN barrier layers, respectively [35]. Note that the GaN channel layer was grown on 0.15 µm AlN. The peak at 36.1° is due to the (002) AlN reflection. The peaks at 20.4° and 41.6° correspond to the (003) and (006) sapphire reflections [34]. The most common method of oxide dielectric deposition is ALD, which is mostly used for depositing amorphous materials [36]. The problem with amorphous layers is that, during the rapid thermal annealing (RTA) step required to form ohmic contacts to MOSHFETs, there occurs a phase transformation from amorphous to crystalline structure [27]. This transformation results in the formation of a microcrystalline structure with multiple grain boundaries, which creates leakage paths, rendering it unsuitable for device applications [27]. The process used for the MOCVD oxide deposition favors the growth of single-crystal β-Ga_2O_3 dielectric layers, as confirmed by the XRD data. Therefore, it is expected that, as Ga_2O_3 is already in the crystalline

form, the thermal treatment will have a minimal impact on its electrical properties, as we demonstrate by the annealing experiments in the later description.

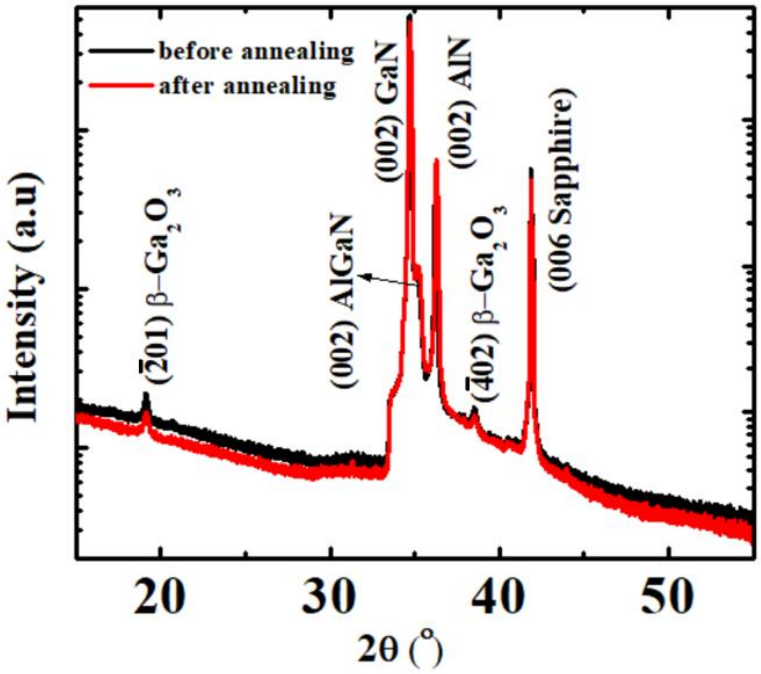

Figure 2. XRD 2θ scan of the MOSHFET structure (before and after annealing) confirming the presence of the peaks consistent with crystalline Ga_2O_3 (β phase), GaN, AlGaN, AlN, and sapphire substrate.

The origin of the highly conductive quantum confined two-dimensional electron gas (2DEG) at the AlGaN/GaN interface is due to the lack of inversion symmetry along the [0001] axis of GaN coupled with AlN being relatively more electronegative [2]. The difference between spontaneous and piezoelectric polarization and band offset at the interface introduces a fixed polarization-induced sheet of carrier charges, indicated by the shift of Fermi level in the conduction band. Schrödinger and Poisson's equation-based charge distribution and band diagram can be calculated using different available tools [37]. However, a simpler approach using the Langer and Heinrich rule helps to estimate different parameters and understand the band structure at the heterojunction interfaces [38,39]. Figure 3 shows the schematical band diagram for the Ga_2O_3 MOSHFET. The bandgaps for GaN, $Al_{0.3}Ga_{0.7}N$, and Ga_2O_3 are 3.4 eV, 4.03 eV (using Vegard's law), and 4.9 eV (β phase), respectively [40]. The position of the Fermi level in GaN near the channel-barrier interface is in the conduction band; where n_s is the sheet carrier density, C_b is the $Al_{0.3}Ga_{0.7}N$ barrier layer capacitance, C_{ox} is the Ga_2O_3 layer capacitance. We can express the total gate capacitance (C_G) using the series capacitance formula as below:

$$\frac{1}{C_G} = \frac{1}{C_b} + \frac{1}{C_{ox}} \quad (1)$$

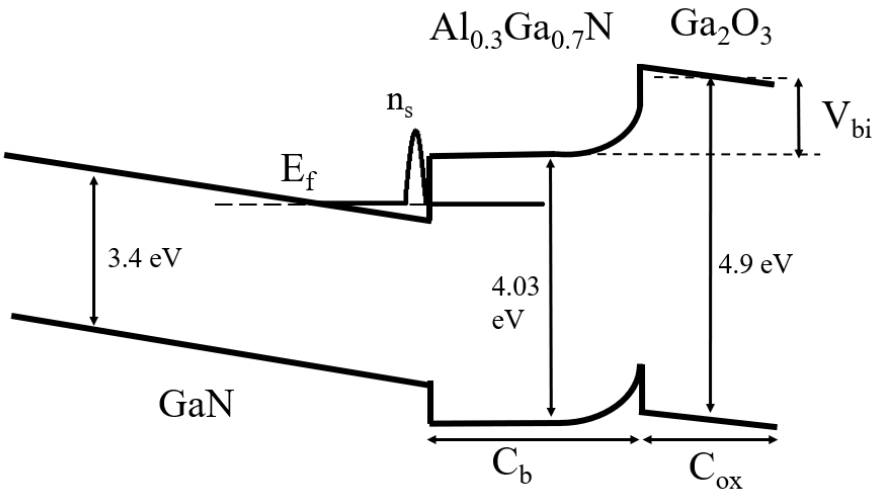

Figure 3. The representative band diagram of GaN/AlGaN MOSHFET with Ga_2O_3 as a gate dielectric.

The capacitance–voltage (*C*-*V*) measurements of the MOSHFET structure were performed using a mercury probe gate contact to extract pertinent electrical parameters of the device structures, such as threshold voltage (V_{th}), zero gate voltage capacitance, and 2DEG electron density. The total gate capacitance is given by Equation (1), i.e., the addition of the oxide dielectric layer capacitance in series with the barrier layer capacitance. The benefit of an oxide dielectric is to increase the gate breakdown voltage and/or reduce the gate leakage current by suppressing the surface states, sometimes superseded by the impact of different device electrical parameters such as threshold voltage and gate leakage current. The threshold voltage of the MOSHFET structure is given by the Equation [41]:

$$V_{th,MOSHFET} = V_{th,HFET}\left(1 + \frac{d_i \varepsilon_{s,b}}{\varepsilon_i d_{s,b}}\right) \quad (2)$$

where $V_{th,MOSHFET}$ and $V_{th,HFET}$ are the threshold voltage of the MOSHFET and HFET (that without the oxide layer- otherwise identical), respectively. d_i, $d_{s,b}$, ε_i and $\varepsilon_{s,b}$ are the thicknesses and dielectric constants of the insulator/oxide (indexed by i) and semiconductor barrier (indexed by s,b) layers, respectively. From equation (2), it is clear that if d_i increases, $V_{th,MOSHFET}$ increases, whereas $V_{th,MOSHFET}$ decreases with the increase in ε_i. Thus, a higher dielectric constant and lower dielectric thickness are desirable for minimum threshold voltage shifts.

Figure 4 shows the capacitance voltage characteteristics, threshold voltage and zero capacitance dispersion of our samples. Figure 4a shows the *C*-*V* data for HFET and MOSHFET structures with oxide thicknesses of 10 nm, 20 nm, and 30 nm. The addition of oxide on the HFET barrier adds capacitance in series with the existing barrier layer capacitance, which would lower the overall gate capacitance. The relative dielectric constants for the AlGaN barrier layer (9.2) and that for the Ga_2O_3 (10.6) are very close [42], and the AlGaN barrier layers is undoped. Due to these reasons, we did not observe any change in the *C*-*V* curve shape near the zero-gate voltage position when increasing the negative gate voltage before depleting the channel. From equation (2), we observe that as the thickness of the oxide layer increases, the V_{th} should increase. The *C*-*V* measurements on the MOSHFET structure with MOCVD-grown Ga_2O_3 gate dielectric confirm the increase in the V_{th} value. As the thickness of the Ga_2O_3 layer increased, the V_{th} exhibited a negative shift. Thus, with the increase in dielectric layer thickness, a higher voltage is required to deplete the 2DEG. During the *C*-*V* measurement, when 2DEG starts to deplete, the capacitance decreases drastically, ultimately leading to pinching off of the channel. By further increasing the gate voltage beyond pinch-off, the depletion layer extends to the GaN channel. Figure 4b summarizes the above discussion.

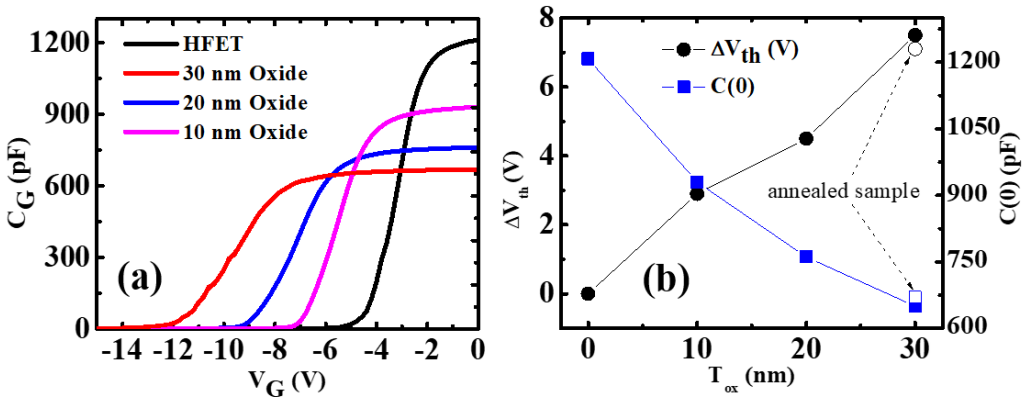

Figure 4. *C-V* characteristics at 1MHz frequency of (a) HFET and Ga_2O_3-based MOSHFETs with different oxide thicknesses, (b) Threshold voltage and zero gate-voltage capacitance dispersion for HFET and Ga_2O_3 MOSHFETs.

Figure 5 compares the *C-V* data for annealed and as-deposited MOSHFETs with a 30 nm thick β-Ga_2O_3 as a gate oxide layer. The 30-min annealing at 900 °C was performed in the MOCVD reactor, used for the Ga_2O_3 growth, as described in the experimental method section. As shown in Figure 2, the pre and post-annealed XRD was similar. As can be concluded from the *C-V* data, the annealing experiment did not result in any discernable change in the V_{th} and zero capacitance values, demonstrating the excellent thermal stability of the crystalline β-Ga_2O_3. The change in threshold voltage (open circle) and capacitance (open square) for the annealed MOSHFET structure are also shown in Figure 4b.

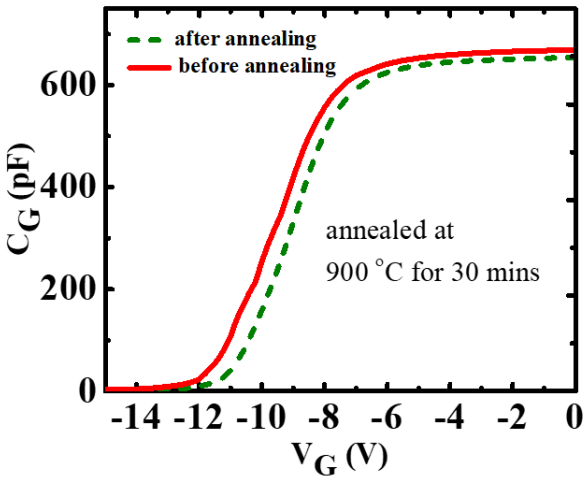

Figure 5. *C-V* data of at 1MHz frequency Ga_2O_3-based MOSHFET with 30 nm oxide thickness annealed (dashed line) and unannealed (continuous line).

The carrier density N_d was calculated using the Hall effect data and found to be on the order of 10^{18} cm^{-3}, the exact values of the carrier density can be found in Table 1. The built-in voltage V_{bi} (as shown in the band diagram: Figure 2) can be measured from $1/C^2$ intercept with the x-axis and expressed by equation (3) [43]:

$$V_{bi} = \frac{qN_d x_d^2}{2\epsilon_s} + \frac{qN_d x_d}{\epsilon_{ox}} t_{ox} + \frac{Q_{ox}}{\epsilon_{ox}} t_{ox} \quad (3)$$

Table 1. The summary of the key electrical parameters measured/calculated from *C-V* and Hall measurements.

	V_{th} (V)	μ (cm^2V^- s^{-1}) (Hall)	R_{sh} (Ωcm^{-2}) (Hall)	N_d (cm^{-3}) (Hall)	n_s (cm^{-2}) (C-V)	n_s (cm^{-2}) (Hall)	Q_{ox} (Ccm^{-2}) (C-V)	D_{it} ($cm^{-2}eV^{-1}$) (C-V)	Leakage Current at −20 V (A/cm^{-2})
HFET	–5	750	537	6.8×10^{18}	1.25×10^{13}	1.55×10^{13}	None	None	1.66×10^{-4}
10 nm	–7.9	772	630	5.0×10^{18}	1.28×10^{13}	1.4×10^{13}	-6.68×10^{12}	7.47×10^{12}	1.3×10^{-6}
20 nm	–9.5	770	650	4.2×10^{18}	1.24×10^{13}	1.42×10^{13}	-1.64×10^{13}	7.57×10^{12}	1.12×10^{-6}
30 nm	–12.5	776	685	4.4×10^{18}	1.4×10^{13}	1.4×10^{13}	-2×10^{13}	4.98×10^{12}	9.54×10^{-7}
annealed	–12.1	760	680	4.5×10^{18}	1.4×10^{13}	1.4×10^{13}	-3.06×10^{12}	3×10^{12}	8.33×10^{-7}

Here, t_{ox} and ϵ_{ox} are the thickness and permittivity of the oxide layer, N_d is the carrier concentration, x_d and ϵ_s are the depletion width and permittivity of the AlGaN barrier layer. If we set $t_{ox} = 0$, then the 2nd and 3rd term of Equation (3) becomes zero, and the equation represents the built-in voltage for conventional HFET structure. Using Equation (1) and the parallel plate capacitance formula for each series capacitor component, we can calculate the value of x_d at zero gate voltage. Inserting the determined value of x_d, and previously calculated/measured N_d, t_{ox}, and known ϵ_{ox}, ϵ_s into Equation (3), we can obtain the oxide charge Q_{ox}. The calculated values of Q_{ox} for all the samples is shown in Table 1. We observe a trend in the value of Q_{ox}; as the oxide thickness increases, the value of Q_{ox}, become more negative which increases V_{th} shift supporting Equation (2). There may be impact of stress on the charge, but we did not isolate that in our calculation. Due to low thickness, we did not observe any signature peak of the dielectric Ga_2O_3 or barrier AlGaN layer in Raman measurement (Figure S2 in Supplementary Section).

Figure 6 shows the 2DEG carrier density (n_s) versus the gate voltage (V_G) for 10, 20, and 30 nm gate oxide thicknesses calculated using the following equation:

$$qn_s = (V_G - V_{th})C_G \quad (4)$$

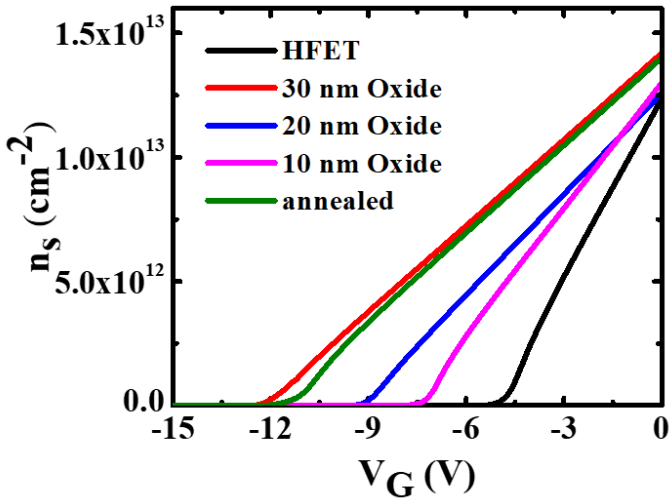

Figure 6. 2DEG carrier density in FETs vs. applied gate voltage for different gate oxide thicknesses.

In all three cases, the zero-gate voltage value of sheet carrier density is very close in the range of (1.25–1.5) $\times 10^{13}$ cm^{-2}, a slightly higher value of n_s could be due to sample-to-sample variations. The sheet carrier concentrations measured using van der Pauw/Hall effect method are also in the range of (1–1.5) $\times 10^{13}$ cm^{-2}, which validates our calculations using the value from the *C-V* measurement by employing equation (4). The sheet carrier

concentration does not change with oxide layer thickness or annealing of the oxide layer. In previous studies for the ALD-grown amorphous oxide dielectrics-based MOSHFETs, it has been demonstrated that the annealing of the oxide layers drastically shifts V_{th}. As we can see in Figure 5, annealing of the crystalline Ga_2O_3-based MOSHFET, there is no noticeable change in the threshold voltage in contrast to the case for previously reported ALD-grown oxides [44]. To further validate the MOCVD oxide material property we can use Equation (1), to calculate the experimental dielectric constant for β-Ga_2O_3. The values of the gate capacitance, C_G, before and after annealing are 1.64×10^{-7} F/cm^{-2} and 1.67×10^{-7} F/cm^{-2} (for 1 MHz frequency measurement). C_b is the barrier capacitance of the MOSHFET, and the value is 3.3×10^{-7} F/cm^{-2}. Based on $C_{ox} = \frac{\varepsilon_r \varepsilon_0}{t_{ox}}$, we get $\varepsilon_r = 10.9$ (using $C_G = 1.67 \times 10^{-7}$ F/cm^{-2}), whereas the reference value is 10.6. Thus, it can be inferred that the MOCVD-grown oxide has a dielectric property that is very close to the previously reported literature value [42].

The interface trapped charge or interface traps stem(s) from dangling bonds at the semiconductor–insulator interface. The frequency-dependent High–Low method is commonly used to determine interface charge density (D_{it}). Figure 7 shows the frequency-dependent CV measurement used to calculate the interface charge densities for MOSHFET with 10 nm oxide thickness (the frequency-dependent *C*-*V* measurements of MOSHFET with 20 nm, 30 nm oxide thickness along with the annealed sample are shown in the Supplementary Section Figure S1).

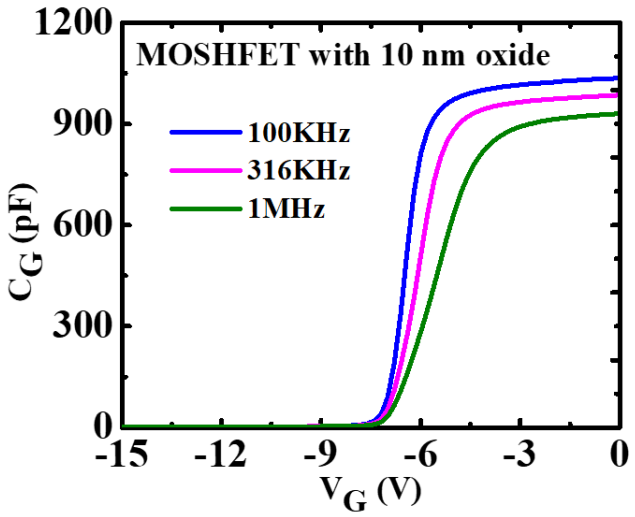

Figure 7. Frequency-dependent C-V characteristic of a MOSHFET with 10 nm thick gate oxide at frequencies of 100 kHz, 316 kHz, and 1 MHz.

The High–Low frequency *CV* method compares a low-frequency *C*-*V* curve with one that is free of interface traps. The latter is usually referred to as a high-frequency *C*-*V* measurement, where interface traps with relatively long-time constants cannot respond, leading to decreased measured capacitance. At low frequencies, the interface traps can respond, if not deep, thus resulting in higher capacitance; 100 kHz and 1 MHz frequencies are the typical values can be used for CV-based calculations of the density of interface states (D_{it}) of Nitride systems [45]. Consequently, from the difference between high- and low-frequency CV measurements, the D_{it} can be obtained based on Equation (5) at a specific applied gate voltage [46]:

$$D_{it}(V_G) = \frac{C_{ox}}{q}\left(\frac{C_{LF}}{C_{ox} - C_{LF}} - \frac{C_{HF}}{C_{ox} - C_{HF}}\right) \quad (5)$$

where C_{ox} is the capacitance of the oxide dielectric layer calculated using the parallel plate capacitor formula, q is the unit elementary charge, C_{LF} is the MOSHFET low-frequency

capacitance value and C_{HF} is the MOSHFET high-frequency capacitance value. The total trap densities for all the samples are tabulated in Table 1. For all samples, the calculated interface trap densities are in the range (3–7.57) $\times$ 10^{12} $cm^{-2}eV^{-1}$; these values are close to the typically calculated values of MOSHFETs (typical values are in the order of ~10^{11} $cm^{-2}eV^{-1}$–10^{13} $cm^{-2}eV^{-1}$) [27]. The D_{it} value is expected to be lower for the processed devices due to the mesa isolation [47]. Our data revealed no specific correlation between the oxide thickness and interface trap densities. Ideally, this is the case, but the total number of bulk defects in the oxide under the gate would depend on the thickness, more data are needed to find any correlation. It is observed that the annealed sample showed a slightly smaller trap density, which can correlate to the higher n_s, the origin of which is not yet explored.

To further investigate the β-Ga_2O_3 viability as a gate dielectric leakage current measurements were performed for all the samples. Figure 8 shows the gate leakage current in the HFET and different thicknesses β-Ga_2O_3 MOSHFET structure. There is a significant reduction in leakage current for the MOSHFET structure compared to the HFET structure in the off-stage. The leakage current at -20 V for HFET is ~10^{-4} A/cm^2, and it reduces to ~10^{-6} A/cm^2 for MOSHFET. This remarkable improvement in the gate leakage current shows that β-Ga_2O_3 can be used as an effective dielectric layer for GaN/AlGaN MOSHFETs. Table 1 summarizes the key electrical parameters of the GaN/AlGaN-based HFET and GaN/AlGaN/β-Ga_2O_3-based MOSHFET determined in this work.

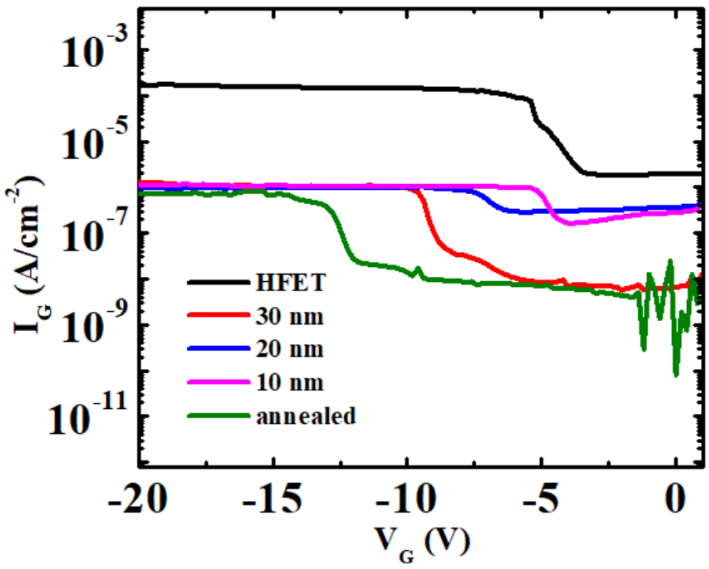

Figure 8. Gate leakage current characteristics for HFET and for different gate oxide thicknesses MOSHFET.

4. Conclusions

We have demonstrated MOCVD-grown single-crystal Ga_2O_3 thin films as a gate dielectric on AlGaN/GaN HFETs. We have found that an increase in the thickness of the dielectric layer has an impact on threshold voltage V_{th}, shifting it to more negative values and reducing the zero capacitance as additional C_{ox} is added in series. The sheet carrier densities for HFET and MOSHFETs were determined to be ~10^{13} cm^{-2}, well within the typical range- of 10^{12} cm^{-2}–10^{13} cm^{-2} for AlGaN/GaN-based devices. The leakage current was reduced by approximately 2 order from ~10^{-4} A/cm^2 for HFET to ~10^{-6} A/cm^2 for MOSHFET at −20 V. Moreover, the addition of the oxide layer did not change the sheet carrier concentration but had an impact on the calculated value of oxide charge Q_{ox}. The calculated Q_{ox} value was found to be negative and mainly responsible for depleting the 2DEG. As the thickness of the Ga_2O_3 layer increases, the Q_{ox} becomes more negative, following a trend similar to the change in V_{th} with increasing gate oxide thickness. The

charge density in the oxide–AlGaN barrier interface was found to be of the order of ~10^{12} cm^2eV^{-1}. The thermal stability, as confirmed by the annealing experiment, suggests that the MOCVD-grown single-crystal Ga_2O_3 layer could be more suitable for the gate dielectric application compared to the ALD-grown oxide due to threshold voltage stability. The moderate interface trap density and good thermal stability indicate that MOCVD-grown β-Ga_2O_3 is an excellent candidate for gate dielectric as well as a passivation layer for III-Nitride-based high-power RF MOSHFET devices.

Supplementary Materials: The following supporting information can be downloaded at: https://www.mdpi.com/article/10.3390/cryst13020231/s1. Figure S1. Frequency-dependent CV measurements of MOSHFET with (a) 20 nm thick gate oxide (b) 30 nm thick gate oxide, and (c) annealed 30 nm thick gate oxide. Figure S2. (a) Raman spectra of HFET and MOSHFET (30 nm oxide), (b) Raman spectra of Ga_2O_3 on sapphire to identify the Ga_2O_3 signature peak positions.

Author Contributions: S.H. Conceptualization of this study, Experimentation, Data curation, Methodology, Writing—original draft, M.U.J.: Revision, Experimentation, S.R.C.: Revision, Experimentation, Editing, D.L.: Revision, Experimentation, Editing, V.A.: Revision, Editing, Ü.Ö.: Revision, Editing, H.M.: Revision, Editing, I.A.: Conceptualization of this study, Visualization, Editing, Revision, Principal Investigator of this study. All authors have read and agreed to the published version of the manuscript.

Funding: This research was funded by National Science Foundation (NSF), grant number 2124624.

Data Availability Statement: The data generated during and/or analyzed during the current study are available from the corresponding authors on reasonable request.

Acknowledgments: This research was supported by National Science Foundation (NSF) award No. 2124624 managed by Dominique M. Dagenais.

Conflicts of Interest: The authors declare that they have no conflict of interest.

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