The Role of III-V Substrate Roughness and Deoxidation Induced by Digital Etch in Achieving Low Resistance Metal Contacts

Florent Ravaux, Irfan Saadat and Mustapha Jouiad *

Department of Mechanical & Materials Science and Electrical Engineering & Computer Science,
Masdar Institute of Science and Technology, A part of Khalifa University of Science and Technology,
P.O. Box 54224, Abu Dhabi 54224, UAE; fravaux@masdar.ac.ae (F.R.); isaadat@masdar.ac.ae (I.S.)
* Correspondence: mjouiad@masdar.ac.ae; Tel.: +971-02-810-9235

Abstract: To achieve low contact resistance between metal and III-V material, transmission-line-model (TLM) structures of molybdenum (Mo) were fabricated on indium phosphide (InP) substrate on the top of an indium gallium arsenide (InGaAs) layer grown by molecular beam epitaxy. The contact layer was prepared using a digital etch procedure before metal deposition. The contact resistivity was found to decrease significantly with the cleaning process. High Resolution Transmission & Scanning Electron Microscopy (HRTEM & HRSTEM) investigations revealed that the surface roughness of treated samples was increased. Further analysis of the metal-semiconductor interface using Energy Electron Loss Spectroscopy (EELS) showed that the amount of oxides (In_xO_y, Ga_xO_y or As_xO_y) was significantly decreased for the etched samples. These results suggest that the low contact resistance obtained after digital etching is attributed to the combined effects of the induced surface roughness and oxides removal during the digital etch process.

Keywords: III-V materials; digital etch; low contact resistance; HRTEM; EELS

1. Introduction

Since the emergence of the semiconductor industry in the 1950s, research orientations have been driven by the downscaling of Metal Oxide Semiconductor Field Effect Transistor (MOSFET) dimensions, as described by Moore's law and Dennard's scaling rules. As the gate dimensions are approaching a single digit node, new MOSFET performance boosters have been successfully introduced to overcome scaling issues due to lithography challenges. Thus, the integration of new materials, such as strained semiconductors, new gate materials, and high mobility channel materials, as well as new transistor architectures such as ultra-thin body, FinFet, or gate all around architectures are valuable solutions to increase MOSFET performances [1].

In this context, the integration of a lIII-V semiconductor is considered as a tangible solution for the replacement of a silicon channel. Due to its exceptional mobility, this technology is targeted for the 5–7 nm technology nodes, thanks to the successful integration of a high mobility active area on the silicon substrate (by localized epitaxial growth) [2]. Thus, the optimization of III-V semiconductor MOSFET characteristics in term of low contact resistance, doping profile, or oxide integration has attracted great interest. In light of this, the integration of performing source/drain contacts is a critical aspect of the success of III-V semiconductors for extreme dimensions/technology nodes. Historically, multilayered contacts based on gold were usually used in III-V semiconductors [3]. With this renewed interest, several techniques have been explored to overcome this technological obstacle. For instance, Ni-III-V semiconductor compounds showed low contact resistance but poor thermal stability. Nevertheless,

the integration of an interlayer between the metal and the semiconductor resulted in thermal stability improvement while availing the self-aligned advantage of this technology [4–6]. In addition, non-alloyed Mo contacts to III-V semiconductors have been also identified as a possible solution [7]. To further improve this performance, several techniques have been developed [8]. For example, the insertion of a good quality, high-k dielectric layer between the metal and silicon was found to reduce Fermi level pinning, leading to a lower specific contact resistance. This method was applied to InGaAs with relatively great success [9].

Moreover, doping was also found to decrease contact resistance once appropriately tuned [10]. Indeed, silicon implantation has historically been used for III-V MOSFET implementation, but this technique suffers from two main disadvantages: (1) the surface and the crystal are damaged during the implantation, and (2) the doping level is limited to 1×10^{19} atoms/cm^3 due to the amphoteric behavior of silicon [11]. For these reasons, two other unconventional solutions have been explored to further improve source/drain characteristics: (1) sulfur monolayer doping, which was successfully combined with Mo contacts to overcome the crystal damage induced by the implantation [12]. This technique has the advantage of giving a sharp doping profile but struggles against short channel effects. (2) Tellerium doping, which was performed during the chemical vapor deposition (CVD) growth, allows for the prevention of the crystal damage and amphoteric issues [13].

In this study, we conducted in-depth characterization investigations using advanced analytical tools to describe the role of the digital etch method as a novel surface treatment prior to metal deposition over III-V semiconductors in achieving low resistance metal contacts. Digital etching is a self-limiting etching process developed for the fabrication of optoelectronic devices, quantum devices, and nanostructures. This process allows one to control the etching rate with near-monolayer accuracy, which makes it very interesting compared to other technologies. Moreover, the monolayer self-limiting etching of silicon has been demonstrated using a four-step process (dry oxidation using chlorine gas, followed by a dry etching using argon gas) [14]. A similar technique was commonly used with III-V semiconductors, mainly for gate recess etching during the fabrication of high-electron-mobility transistors (HEMTs). As for silicon technology, a surface oxidation step, which can be dry [15,16] or wet [17,18], is followed by a wet oxide removal step.

2. Materials and Methods

The semiconductor surface treatment consists of performing an atomic layer etching of InGaAs prior to Mo deposition. In this study, the digital etch process was performed using low power O_2 plasma (100 watts) in an Asher system and wet etching at room temperature using a solution of H_2SO_4:H_2O = 1:1 for 30 s [19]. TEM lamella, used for High Resolution Transmission Electron Microscopy and Energy Electron Loss Spectroscopy (HRTEM & EELS) investigations, were then prepared using a dual beam system consisting of Focused Ion Beam and Scanning Electron Microscopy (FIB/SEM) Helios Nano Lab FEI™, using the standard method [20]. HRTEM & EELS analyses were performed using Cs corrected Titan FEI™ and Gatan™ filter, respectively.

To evaluate the effect of the digital etch process, the electrical characterization of Transmission-Line-Model (TLM) structure was carried out on two different devices prepared respectively with and without the digital etch procedure [21]. Both TLM structures were processed on a bilayer heterostructure grown on InP substrate. The bilayer heterostructure contained two main layers: 150 Å InGaAs conductive active layer and 4000 Å InP conductive buffer layer, as described in the insert of Figure 1. The cap layer consisted of two layers of heavily N-doped InGaAs (3.0×10^{19}): 50 Å layer of $In_{0.65}Ga_{0.35}As$, and 100 Å thick layer of $In_{0.53}Ga_{0.47}As$.

3. Results and Discussion

Figure 1 illustrates the TLM structure geometry consisting of an active mesa of InGaAs overlaid by two lines of Mo, separated by a distance L_D. The width L_C of the lines is equal to 220 nm. Two metal contact pads (gold) are present at these lines ends. The function of these metal pads is to force the

current flowing through the Mo/InGaAs interface and mesa while probing the voltage difference between the two Mo lines. The resistance is then calculated for different devices with various L_D values [22].
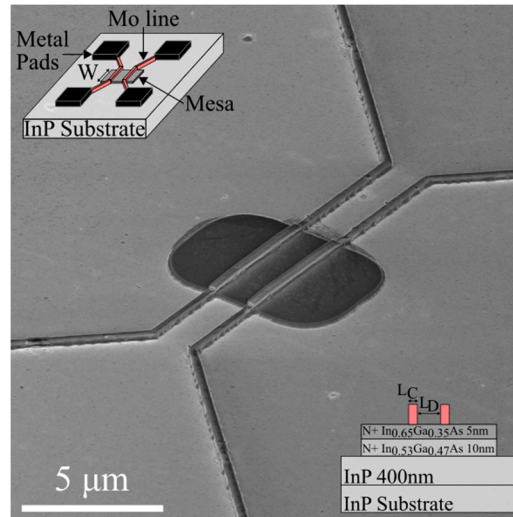

Figure 1. SEM image of the Transmission-Line-Model (TLM) device. The inserts represent the TLM structure scheme (**top**) and the cross-section showing different layers of the active area (**bottom**).

3.1. Resistivity

Figure 2 provides the electrical characterization of the two different devices. The normalized resistance is given as a function of L_D (the distance separating the Mo lines). The specific contact resistance is then extracted by fitting the model with experimental data for structures processed with and without digital etch [21]. The use of the digital etch procedure allows one to obtain an 84% decrease of the specific contact resistance, namely dropping from 1.365 $\Omega \cdot \mu m^2$ to 0.710 $\Omega \cdot \mu m^2$. These results are lower than those obtained by Zhang [7] (10 $\Omega \cdot \mu m^2$ for Mo/InGaAs), but higher than those obtained by Liao [9] (0.67 $\Omega \cdot \mu m^2$ for Al/ZnO/InGaAs).
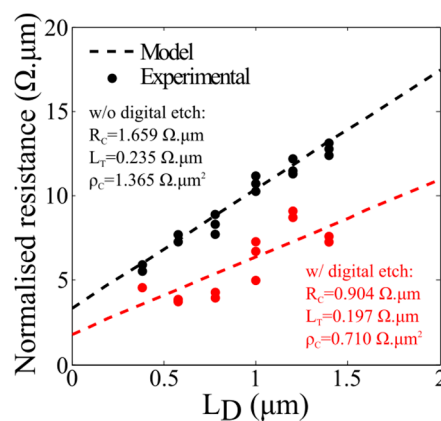

Figure 2. Variation of normalized resistance as a function of contact spacing L_D.

3.2. Device Conformity

Figure 3a,b show the High Resolution Scanning Transmission Electron Microscope (HRSTEM) micrographs of the device and the metal/semiconductor interface, which are the most convenient to check the different steps of the process flow. Based on these images, two main remarks can be made

regarding the structure of the device. First, the SiO$_2$ deposition seems to be conformal because the covering of the line is uniform at the edges at a very high magnification. The hard mask thickness appears to be sufficient to protect the InGaAs layer during the mesa patterning by plasma etching. Hence, lateral etching is observed to be below the hydrogen silsesquioxane (HSQ) negative resist during the Reactive Ion Etching (RIE) Mo lines patterning. Despite this isotropy, the etching presents good selectivity over InGaAs because the layer thickness seems to be constant over the whole mesa. The dark field STEM image (cf. Figure 3b) highlights the InGaAs layer, which is also present along the whole interface, meaning that the metal deposition was efficient and nondestructive.

3.3. Interface Probing

Figure 3c,d give HRTEM images of the Mo/InGaAs interface for both samples with and without digital etch. The interfaces quality was first checked along the 3-µm Mo lines on multiple samples treated with digital etching. The deposited Mo lines exhibit good uniformity and a uniform thickness. One can clearly notice (Figure 3d) the presence of the surface roughness, which was generated by digital etching during the contact surface preparation, whereas this contact surface appears flat in Figure 3c for the untreated sample. A maximum height of 3 nm was measured in all observed samples. This effect is generally observed on the surface morphology during the digital etch process for different materials and different wet etchants [23]. Therefore, we believe that these serrated lines present in the interface due to the surface roughness allow one to obtain a large contact surface of the Mo layer over the InGaAs surface, leading to a significant decrease in the contact resistance.
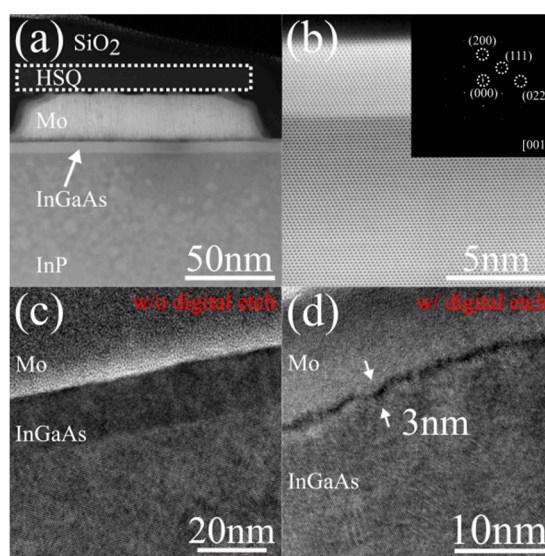

Figure 3. (**a**) STEM-HAADF (High-Annular Angle Dark Filed) cross-sectional image; (**b**) HR-STEM of the InGaAs layer (insert shows the Fast Fourier Transform FFT); TEM images of (**c**) the untreated sample and (**d**) the sample prepared with digital etch.

It is worth noting that the HRTEM investigations provided us with one possible reason (surface roughness) behind the low contact resistance obtained for the treated sample; nevertheless, additional investigations were performed to further comprehend such a low value. Therefore, the correlation between the digital etch process and its effect on local chemistry, especially at the interface, attracted great interest. To screen the chemical composition at this fine region, we combined both HR-STEM and EELS techniques. These techniques allow one to probe the interface quality in terms of defects and at the same time it provides the local chemistry to evaluate the reactivity of Mo with InGaAs [24,25].

Figure 4a,b show the line scans across the Mo/InGaAs interfaces using EELS for the untreated sample and the digital etched sample, respectively. The EELS spectra were recorded along the black

arrows. The energy window was decreased and limited to 520–570 eV range to increase the resolution of the oxygen k-edge detection.
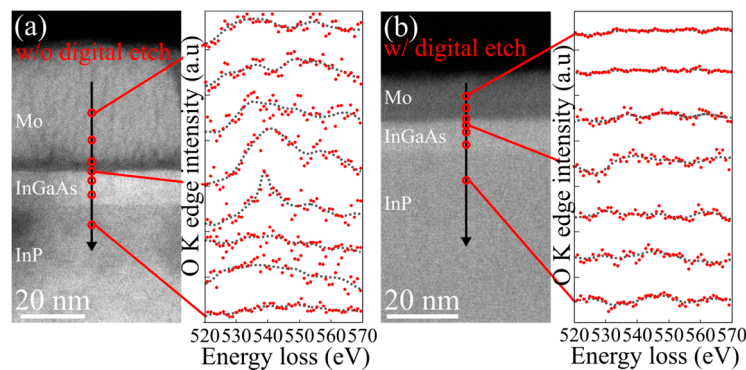

Figure 4. STEM-HAADF image of the metal/semiconductor interface of sample (**a**) without the digital etch treatment and (**b**) with the digital etch treatment. The arrow represents the localization of the EELS spectra recorded point-by-point.

Close inspection of the energy spectra, especially around the peak value of 535 eV, which is the signature of the oxygen k-edge, reveals the presence of this peak for the untreated sample. This peak appears broad in the upper and bottom layers, but it is more acute and sharp when crossing the interface. In the contrast, for the digital etched sample, the peaks remain flat for all scanned regions; this shows the absence of oxygen atoms at the interface for the treated sample. This result suggests then that oxides such as In_xO_y, As_xO_y, and the more energetically favored oxide Ga_xO_y may be present at the interface between Mo and the InGaAs layers [26,27], but that they had been successfully removed by the digital etch process. This finding brings an additional fact that can be considered as another reason behind the low contact resistance measured in digital etched samples.

4. Conclusions

Thanks to the digital etch process, we obtained contact resistance values as low as 0.710 $\Omega \cdot \mu m^2$ for InGaAs compound. This low resistance is attributed to two main factors generated by the digital etch process, namely: (1) large contact surface due to the surface roughness, and (2) the oxides removal during the etch process.

Author Contributions: Florent Ravaux and Irfan Saadat designed and fabricated the devices. Florent Ravaux and Mustapha Jouiad characterized the devices and analyzed the data. Florent Ravaux and Mustapha Jouiad wrote the paper.

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