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Enhanced Fault Current-Limiting Circuit Design for a DC Fault in a Modular Multilevel Converter-Based High-Voltage Direct Current System

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Abstract: The main weakness of the half-bridge modular multilevel converter-based high-voltage direct current (MMC-HVDC) system lies in its immature solution to extremely high current under direct current (DC) line fault. The development of the direct current circuit breaker (DCCB) remains constrained in terms of interruption capacity and operation speed. Therefore, it is essential to limit fault current in the MMC-HVDC system. An enhanced fault current-limiting circuit (EFCLC) is proposed on the basis of fault current study to restrict fault current under DC pole-to-pole fault. Specifically, the EFCLC consists of fault current-limiting inductance L_{FCL} and energy dissipation resistance R_{FCL} in parallel with surge arrestor. L_{FCL} reduces the fault current rising speed, together with arm inductance and smoothing reactor. However, in contrast to arm inductance and smoothing reactor, L_{FCL} will be bypassed via parallel-connected thyristors after blocking converter to prevent the effect on fault interruption speed. R_{FCL} shares the stress on energy absorption device (metal oxide arrester) to facilitate fault interruption. The DCCB requirement in interruption capacity and breaking speed can be satisfied effortlessly through the EFCLC. The working principle and parameter determination of the EFCLC are presented in detail, and its effectiveness is verified by simulation in RT-LAB and MATLAB software platforms.

Keywords: fault current-limiting circuit; DC circuit breaker; MMC-HVDC; fault protection

1. Introduction

Fault vulnerability and protection immaturity constrain the development of the voltage source converter-based high-voltage direct current (VSC-HVDC) system, especially in terms of DC side fault at high power levels. Thus, reliability has become an important challenge in multilevel converter-based (MMC)-HVDC with long-distance transmission lines [1,2]. The lack of a perfect fault isolation scheme and mature DC switchgear products are the primary issues [3]. However, the VSC-HVDC system has attracted worldwide attention and research interests due to its advantages with respect to control flexibility and interconnection feasibility. A related analysis of DC faults has been performed to enhance its fault ride through (FRT) ability under DC fault in the VSC-HVDC system [4,5]. An overview of HVDC system protection mentions that the major limitation in development of VSC-HVDC is the inability to limit fault current, given the limitation of the DC circuit breaker (DCCB) in interruption capability and operation speed [6]. Moreover, limiting fault current can protect the semiconductor device from excessive electrical pressure, particularly insulated gate bipolar thyristor (IGBT) and

freewheeling diode in a converter sub-module (SM). Furthermore, restriction of fault current can provide additional time for fault detection and operation delay. Therefore, limiting fault current development and propagation in the VSC-HVDC and multi-terminal HVDC (MTDC) systems is essential.

State-of-the-art fault current-limiting (FCL) techniques can be classified into improved SM topologies [7–12], auxiliary FCL circuits (FCLC) [13–20], and fault current limiters [21–25]. The SM topology has been modified to reinforce its fault handling ability, because the classical half-bridge SM (HBSM) is likely to be destroyed under overcurrent if no proper protection scheme is applied, even if insulated gate bipolar translators (IGBTs)are blocked in a timely fashion [26]. Thus, several innovative improvements, including full-bridge SM (FBSM) [7,8], clamp double SM (CDSM) [9], and hybrid SM, which combines FBSM and HBSM, have been conceived in the SM topology design [10]. Although the FBSM solution can ride through faults without blocking the converter, given its ability to output bipolar voltage, regardless of arm current direction [9], the doubled number and on-state loss of semiconductors are their main drawbacks. A CDSM solution only has 50% higher semiconduction than the HBSM to extinguish the DC arc by blocking IGBTs under nonpermanent fault [10]. However, the MMC converter has generally been regarded as the most appropriate static synchronous compensator to support alternating current (AC) grids in DC pole-to-pole fault scenarios [11]. Thus, enhancing the FRT capability without blocking the converter is crucial. A hybrid MMC topology requires each arm to have the same amount of FBSM and HBSM by considering their nature [10,12]. Thus, the cost of semiconductor devices and conduction losses have been reduced in comparison with those in the FBSM. However, further research on control strategies in terms of dynamic characteristics and SM voltage balancing is required [2]. Overall, control complexity and high cost are the weaknesses of SM topology-based solutions.

Another FCL technology relies on an auxiliary circuit, which consistently includes energy dissipation resistance and an FCL reactor. For example, a hybrid current-limiting circuit (Figure 1a) has been designed to restrain the DC line fault current in the MTDC system [13], which is settled at the end of the DC line between the DCCB and DC converter ports. The energy dissipation resistance R_r is equipped to share the stress on energy absorption element in the DCCB, and the fault current interruption speed is accelerated. However, the tradeoff between FCL performance and the extra cost of the resistor must be considered. In addition, a bridge-type FCLC is composed of a DC voltage source, a DC reactor, and four groups of diodes (Figure 1b) [14]. Reference [14] shows that the DC biased current given by the DC power supply is considered to be the threshold value of the DC fault current in order to automatically activate the FCLC itself. The main advantage is that the DC reactor can be bypassed in its normal state and after turning off the main breaker of the DCCB. In addition, the idea of the FCLC is also reflected in the form of an SM [15], which is inserted into each arm in series. However, the FCL-SM can only limit a unidirectional fault current, and the surge voltage across FCL-SM must be given further attention. Moreover, an enhanced reverse blocking SM (ERBSM) topology has been proposed to extinguish a fault current arc by inverse voltage [16]. Control complexity is reduced because the ERBSM adopts the same modulation strategy. In Reference [17], thyristors have better performance than diode in withstanding overcurrent (Figure 1e), and the overcurrent pressure on freewheeling diode has been relieved via the shunting effect of a single-thyristor switch scheme (STSS) [17–19]. Although the STSS can protect semiconductor devices, the AC grid current fed into the DC side cannot be prevented. Thus, the double-thyristor switch scheme (DTSS) has been introduced to protect the DC overhead line (Figure 1f), which can eliminate the freewheeling effect of diodes, and the DC line fault current can freely decay to zero [20]. Then, the DC fault is transformed into an AC short circuit fault that can be cleared by switching off the thyristor. However, the high dv/dt across thyritors and the sharing current effect of bypassed diodes are ignored in the DTSS solution. To solve this problem, double-thyristor switches are combined and connected at the AC port of the converter instead of across the diode in the SM to isolate the AC side from the DC side when a fault occurs. Moreover, the feasibility of such a scheme has been verified via a case study that considers STSS and DTSS in a classical VSC-HVDC system, as well as MMC-HVDC.

The superconducting fault limiter (SFCL) has attracted considerable attention because its nonlinear impedance characteristics can be used to limit the increase in fault current rate to provide a necessary time for relay protection. The SFCL can mainly be divided into resistive-SFCL (R-SFCL) and inductive-SFCL (I-SFCL) [21]. The study concludes that R-SFCL can constrain the amplitude of fault current, but reduces the increase in fault current rate differently, and I-SFCL can delay the increase in fault rate significantly [22]. Related research has been performed on the basis of the unique characteristics in SFCL. For example, R-SFCL has been thoroughly investigated on the basis of the current-limiting capability comparison and parameter influence, thus indicating that the use of R-SFCL is suggested for real applications, provided that it is sufficiently sensitive to develop an adequate quenching resistance [23]. Hybrid DCCB has been equipped with SFCL in the main line to limit the fault current until a fault is completely interrupted [24,25]. In addition, the superconducting magnetic energy storage technique has been adopted to limit fault current, which is achieved via a power transform between the power system and superconducting coil [26]. A rapid limitation can be realized when controlled FCL (molded as pancakes) is isolated to maintain its dynamic stability.

In contrast to the AC line fault current, the fault current under DC short circuit fault in the MMC-HVDC system does not have a natural zero crossing. Thus, applying DCCB has been limited given its high cost and technical immaturity [27]. Mechanical breakers can limit fault current in a few tens of milliseconds but cannot satisfy the demand in the VSC-HVDC system protection [28]. Although semiconductor circuit breakers have a large on-state loss, the operation speed requirement is satisfied. The hybrid HVDC breaker has been proposed and investigated in References [29–31] to eliminate on-state power loss and limit fault current within several milliseconds. Parametric analysis of hybrid DCCB has also been conducted thoroughly considering the influence of the main parameters on the system and the breaker design [32]. Moreover, an interlink DCCB has been proposed to maintain the fault current interruption ability with a few components to reduce the overall cost of the DCCB in the DC grid [33].

In Reference [24], varying the DC current is considered an underdamping decay process, given the small resistance in the fault circuit. Thus, the fault current-limiting inductance L_{FCL} cannot change the damping characteristics which refer to criterion $R < 2\sqrt{L/C}$. That is, L_{FCL} can only limit DC fault current, but not relieve the overcurrent effect in the converter and AC sides [24]. The SFCL has not been applied extensively in real projects because of its high cost and lack of maturity, particularly with respect to SFCL recovery after being activated. The main advantage of the SFCL is that it does not influence the dynamic response under normal state. The direct installation of the DC reactor affects the system's normal operation and DCCB isolation speed [34]. Therefore, the present study proposes an enhanced fault current-limiting circuit (EFCLC) that primarily consists of energy dissipation resistance, limiting reactor, surge arrester, and semiconductor switches on the basis of existing works. The EFCLC aims to limit fault current through converter arms and DC line before the DCCB operates, thereby decreasing the peak current for fault interruption and reducing overcurrent effect on converter arms. Moreover, the required DCCB capability could be reduced, given limited fault current with EFCLC and more time is saved for fault detection, since fault current rising speed is more or less restricted.

The remainder of this paper is organized as follows. Section 2 thoroughly analyzes DC fault current on the basis of theoretical calculation and simulation verification. Section 3 presents the topology and working principle of EFCLC. Section 4 performs the parametric design study of EFCLC. Section 5 further investigates the proposed scheme with EFCLC in terms of FCL ability and cost. Finally, Section 6 summarizes the conclusion and future scope.

2. DC Fault Current Analysis

2.1. Test System Introduction

The scheme of the MMC-HVDC system can be categorized into monopolar and bipolar symmetrical wiring systems (Figure 1). The monopolar symmetrical HVDC system is also known as the pseudo

bipolar HVDC system, which typically adopts a cable as a DC line. However, a real bipolar HVDC system is commonly applied in the HVDC transmission system with a high-capacity and overhead DC line. The main difference between the two schemes lies in operation mode. Bipolar systems can work under both monopolar mode and bipolar mode. Namely, the power transmission of the positive pole overhead line and negative pole overhead line is independent. Therefore, bipolar systems can work during fault by transferring power through healthy line (monopolar mode). In contrast, monopolar systems cannot maintain power transmission under fault, since they only operate under monopolar mode. Hence, the bipolar system demonstrates advantages in terms of power supply reliability and FRT capability.

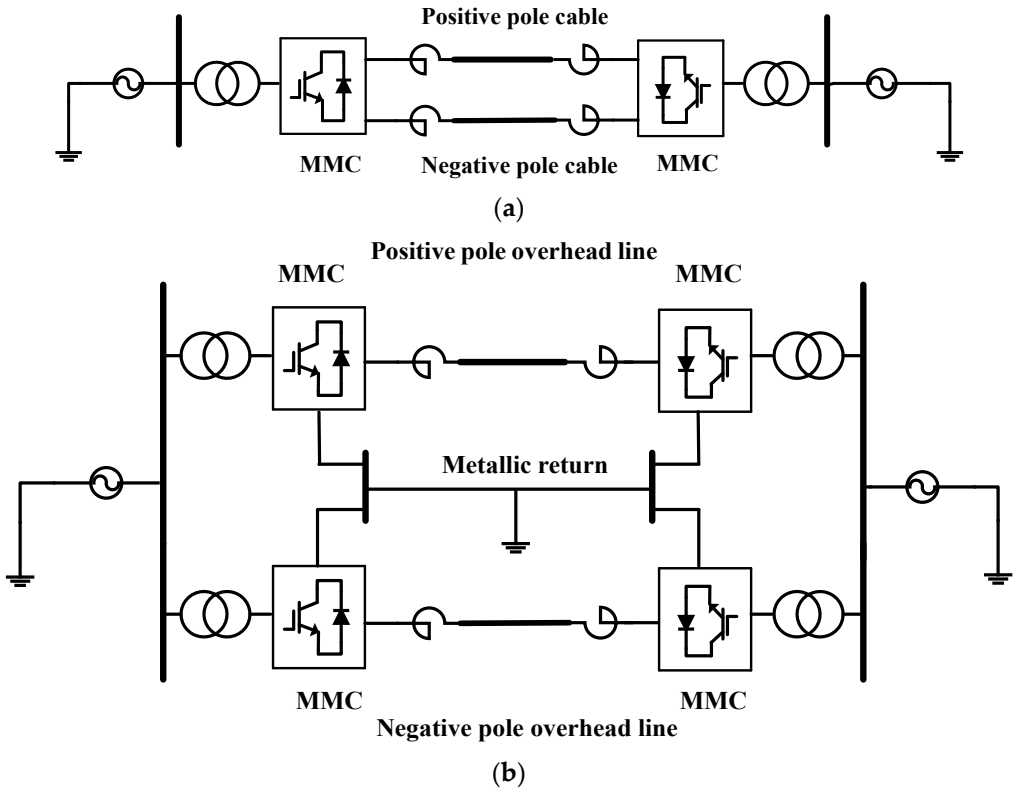


Figure 1. Diagram of the modular multilevel converter-based high-voltage direct current system in (**a**) monopolar symmetrical wiring and (**b**) bipolar symmetrical wiring.

The MMC-HVDC system mainly consists of modular multilevel converter stations and DC line parts. The topology structure of MMC, which includes three converter units, is displayed in Figure 2. Each unit involves upper and lower bridge arms that are connected with the bridge arm reactor L_0. The SMs are connected in series in every bridge arm, which consists of two switches, namely, T_1 and T_2 (IGBT); anti-parallel connected diodes, namely, D_1 and D_2; and energy storage capacitor C_0. The DC voltage is maintained by switching T_1 and T_2 on and off in every SM tripped by a control signal. If the amount of SMs in each converter unit is 2N, then it has N switched-on and N switched-off SMs during normal operation. The DC side voltage U_{DC} is equal to the sum of the switched-on SM voltage U_0. The main modulation modes are divided into pulse width modulation and nearest level modulation. The converter stations are blocked by turning off IGBTs in all SMs given the local overcurrent protection when a current reaches a threshold value (normally twice the value of the nominal current).

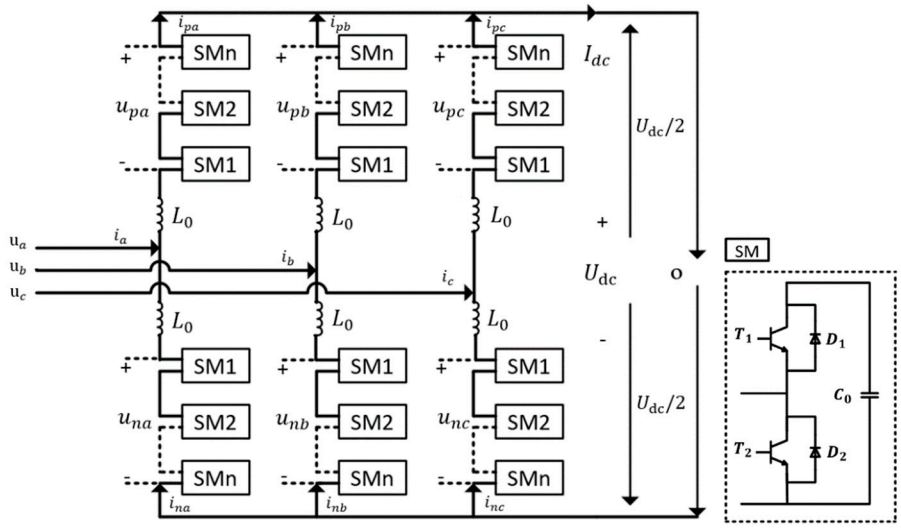


Figure 2. Topology structure of the MMC.

2.2. DC Fault Analysis of the Test System

In the monopolar MMC-HVDC system, the DC line is typically composed of cables because the fault possibility is considered much lower in cables than in overhead lines [35]. However, an overhead line is typically adopted in the bipolar system, especially in long-distance power transmission with a high capacity. Given that an overhead line is likely to be affected by a short circuit, grounded fault, and nonpermanent fault, analyzing the fault characteristics for protection relaying is necessary. The DC line faults are mainly classified into a single pole-to-ground fault, pole-to-pole short-circuit fault (PPF), and line disconnection. The PPF is regarded as a serious fault considering an extremely high fault current within a few milliseconds after fault occurrence. In Figure 2, the MMC-HVDC scheme indicates that the single pole-to-ground fault in the bipolar system can be equivalent to the PPF given bipolar system's metallic return is connected to ground. Therefore, the PPF is selected to be investigated in this study, especially in terms of fault current. Fault current propagation can be segmented into SM capacitor discharging before blocking IGBT, decayed freewheeling current, and AC gird in-feed current after blocking IGBT. Before blocking IGBT, the discharging capacitor in inserted SMs leads to surge current, which provides a high electrical pressure on semiconductor devices. Thus, from a protection perspective, IGBT is blocked with a control signal when the arm current reaches the threshold value.

2.2.1. Submodule Capacitor Discharging Period

At the beginning of the PPF, the capacitor in every inserted SM discharges and bridge arm current surges. Figure 3 depicts the fault current circuit, in which the capacitor discharging current flows through the IGBT of the inserted SMs and the anti-parallel diode of the removed SMs in each converter unit. The fault occurs at point A and point B, which are connected with dashed line in Figure 3. Considering that converter includes six arms with same topology, hence, only the upper arm of phase A is shown with insert SMs and removed SMs due to the space of figure and simplicity. All the IGBT can be turned off as the bridge arm current reaches the threshold value to protect the IGBT from overcurrent damage. The voltage cross converter unit v_{conv} decreases with SM capacitor discharging until the IGBT is blocked. In contrast to the two-level VSC-HVDC system under the PPF, in which a large capacitor connected to the DC side discharges to zero, even if IGBT is blocked (assuming the resistance in fault circuit $R_{eq} < 2\sqrt{L_{eq}/C_{eq}}$), the voltage of the SM capacitor is normally maintained given the blocked IGBTs in the MMC-HVDC system. If v_{conv} is higher than the AC grid line voltage v_{sj_line} (j indicates phases a, b, and c), then the AC grid current cannot be fed in the fault current loop. If V_{conv} is lower than the AC grid line voltage, then the AC grid begins to feed the AC current i_{sj} (j indicates phases a, b, and c) into the fault current loop. In Figure 3, the red dashed line indicates the

fault currents i_{sj} fed from the AC grid; these fault currents are equally divided into an upper arm current i_{pj_ac} and a lower arm current i_{nj_ac} (not marked in the figure due to complexity). The blue dashed–dotted line represents the capacitor discharging path, and i_{cj} expresses the discharging arm currents. Both AC feeding current in red and SM capacitor discharging current in blue flow through inserted SMs and removed SMs in each arm. Specifically, the fault current flows through freewheeling diode in removed SMs and capacitor and on-state IGBT in inserted SMs, shown in Figure 3. The equivalent circuits of the two fault current paths are exhibited in Figure 4a,b. However, the AC feeding current can be ignored in comparison with the capacitor discharging current during this period.

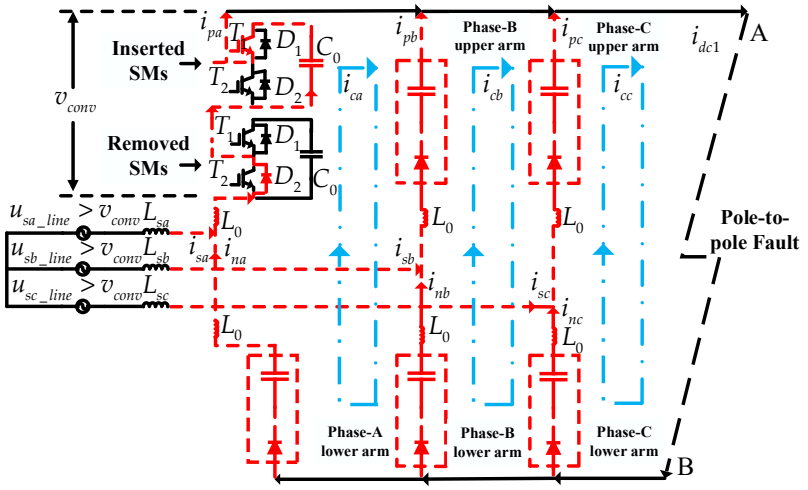


Figure 3. Direct current pole-to-pole fault circuit diagram before blocking submodules.

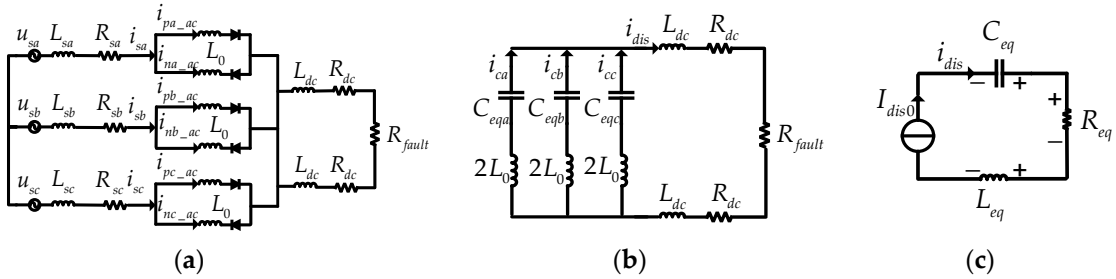


Figure 4. (**a**) Equivalent AC grid feeding current circuit, (**b**) equivalent SM capacitor discharging current circuit, (**c**) simplified SM capacitor discharging current circuit.

The equivalent phase capacitor C_{eq} demonstrated in Figure 4b is normally considered $\frac{2C_0}{N}$ in the existing references [5,6,15,17]. However, Reference [36] proposed that the calculation value of the fault current with $C_{eq} = \frac{C_0}{N}$ is close to the simulation value. Furthermore, C_{eq} is obtained as $\frac{1.4\ C_0}{N}$ for the optimal approximation of the discharging current via a tracing point method [37]. Consequently, Reference [38] verified that C_{eq} of the three converter units depends on the fault time t_f and modulation ratio m, as expressed in Equation (1). Thus, the selection of fault time t_f and modulation ratio m should be reconsidered in this paper. Based on equivalent capacitor expression in Equation (2), the relationship between discharging coefficient σ and time is shown in Figure 5, given the preset modulation ratio m (0.93) of test system. From the perspective of fault protection, the most serious situation must be considered in selecting t_f. According to the red curve in Figure 5, the maximum discharging coefficient σ is obtained when $t_f = \frac{k\pi}{3}$, $k = 0, 1, 2 \ldots$. Namely, the maximum C_{eq} equals 1.473, since the fault time of the simulation is set at 1.2 s.

$$C_{eq} = \frac{2C_0}{[1 + m^2 \sin^2(\omega t)]N} + \frac{2C_0}{[1 + m^2 \sin^2(\omega t - \frac{2}{3}\pi)]N} + \frac{2C_0}{[1 + m^2 \sin^2(\omega t + \frac{2}{3}\pi)]N} \quad (1)$$

$$C_{eq} = \sigma \frac{C_0}{N} \tag{2}$$

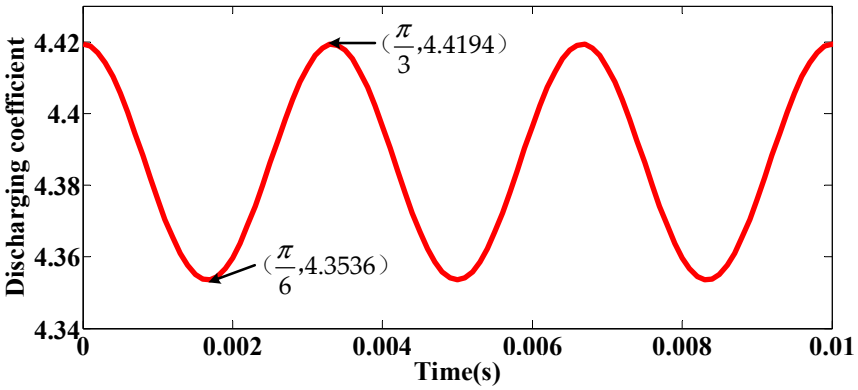


Figure 5. Relationship between discharging coefficient and fault time (m = 0.93).

During the SM capacitor discharging period, the AC feeding current can be ignored, because the discharging current is dominant. For example, the Phase-A discharging circuit can be regarded as a second-order RLC circuit (circuit consisting of a resistor, an inductor and a capacitor), as displayed in Figure 4c. Here, the resistance in the arms is neglected. The initial voltage and current of the capacitor discharging circuit are expressed by Equations (3) and (4), respectively.

$$u_c(0_+) = u_c(0_-) = U_{dc} \tag{3}$$

$$i_{dis}(0_+) = i_{dis}(0_-) = -C_{eq}\frac{du_c}{dt} = I_{dis0} \tag{4}$$

The equivalent capacitor, inductance, and resistance presented in Figure 4c are obtained as follows:

$$C_{eq} = \frac{\sigma C_0}{N} \tag{5}$$

$$L_{eq} = \frac{2}{3}L_0 + 2L_{dc} \tag{6}$$

$$R_{eq} = R_{fault} + 2R_{dc} \tag{7}$$

The second-order equation of the RLC circuit is expressed in Equation (8) as follows:

$$\frac{d^2 i_{dis}}{dt} + \frac{R_{eq}}{L_{eq}}\frac{di_{dis}}{dt} + \frac{1}{L_{eq}C_{eq}}i_{dis} = 0 \tag{8}$$

$$i_{dis}(t) = e^{-\frac{t}{\tau}}\left[U_{dc}\sqrt{\frac{C_{eq}}{L_{eq}}}\sin(\omega_1 t) - \frac{I_{dis0}\omega_0}{\omega_1}\sin(\omega_1 t - \theta)\right] \tag{9}$$

$$\tau = \frac{2L_{eq}}{R_{eq}} = \frac{2(\frac{2}{3}L_0 + 2L_{dc})}{2R_{dc} + R_{fault}} \tag{10}$$

$$\omega_1 = \sqrt{\frac{1}{L_{eq}C_{eq}} - \left(\frac{R_{eq}}{2L_{eq}}\right)^2} \tag{11}$$

$$\omega_0 = \sqrt{\frac{1}{L_{eq}C_{eq}}} \tag{12}$$

$$\theta = \arctan(\omega\tau) \tag{13}$$

where τ is the attenuation coefficient of the capacitor discharging current, ω_1 is the oscillating current angular frequency, ω_0 is the inherent angular frequency of the circuit, and θ is the initial phase angle of the initial current. The capacitor discharges until the capacitor voltage decreases to 0. The maximum discharging current can be obtained at t_{dis_peak} without blocking IGBT.

$$t_{dis\_peak} = \frac{1}{\omega_0}\arctan\left(\frac{U_{dc}}{I_{dis0}}\sqrt{\frac{C_{eq}}{L_{eq}}}\right) \tag{14}$$

$$I_{dis\_peak} = e^{-\frac{t_{dis\_peak}}{\tau}}\left(U_{dc}\sqrt{\frac{C_{eq}}{L_{eq}}} + \frac{I_{dis0}\omega_0 L_{eq}}{U_{dc}}\right)\sqrt{\frac{U_{dc}^2}{I_{dis0}^2\omega_0^2 L_{eq}^2 + U_{dc}^2}} \tag{15}$$

The AC side can be considered a three-phase short-circuit fault under the DC pole-to-pole fault, and the DC fault current only consists of the discharging currents of the three converter units, given the balance fault on the AC side. Thus, the fault current through DC line is defined as

$$i_{dc}(t) = i_{dis}(t) \tag{16}$$

For example, Phase-A arm current during this period can be decomposed using Equations (17) and (18).

$$i_{pa}(t) = \frac{1}{3}i_{dc}(t) + \frac{1}{2}i_{sa}(t) \tag{17}$$

$$i_{na}(t) = \frac{1}{3}i_{dc}(t) - \frac{1}{2}i_{sa}(t) \tag{18}$$

The Phase-A voltage on the AC side is set as

$$u_{sa} = \sqrt{2}U_s\sin(\omega_s t + \theta_a) \tag{19}$$

where θ_a is the phase angle (taken as 0 for convenience in calculation afterward), and ω_s is the fundamental angular frequency. Then, the Phase-A current can be obtained using Equation (20).

$$i_{sa} = \frac{\sqrt{2}U_s}{Z_{eq}}\sin(\omega_s t + \theta_a - \varphi) \tag{20}$$

where φ is the impedance angle. The AC feeding current in each phase is equally divided into upper and lower arms.

$$i_{pa\_ac}(t) = i_{na\_ac}(t) = \frac{1}{2}\frac{\sqrt{2}U_s}{Z_{eq}}\sin(\omega_s t + \theta_a - \varphi) \tag{21}$$

$$Z_{eq} = \sqrt{R_{sa}^2 + \omega_s\left(L_s + \frac{1}{2}L_0\right)^2} \tag{22}$$

$$\varphi = \arctan\left(\frac{L_{sa} + \frac{1}{2}L_0}{R_{sa}}\right) \tag{23}$$

In accordance with Equations (9), (16)–(18), and (21), the expression of the Phase-A arm current can be obtained.

$$i_{pa} = \frac{1}{3}e^{-\frac{t}{\tau}}\left[U_{dc}\sqrt{\frac{C_{eq}}{L_{eq}}}\sin(\omega_1 t) - \frac{I_{dis0}\omega_0}{\omega_1}\sin(\omega_1 t - \theta)\right] + \frac{1}{2}\frac{\sqrt{2}U_s}{Z_{eq}}\sin(\omega_s t + \theta_a - \varphi) \tag{24}$$

$$i_{na} = \frac{1}{3}e^{-\frac{t}{\tau}}\left[U_{dc}\sqrt{\frac{C_{eq}}{L_{eq}}}\sin(\omega_1 t) - \frac{I_{dis0}\omega_0}{\omega_1}\sin(\omega_1 t - \theta)\right] - \frac{1}{2}\frac{\sqrt{2}U_s}{Z_{eq}}\sin(\omega_s t + \theta_a - \varphi) \tag{25}$$

2.2.2. Freewheeling Current and AC Feeding Current Period

The fault current circuit after completely discharging IGBT blocks or capacitor to $V_{conv} = 0$ is depicted in Figure 6, in which the red dotted line indicates the AC feeding current, and the blue dash-dotted line represents the freewheeling current given the stored energy in the arm reactors. The equivalent circuits of the AC feeding and freewheeling DC currents are illustrated in Figure 7a,b, respectively. The fault current can be considered a superposition of the three-phase short-circuit fault and decayed freewheeling currents. Thus, the fault currents in the upper and lower arms can be defined as

$$i_{pj} = i_{fwj} + i_{pj\_ac} \tag{26}$$

$$i_{nj} = i_{fwj} - i_{nj\_ac} \tag{27}$$

where i_{fwj} denotes the freewheeling current in each converter phase. i_{pj_ac} and i_{nj_ac} indicate the AC feeding current via the upper and lower arms of each phase, respectively. The analysis during the SM capacitor discharging period shows that the initial freewheeling current is equal to the peak value of the discharging current in each converter phase.

$$I_{fw0} = \frac{1}{3} I_{dis\_peak} \tag{28}$$

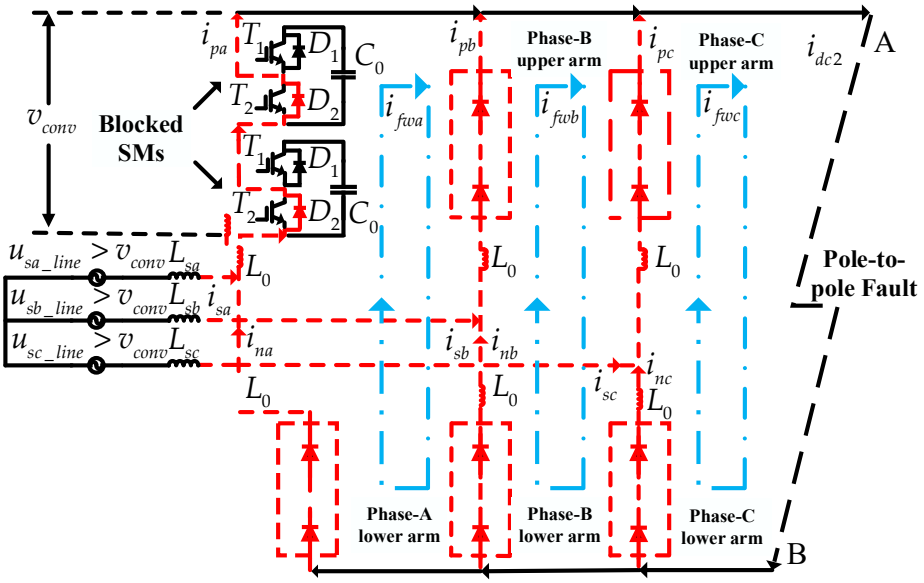


Figure 6. Diagram of the DC pole-to-pole fault circuit after blocking SMs.

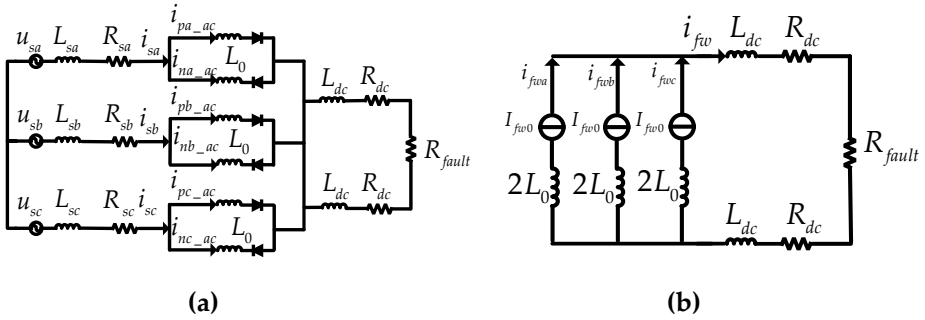


Figure 7. Equivalent circuit of the (**a**) AC feeding current and (**b**) freewheeling DC current.

Thus, the freewheeling current of each arm and the DC line current can be obtained using Equations (29) and (30).

$$i_{fwj}(t) = I_{fw0}e^{-\frac{t}{\tau_1}} \tag{29}$$

$$i_{dc}(t) = 3I_{fw0}e^{-\frac{t}{\tau_1}} \tag{30}$$

For example, the initial arm current of the freewheeling period of Phase A is expressed as follows:

$$I_{pa\_bk} = I_{fw0} + \frac{1}{2}i_{sa}(t_{dis\_peak}) \tag{31}$$

$$I_{na\_bk} = I_{fw0} - \frac{1}{2}i_{sa}(t_{dis\_peak}) \tag{32}$$

Similarly, the arm currents can be decomposed as Equations (33) and (34).

$$i_{pa}(t) = i_{fwa}(t) + i_{pa\_ac}(t) \tag{33}$$

$$i_{na}(t) = i_{fwa}(t) - i_{na\_ac}(t) \tag{34}$$

In reference to Equations (21) and (28), the arm currents can be defined as

$$i_{pa}(t) = \frac{1}{3}I_{dis\_peak}e^{-\frac{t}{\tau_1}} + \frac{1}{2}\frac{\sqrt{2}U_s}{Z_{eq}}\sin(\omega_s t + \theta_a - \varphi) \tag{35}$$

$$i_{na}(t) = \frac{1}{3}I_{dis\_peak}e^{-\frac{t}{\tau_1}} - \frac{1}{2}\frac{\sqrt{2}U_s}{Z_{eq}}\sin(\omega_s t + \theta_a - \varphi) \tag{36}$$

$$\tau_1 = \frac{2(2L_0+2L_{dc})}{2R_{dc}+R_{fault}} \tag{37}$$

where τ_1 is the attenuation coefficient of the freewheeling current. Equivalent impedance is expressed in Equation (22), and the peak value of the discharging current can be obtained via Equation (15).

2.3. Simulation Verification

The analyses of the arm and DC line currents have been verified via a simulation. The monopolar MMC-HVDC system is adopted in this study, and the model parameters are listed in Table 1. The rectifier side takes DC voltage and active power control, and the inverter side adopts active and reactive power controls. The protection action, including blocking IGBTs, is disregarded in the simulation to investigate the natural response to a fault. A completely discharged SM capacitor can be equivalent to blocking IGBTs at t_{dis_peak}. The comparison between the calculation and the simulation in terms of DC line and arm currents (Phase-A upper arm) is depicted in Figures 8 and 9, respectively. Figure 8 demonstrated that the DC line current increases to a high level in a few milliseconds. The IGBTs must be blocked rapidly due to the electrical pressure on the DC line. The DC line current decays after completely discharging the SM capacitor. Similarly, the arm current accelerates during the discharging period (Figure 9) but involves the AC feeding component after completely discharging the SM capacitor at 1.213 s. The difference between the simulation and calculation values in the arm current before 1.213 s may be attributed to the imbalance shunt current among the converter units. In addition, the initial AC current at fault time (1.2 s) is ignored in the calculation, thereby leading to more or less error. However, the overall accuracy of the calculation analysis can be accepted for fault study on the basis of the general consistency between the simulation and calculation curves in Figures 8 and 9.

Table 1. Parameters of the modular multilevel converter-based high-voltage direct current system's simulation model.

System Parameters			
DC voltage	±420 kV	SM number (2 N)	60
Rated power	1250 MW	Arm inductance	140 mH
Short-circuit ratio	20	Internal grounding	Yg
AC voltage	450 kV	AC line length	10 km
Frequency	50 Hz	Line resistance	12.73 mΩ/km
Transformer voltage	525 kV/450 kV	Line inductance	0.9937 mH
Transformer grounding	Yn/yn	Line capacitance	12.74 nF/km
Smoothing inductance	20 mH	DC line length	200 km

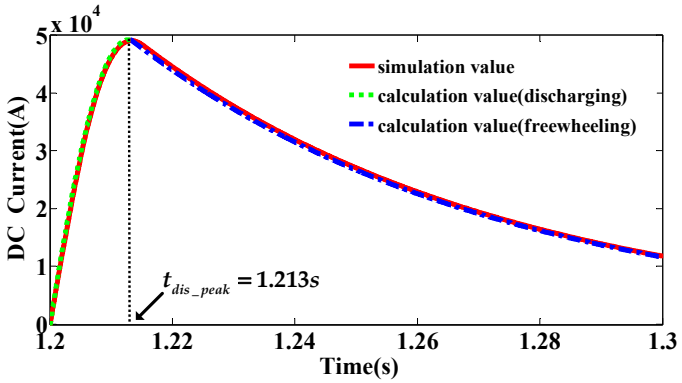


Figure 8. Simulation and calculation values of the DC line current.

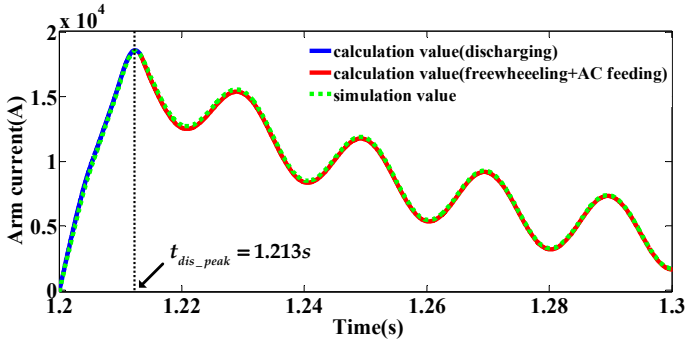


Figure 9. Simulation and calculation values of the arm current (Phase-A upper arm).

2.4. Protection Demand

The MMC-HVDC system focuses on the protection and healthy part safety of the converter station. Specifically, the IGBTs are regarded as important components in the converter station given their high cost but low electrical withstanding ability. IGBTs and freewheeling diodes are destroyed due to overheating under extremely high arm current. Another point in protection relaying is that the DCCB occupies a large portion of the cost in the HVDC project considering its high interruption capacity. Therefore, the arm and DC line currents under a fault must be investigated, and the limitation of fault current methods is required to satisfy protection demands. In accordance with the fault current analysis discussed in Section 2, the anti-parallel diodes in removed SMs and IGBTs in inserted SMs experience a dramatic overcurrent before blocking IGBTs. Moreover, the diode D_2 in inserted SMs can withstand the peak value of the discharging current when the IGBTs T_1 are blocked; this issue is considered an essential challenge to the DC fault protection of the MMC-HVDC system [4].

Considering the action of blocking IGBTs, the arm current under the DC pole-to-pole fault has been simulated (Figure 10). Using Equations (16) and (28), the DC current reaches 30 kA when the

IGBT is blocked beyond the maximum interruption capacity of 16 kA [33]. When a fault occurs, the arm current mainly consists of the capacitor discharging and AC feeding currents in the initial stage. Specifically, the SM capacitor begins to discharge the current through arms and DC loops, and the IGBTs are blocked with a triggering signal while the arm current reaches the threshold value. The IGBT blocking time is set to 1.205 s, that is, 5 ms after fault occurrence to provide a distinguishable vision on the current development; this timeframe is slightly longer than that in the real project (2–3 ms). In addition, the AC side begins to feed current into the fault current circuit while a fault occurs because the rated AC line voltage is set to more than half of the DC voltage ($V_{AC\_line} = 450$ kV, $V_{DC} = \pm 420$ kV). However, if $V_{AC\_line} < V_{DC} = 0.5U_{DC}$, then the AC feeding current will appear as $V_{AC\_line} > V_{DC}$ given the SM capacitor's discharging effect. In Figure 10, the AC feed current (red line) in the three-phase uncontrolled rectifier bridge, and the energy stored in the arm reactors begin to freewheel decayed current (blue line) through anti-parallel diodes because the IGBTs are blocked. The AC circuit breaker (ACCB) is triggered to isolate the fault section after a fault is detected. The delay in the ACCB is normally 4–5 cycles. Thus, the triggering time point is set to 100 ms after the fault occurrence. Figure 10 demonstrates that the arm current reaches approximately 10 kA while the IGBT blocks and decays slowly with the AC feeding component. The limitation of the fault current is essential to realize protection considering the limitation in the DCCB capability. The AC feeding current can be restrained using a parallel-connected thyristor in previous works [18–21]. Therefore, the discharging current limitation and rapid decaying freewheeling current are the focus in the present study.

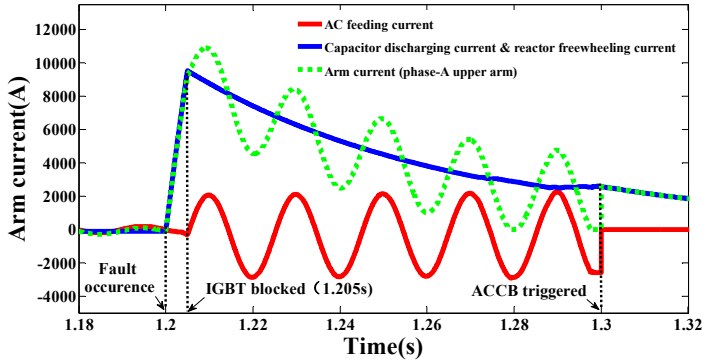


Figure 10. Phase-A upper arm current under the DC pole-to-pole fault.

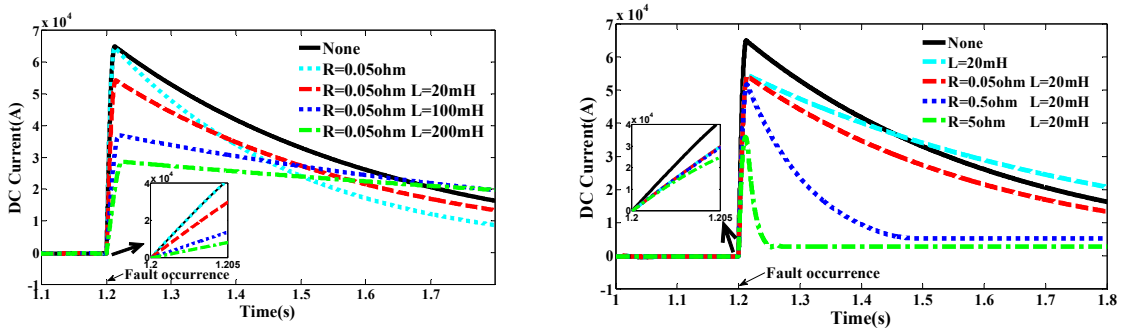
3. Enhanced Fault Current Limiting Circuit

3.1. Fault Current-Limiting Characteristics

The FCLC mainly consists of energy dissipation resistance and limiting inductance [14,15,25,35]. Thus, investigating the influence of the two elements on the fault current development is important. The related simulation was performed under controlled conditions. Figure 11a displays that limiting inductance can help slow down the accelerating speed of the fault current but increase the time spent in decaying the freewheeling current to its expected level. In Figure 11b, the energy dissipation resistance facilitates the constraining fault current peak value and the accelerating extinguishment of the freewheeling current. The adoption of the reactor and resistance in the discharging period is suitable, considering that the maximum fault current will flow through the freewheeling diode while the IGBTs are blocked or the SM capacitors are completely discharged. However, the limiting inductance can affect the dynamic response speed and prolong the recovery time. Therefore, further study on the FCLC design is required.

A series of simulations was conducted under controlled conditions to obtain the expected fault current limitation and rapid recovery. The simulation conditions are divided into resistance and reactor groups as follows: the former is labeled with "a", "b", "c", and "d", and the latter with "e", "f", "g", and "h". Specifically, the related explanations of the conditions are listed in Table 2. "✓" indicates that

the resistance or reactor is inserted in the fault circuit, and "×" denotes the absence of resistance or reactor. First, the reactor was ignored, and Figure 12a illustrates that the red curve ("ag") provides an improved performance in limiting fault current. Thus, the condition with "a" was selected for the following simulation. Figure 12b depicts the performance of various reactor-based FCLC scheme, in which the red dashed–dotted curve ("ad") represents the lowest fault current level. However, the "ad" scheme was unsatisfactory for real projects, where large inductance will affect the dynamic response speed of the entire system during the normal state. Therefore, the "af" scheme most closely approaches the optimized FCLC scheme, because the energy dissipation resistance consumes the energy in the fault circuit. This phenomenon is due to the fault being detected, and the FCL reactor being inserted to limit the increase in current speed, but also being removed to accelerate the decaying speed of the freewheeling current after blocking the IGBT.

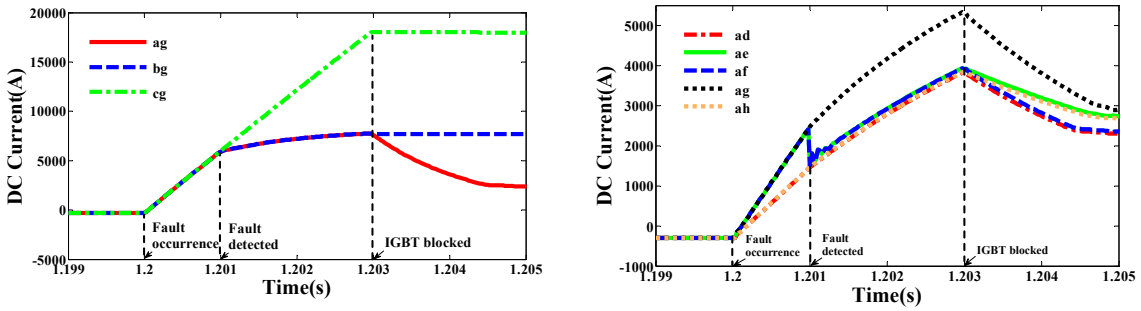


(**a**) (**b**)

Figure 11. DC fault current characteristics (**a**) with variable limiting inductance; (**b**) with variable energy dissipation resistance.

Table 2. Condition classification for the fault current limiting circuit scheme.

Time Point	Label	Fault Occurred	Fault Detected	IGBT Blocked
Resistance-related condition	a	×	✓	✓
	b	×	✓	×
	c	×	×	×
Reactor-related condition	d	✓	✓	×
	e	×	✓	✓
	f	×	✓	×
	g	×	×	×
	h	✓	✓	✓



(**a**) (**b**)

Figure 12. Comparison among different FCL schemes (**a**) different resistance conditions without considering the reactor, (**b**) different reactor conditions with selected resistance schemes.

3.2. Basic Topology

The EFCLC is proposed on the basis of analyzing the fault current limitation characteristics (Figure 13). During the normal state, the series-connected IGBTs, namely, T_1 and T_2, are opened. When a fault is detected, T_1 and T_2 are closed by a switching-off signal, and the energy dissipation resistance R_{FCL} and FCL reactor L_{FCL} are inserted in the fault circuit. L_{FCL} will be bypassed via bidirectional parallel-connected thyristors T_3 and T_4. The surge arrestor is equipped to protect circuit components from surge current and voltage. In addition, the thyristors can function as a voltage stabilizer due to the surge voltage across L_{FCL}. Considering zero voltage switching and loss reduction, the IGBTs are protected by a snubber circuit, which consists of snubber capacitor, snubber resistance, and diode [34].

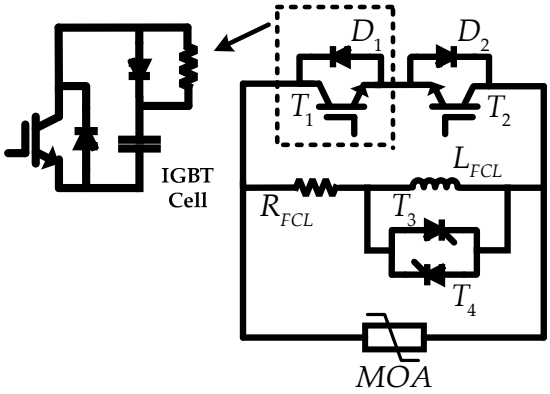


Figure 13. Proposed enhanced fault current limiting circuit.

3.3. Fault Current Interruption with DC Circuit Breaker

Considering that fault relay involves FCL behavior and DCCB operation, it is necessary to investigate the coordination between EFCLC behavior and DCCB operation in this paper. Hence, the fault interruption progress could be determined for further parameter setting of EFCLC. The DCCB topologies in articles and patents can be classified into passive and active resonance DCCB, hybrid DCCB (HCB), and solid-state DCCB (SCB) [39]. The resonance-based DCCB spend a relatively long time in fault current interruption and may lead to overcurrent. The HCB and SCB have a rapid operation speed. Although the detailed topologies of the HCB and SCB are different from the nominal path, these topologies can be equivalent to the ideal breaker in the nominal path and a metal oxide arrestor (MOA) when proactive switching control is applied [14,24]. A residential current breaker is used to cut a residential current in the MOA, which is also modeled as an ideal breaker. The topologies of the DCCB and equivalent simulation model [14] are exhibited in Figure 14a,b, correspondingly. The main breaker demonstrated in Figure 14b will wait for the operation delay in ultrafast disconnector switch (Figure 14a) operation, and the delay time is normally 2ms [33]. The fault current with a hybrid DCCB operation is exhibited in Figure 15.

Figure 16 displays the fault current interruption sequence of the EFCLC with DCCB. T_1 and T_2 are opened during the normal state, whereas T_3, T_4, and the DCCB main breaker are closed. When a fault occurs, T_1 and T_2 remain open before a fault is detected, and the main breaker of the DCCB remains closed (Figure 16a). When a fault is detected, T_1 and T_2 are switched off to insert an FCL branch in the fault circuit loop, and the DCCB main breaker remains closed due to operation time delay [33] (Figure 16b). Thus, the fault current level and accelerating speed are limited by the FCL branch, which releases the overcurrent pressure on the IGBTs and diodes in the converter and reduces the requirement of the DCCB in an interruption capacity. Once the converter is blocked under an overcurrent protection, T_3 and T_4 are switched on to bypass L_{FCL}, and the DCCB main breaker is opened (Figure 16c). Consequently, R_{FCL} shares the fault current with the MOA in the DCCB, and the fault circuit inductance is reduced to quickly extinguish the fault current. Afterward, when the current

level slightly decreases, the fault current will be cut via the residential current breaker. In addition, T_1, T_2, T_3, and T_4 are switched to their normal states.

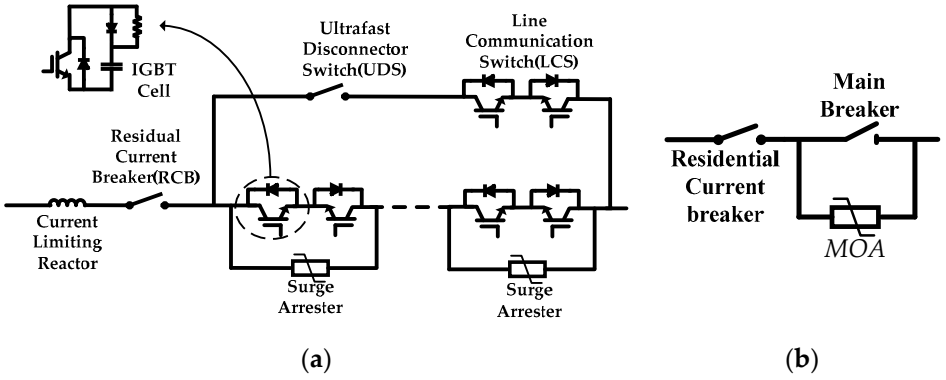


Figure 14. (**a**) Direct current circuit breaker topology, (**b**) simplified simulation model.

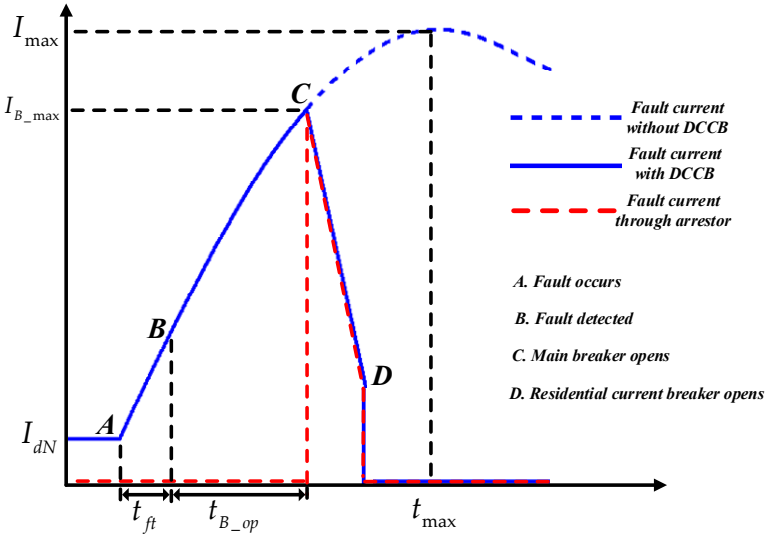


Figure 15. Fault current with hybrid DCCB operation.

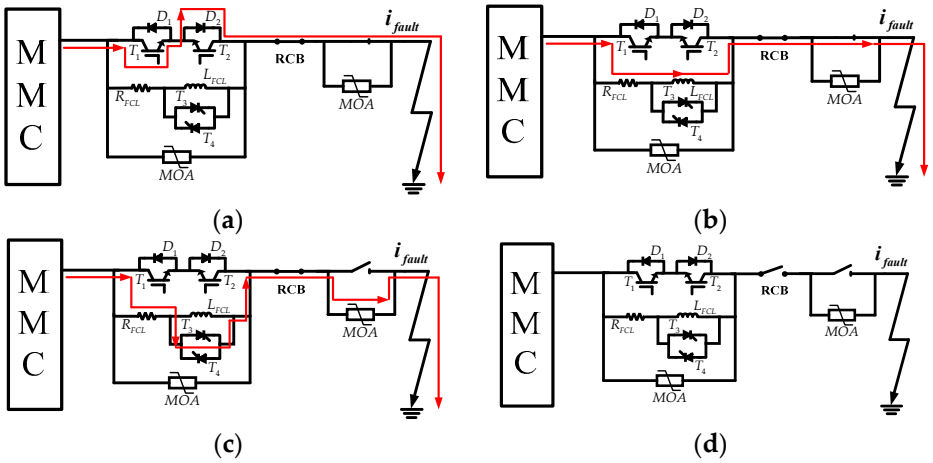


Figure 16. Sequence of fault interruption. (**a**) After fault occurrence and before fault detection, (**b**) T_1 and T_2 are switched off, (**c**) DCCB operates, T_3 and T_4 are turned on, (**d**) RCB opens, and T_3 and T_4 are turned off.

4. Design of the Enhanced Fault Current Limiting Circuit

4.1. Design Objective

The EFCLC aims to reduce the requirement for the interruption capacity and isolation speed in the DCCB. Several factors are considered to achieve the design objective.

1. The peak value of the DC line current i_{dc} must be limited under the maximum breaking current of the DCCB I_{B_max} when the main breaker opens.
2. The fault current rising speed (di_{dc}/dt) must be lower than the largest rate of the current change withstood by the DCCB ($(di/dt)_{B\_max}$).
3. In accordance with the fault current through the converter arms displayed in Figure 10, the freewheeling diodes still withstand overcurrent after blocking IGBTs. Thus, the DCCB is required to operate before the fault current reaches its maximum value. That is, the main breaker must open before the IGBT is blocked, thereby benefiting the system recovery and restart. The time period from fault occurrence to the DCCB operation (t_{op}) must be shorter than the time consumed from fault occurrence to blocking IGBTs (t_{bl}). Specifically, t_{op} involves the fault detection time $\left(t_{fd}\right)$ and DCCB operation time $\left(t_{B\_op}\right)$ (Figure 15). In accordance with the aforementioned points, the following condition can be obtained:

$$\max(i_{dc}) < I_{B\_\max} \tag{38}$$

$$\max(di_{dc}/dt) < (di/dt)_{B\_\max} \tag{39}$$

$$t_{bl} > t_{op} = t_{fd} + t_{B\_op} \tag{40}$$

4.2. Determination of Boundary Condition

Reference [33] mentioned that the hybrid DCCB has been tested to interrupt the maximum fault current of 9 kA within 2 ms. Thus, I_{B_max} is set to 9 kA in this study. The DCCB operation time t_{B_op} is set to 2 ms. Therefore, $(di/dt)_{B\_max}$ is set to 9 kA/2 ms = 4.5 kA/ms. The fault detection time under the DC fault in the HVDC system has been reduced to within 1 ms via a wavelet-based algorithm without using communication [40]. Consequently, the fault detection time t_{fd} can only be set to 1ms, and the capacitor discharging time t_{bl} must be more than 1 ms + 2 ms = 3 ms. The worst fault scenario has been adopted in this part as the PPF at the end of the DC overhead line. Furthermore, the threshold value of the arm current (I_{th}) is normally set to twice as that of the rated current (I_N) to block the IGBT. Therefore, $\mathrm{I_{th}} = 2 \times \mathrm{I_N} = 2 \times 1000\ \mathrm{A} = 2000\ \mathrm{A}$ with I_N is set to 1000 A in this study.

The capacitor discharging current is defined in Equation (9) on the basis of the fault current analysis discussed in Section 2. The contributions from the AC grid and distributed line capacitance are omitted here. According to Constraint (38), the time during fault detection and main breaker operation delay is 3 ms.

$$\max(\mathrm{i_{dc}}) = \mathrm{i_{dis}(t)}\big|_{\mathrm{t=3\ ms}} < \mathrm{I_{B\_max}} = 9\ \mathrm{kA} \tag{41}$$

The change rate in the DC fault current can be obtained using Equation (42); the change rate must be less than 4.5 kA/ms.

$$\max(\mathrm{di_{dc}/dt}) = \max(\mathrm{i_{dis}(t)'}) < 4.5\mathrm{kA/ms} \tag{42}$$

In reference to Equations (35) and (36), Constraint (40) must be considered to decrease the arm current at 3 ms less than the threshold value of blocking the IGBT after fault occurrence.

$$\mathrm{i_{arm}(t)}\big|_{\mathrm{t=3ms}} < \mathrm{I_{th}} = 2\mathrm{kA} \tag{43}$$

Equations (35)–(37) express that the equivalent capacitance and inductance determine the fault current development and capacitor discharging time. Moreover, the fault current curve must be

separated into two stages using the proposed EFCLC (Figure 12b). Specifically, the fault current rising speed is higher in the first 1 ms stage than in the rest time. Thus, the fault current change rate within the first 1 ms must be limited by Constraint (42). Furthermore, the fault current value at 3 ms after fault occurrence must be obtained by superposing the fault current calculation in two discharging stages. Therefore, varying the fault circuit parameters, which are similarly considered in determining the capacitor discharging time, must be addressed.

4.3. Parametric Design

Before the EFCLC is inserted in the fault circuit loop, the fault current is only limited via the smoothing reactor, which decides the maximum increase in the fault current rate. The minimum smoothing reactor can be obtained using Equation (9) considering the limitations in the DCCB withstanding fault current change rate (4.5 kA). The theoretical minimum smoothing reactor is 41.2 mH. However, the simulation result provides 43 mH with 4.2% error. The reason may be attributed to the consideration of DC line current under the normal states. The smoothing reactor L_{dc} is set to 50 mH considering the margin. The EFCLC will be inserted to limit fault current rising speed and amplitude after detecting a fault. Thus, the fault current rising speed is less than the fault detection time; thus, Constraint (39) is satisfied by properly selecting a smoothing reactor.

An initial test with the EFCLC has been performed. The energy dissipation resistance R_{FCL} is set to 50 Ω, and the FCL reactor L_{FCL} is set to 100 mH. The simulation conditions "af" and "ah," as listed in Table 2, are compared here. The red dashed line in Figure 17 indicates that a fault occurs at 1.2 s and takes 1 ms to detect fault [37]. Furthermore, the delay in the IGBT of the EFCLC is disregarded here. The fault current change rate during Δt_1 is approximately 4 kA/ms, which is expectedly limited under the maximum current change rate of the hybrid DCCB. The EFCLC is inserted in the fault current circuit at 1.201 s, and the fault current experiences a sharp decrease ΔI_1 because a part of the electrical energy is stored in L_{FCL}. The fault current rising speed is lower during Δt_2 than during Δt_1. Therefore, the fault current at 1.203 s (the main breaker opens) is limited to approximately 6.6 kA, which is far below the maximum breaking current of the DCCB. Moreover, L_{FCL} is bypassed by the thyristor while the main breaker opens, and the fault current extinguishment can be accelerated. The initial simulation result suggests that Constraint (41) leads to the minimum value of L_{FCL} and R_{FCL}. Therefore, the controlled match of L_{FCL} and R_{FCL} must be investigated. The fault current at 1.201 s is consistently 4 kA given the unchanged fault circuit parameter. Therefore, Figure 17 presents that

$$4kA - \Delta I_1 + \Delta I_2 < 9kA \tag{44}$$

In comparison with the blue dashed-dotted line illustrated in Figure 17, two current curves share nearly the same part during Δt_2. Thus, ΔI_1 can be obtained with a difference between the current values of the two discharging conditions. In accordance with Equation (9), ΔI_1 is expressed as Equation (45).

$$\Delta I_1 = i_{dis\_af}(t)\big|_{t=1ms} - i_{dis\_ah}(t)\big|_{t=1ms} \tag{45}$$

Moreover, Equations (44) and (38) can be simplified as Equation (46), because the two current curves depicted in Figure 17 have nearly the same value at 1.203 s.

$$i_{dis\_ah}(t)\big|_{t=3ms} < 9kA \tag{46}$$

The equivalent resistance R_{eq_ah} and equivalent inductance L_{eq_ah} are acquired as Equations (47) and (48), respectively. Thus, on the basis of Equation (9), the fault current i_{dis_ah} at 1.203 s can be calculated. If $R_{FCL} = 20\ \Omega$, then L_{FCL} must be larger than 46.4 mH to limit the fault current at 1.203 s under 9 kA. The minimum L_{FCL} matched with $R_{FCL} = 20\ \Omega$ has been verified via a controlled simulation (Figure 18). The simulation results of the EFCLC with controlled R_{FCL} and different L_{FCL} are compared (Figure 18). The fault current with the EFCLC (calculated $L_{FCL\_min} = 46.4$ mH with $R_{FCL\_min} = 20\ \Omega$)

reaches 9106 A at 1.203 s. Thus, the error rate of the theoretical calculation is approximately 1.2% within a reasonable range, and the minimum L_{FCL} can be set to 47mH. Constraint (43) can be analyzed using the arm current Equations (24) and (25) in Section 2. Setting $R_{FCL} = 20\ \Omega$, the L_{FCL_min} is calculated as 219 mH to satisfy Constraint (43). The arm currents are compared under the calculated L_{FCL_min} and L_{FCL_min} obtained via a simulation (Table 3). The calculated L_{FCL_min} leads to the maximum arm current (2023.5 A), which can contribute to blocking the IGBTs. The error in the calculation method may be attributed to the circulating current among arms. However, the simulation method provides expected results; that is, the currents of the six arms are all limited under 2 kA at 1.203 s. Therefore, in the overall view of constrains, L_{FCL_min} is approximately 225 mH when R_{FCL} is set to 20 Ω. However, L_{FCL_min} is selected as 250 mH with $R_{FCL} = 20\ \Omega$ considering the margin in the parameter setting.

$$R_{eq\_ah} = R_{fault} + 2R_{dc} + R_{FCL} \tag{47}$$

$$L_{eq\_ah} = \frac{2}{3}L_0 + 2L_{dc} + L_{FCL} \tag{48}$$

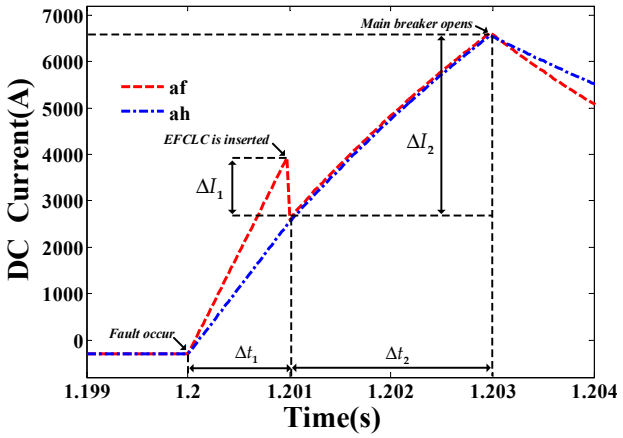


Figure 17. Simulation results of the DC line current with the EFCLC.

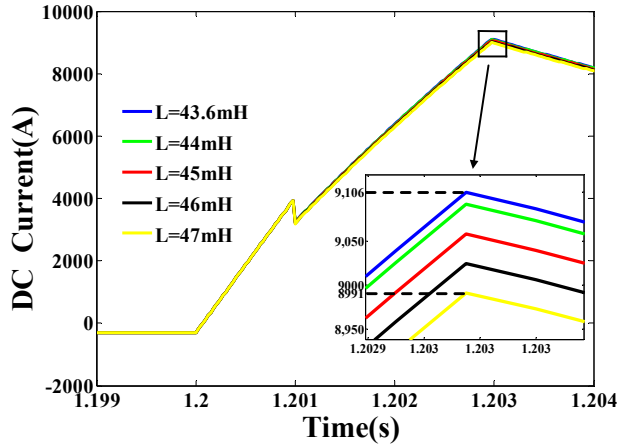


Figure 18. Simulation results of the controlled R_{FCL} and different L_{FCL}.

Table 3. Arm currents under the calculated and simulated L_{FCL_min}.

L_{FCL} = 219 mH, R_{FCL} = 20 Ω		L_{FCL} = 225 mH, R_{FCL} = 20 Ω	
Phase-A upper arm current	1712.7 A	Phase-A upper arm current	1668.3 A
Phase-A lower arm current	2023.4 A	Phase-A lower arm current	1999.2 A
Phase-B upper arm current	2023.5 A	Phase-B upper arm current	1999.1 A
Phase-B lower arm current	1704.4 A	Phase-B lower arm current	1680.2 A
Phase-C upper arm current	1876.5 A	Phase-C upper arm current	1834.3 A
Phase-C lower arm current	1858.7 A	Phase-C lower arm current	1852.3 A

5. Discussion

Several existing FCL schemes were compared in terms of FCL ability, cost, power loss, and influence on recovery and restart operations. The energy dissipation resistance-based FCL method in Reference [14], the inductance-based FCL scheme [15,35], and the proposed EFCLC were simulated under controlled conditions in this section.

5.1. Fault Current-Limiting Ability Comparison

To investigate the FCL ability, the bias voltage adopted in the scheme presented in Reference [15] is omitted for convenience, and the values of the FCL reactor and energy dissipation resistance are maintained in comparison with the FCL ability (R_{FCL} = 20 Ω, L_{FCL} = 250 mH). In accordance with the FCL method in Reference [21], the AC feeding current can be limited via a parallel-connected thyristor, and the FCL ability is compared on the basis of the capacitor discharging current in the present study. Therefore, the AC feeding current is eliminated by switching off the start connector in the simulation while the DCCB operates. The simulation results of the arm and DC line currents with different FCL schemes are compared, as exhibited in Figure 19. The arm current with the resistance-based method (R-method) is limited to approximately 6 kA (Figure 19a). The arm currents with inductance-based method (I-method) and proposed scheme are restricted under 2 kA (Figure 19c,e, respectively). The proposed method can accelerate the fault current decay while the main breaker opens. Thus, the freewheeling diodes and IGBTs can be protected from overcurrent for a long time, and the fault current isolation speed is shortened. The R-method has the worst FCL performance, thereby limiting the DC line current to approximately 18 kA (Figure 19b). By contrast, the I-method and the proposed method can restrain the DC line current under 5.5 kA (Figure 19d,f, correspondingly). However, the DC line current with the I-method remains at a high level after the main breaker opens. In summary, the proposed scheme has an improved performance in limiting the fault current through converter arms and DC line.

5.2. Cost

The main cost of the proposed EFCLC lies in fault current-limiting inductance L_{FCL}, energy dissipation resistance R_{FCL}, semiconductor switches, and surge arrester. Similar to the main breaker in the hybrid DCCB, the number of IGBT depends on the voltage across the EFCLC. The amount and parameter selection of a surge arrester are also determined by protection requirement. The EFCLC can be regarded as an auxiliary circuit to share the energy absorption and electrical pressure by limiting the fault current under an acceptable level. Although IGBTs and surge arrester in EFCLC lead to extra cost, the HVDC system can ensure the fault interruption with a low risk on the DCCB failure. Moreover, according to the simulation result in Figure 19, the R-method adopted in References [14,41] has a higher fault current level than the proposed method during the fault interruption period, thereby indicating extra cost on interruption capacity, surge arrester, and the cooling system. Therefore, it might be economic to have EFCLC in protection operation, given its strength in FCL ability. Furthermore, lower peak fault current indicates less investment in DCCB interruption capability. The main expenditure of the I-method depends on the SFCL inductance technology because its unique characteristics can limit the fault current without affecting the system's dynamic response speed. However, the immaturity of

the SFCL device leads to an increased cost to satisfy the protection requirement in terms of the system recovery and restart. Furthermore, compared with the proposed approach, the I-method requires additional cost in the energy dissipation component to accelerate the fault current extinguishment. In summary, taking comprehensive consideration of economic efficiency and FCL performance, EFCLC deserves consideration to be applied in real project.

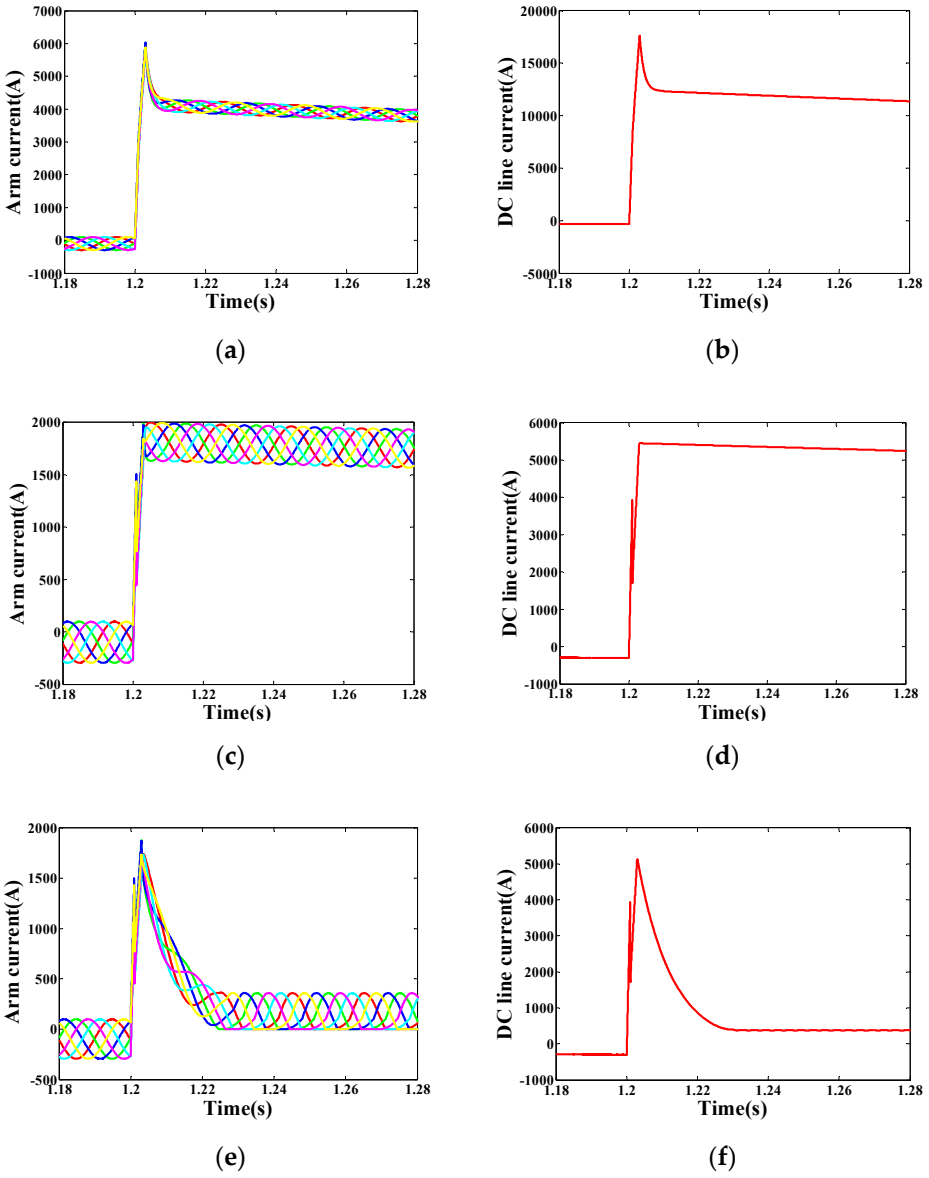


Figure 19. FCL ability comparison among existing methods: (**a**) Arm current in the resistance-based method, (**b**) DC line current in the resistance-based, (**c**) Arm current in the inductance-based method, (**d**) DC line current in the inductance-based method, (**e**) Arm current in the proposed method, (**f**) DC line current in the proposed method.

5.3. Power Loss

As explained in Section 4.3, the proposed scheme requires a smoothing reactor of 50 mH, thereby leading to power loss during the normal state. Considering that the resistance value of a 2 mH reactor equals 18.9 mΩ [42], the power loss P_L is expressed as Equation (49).

$$P_L = \frac{4I_{dN}^2 R_L L_r}{P_{cableN}} \times 100\% \tag{49}$$

where I_{dN} is the rated DC line current, $R_L = 0.00945\,\Omega/\text{mH}$ is based on Reference [43], L_r is the smoothing reactor, and P_{cablrN} is the rated DC line power. Thus, the smoothing reactor in the proposed scheme causes 0.135% power loss in comparison with the rated DC line power, thus denoting a promising economic efficiency.

5.4. Influence on Fault Current

Figure 20a,b presents the influence of R_{FCL} and L_{FCL} on the DC line current, respectively. When R_{FCL} increases but L_{FCL} remains at 250 mH, the DCCB capability requirement is low, and the fault current extinguishment is accelerated (Figure 20a). When L_{FCL} increases but R_{FCL} remains at 20 Ω, the peak value of the fault current decreases but the time spent in the fault current interruption is unaffected. Therefore, L_{FCL} in the proposed scheme hardly influences the dynamic response or the fault current extinguishment.

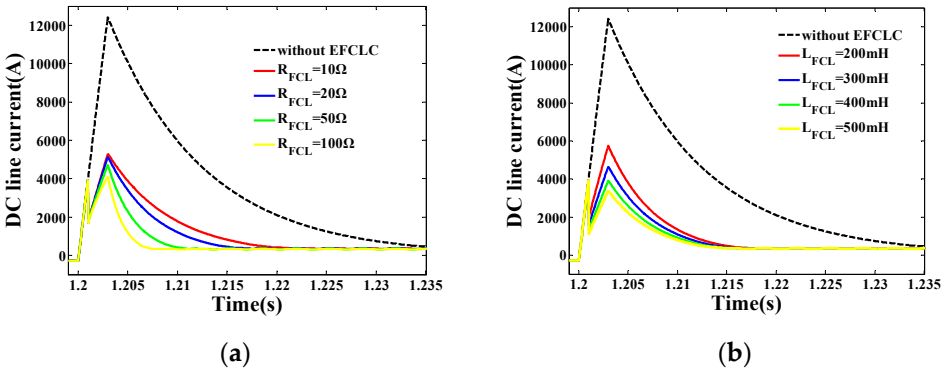


Figure 20. DC line current with variables (**a**) R_{FCL} and (**b**) L_{FCL}.

5.5. Influence on Energy Absorption

Because of the isolation effect of the thyristor on the AC feeding current, the fault current during fault interruption is mainly the freewheeling current, given the energy stored in the smoothing reactor, whose path is depicted in Figure 21. The energy stored in the smoothing reactor can be obtained using Equation (50).

$$E_L = 1/2 L_{dc} i_{fault}^2(t_{op}) \tag{50}$$

where L_{dc} is the smoothing reactor; $i_{fault}(t_{op})$ is the fault current through the DC line while the DCCB operates, which can be obtained using Equation (9); and t_0 is the time point of fault occurrences.

$$i_{fault}(t_{op}) = e^{-\frac{t_{op}-t_0}{\tau}}\left[U_{dc}\sqrt{\frac{C_{eq}}{L_{eq}}}\sin(\omega_1(t_{op}-t_0)) - \frac{I_{dis0}\omega_0}{\omega_1}\sin(\omega_1(t_{op}-t_0)-\theta)\right] \tag{51}$$

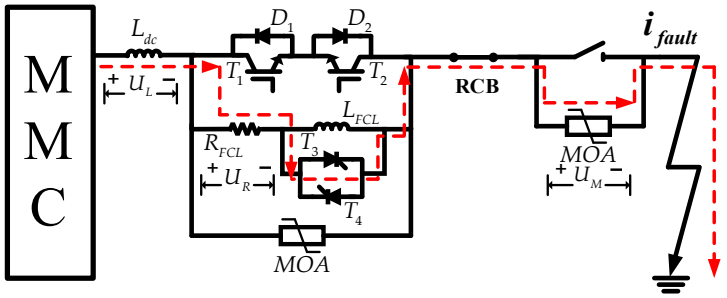


Figure 21. Fault current path during fault interruption.

The energy absorbed by R_{FCL} can be expressed as

$$E_R = \int (U_R^2 / R_{FCL}) dt = \int ((R_{FCL} i_{fault})^2 / R_{FCL}) dt \quad (52)$$

Then, the energy absorbed in the MOA of the DCCB can be expressed as

$$E_M = E_L - E_R \quad (53)$$

Figure 20b displays that a large smoothing reactor will lead to a small $i_{fault}(t_{op})$. Thus, the energy stored in the smoothing reactor will decrease, thereby indicating a reduced energy consumed in the MOA and decreased time spent in the fault current interruption. Moreover, the fault detection time can influence the energy stored in the smoothing reactor in a positive relationship. Thus, determining the energy absorbed in R_{FCL} must consider the effect of inductance and fault detection time to reduce stress on the MOA of the DCCB. The simulation result presented in Figure 22a shows that a large R_{FCL} results in minimal energy absorption in the MOA of the DCCB given the low fault current level at the DCCB operation time point and shared energy absorption. Similarly, a large L_{FCL} denotes a minimal energy absorbed in the MOA because an increase in L_{FCL} leads to a low current and energy stored in L_{dc} when the main breaker opens. Overall, R_{FCL} and L_{FCL} can limit the fault current to a relatively low level to reduce the energy absorbed in the MOA of the DCCB. However, a balance between the DCCB and EFCLC is observed in terms of energy consumption during the fault current-limiting period and fault current extinguishment stage. Therefore, the tradeoff between FCL performance and additional cost on the snubber circuit and cooling system of the EFCLC must be considered.

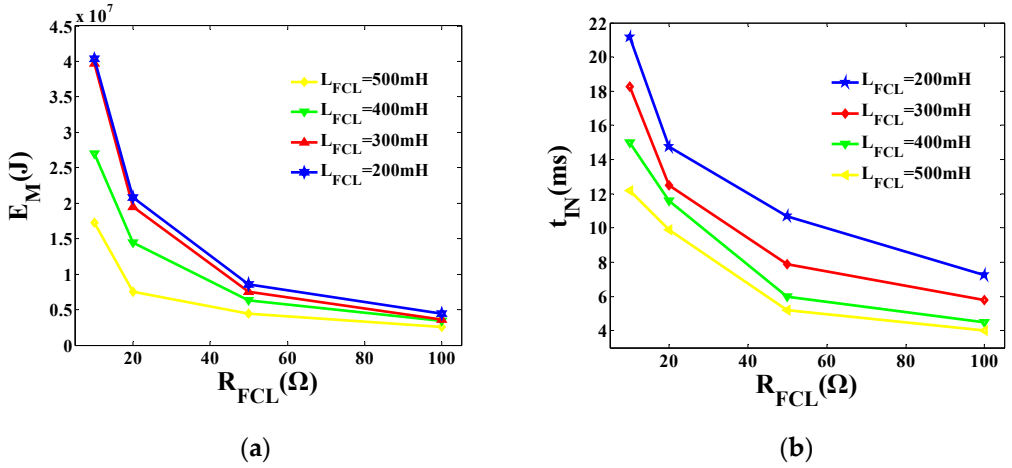


Figure 22. Characteristic curves of absorbed energy and interruption time under variables (**a**) R_{FCL} and (**b**) L_{FCL}.

5.6. Influence on Fault Interruption Time

Although L_{FCL} is involved in the EFCLC, it can still be bypassed by the thyristor after the main breaker operates. Thus, the fault current extinguishment speed cannot be delayed due to large inductance. As mentioned in Section 5.5, the fault current level is restricted by a large R_{FCL} and L_{FCL}, and the interruption time can be reduced at a low fault current level at the beginning of fault extinguishment. According to the expression of the attenuation coefficient during the fault interruption expressed in Equation (37), the large R_{FCL} can accelerate extinguishment speed. In summary, the interruption time is reduced when the values of R_{FCL} and L_{FCL} are high. This result agrees with the simulation result demonstrated in Figure 22b.

5.7. Practicality and Necessity of Proposed Circuit

According to the study in this section, the proposed FCL circuit has better performance in limiting fault current under DC pole-to-pole fault, compared with previous FCL method under same parameter setting. In the viewpoint of reality, the power loss during normal state is considered acceptable as analyzed in Section 5.3. In order to cooperate with protection relaying, the proposed FCL circuit is installed at the ends of transmission line so that communication delay among DCCB, measure point and protection relay could be reduced. Moreover, big smoothing reactor (200 mH) in [42–44] would influence the dynamic response speed and proposed FCL circuit could help reduce value of smoothing reactor for better performance of dynamic response. However, it requires further investigation on economic efficiency of proposed method, considering previous FCL methods, such as superconductor based fault current limiter, FCL circuit and converter topology based approach.

Another point should be noted that the proposed EFCLC would make more contribution to fault interruption and clearance, compared with traditional FCL behavior with DC terminal reactor. The basic advantage of EFCLC over DC terminal reactor could be summarized as following aspects. Firstly, EFCLC is only triggered as fault detected to limit fault current, thereby having no influence on normal state and system dynamic response. By contrast, to achieve the same level of FCL performance of EFCLC, larger DC terminal reactor is required even under normal state, which does affect system dynamic response. Seconded, compared with DC terminal reactor, EFCLC could accelerate fault clearing speed due to its energy dissipation resistor. The last but not the least, the FCL inductor in EFCLC would be bypassed after IGBT blocks. Hence, the fault isolation time would be reduced to some degree since remained inductor would delay the fault current clearance.

5.8. Effectiveness of the Proposed Circuit

With application of the proposed EFCLC in fault loop, the requirement of DCCB's interruption ability is reduced, and fault current interruption speed is accelerated. A comparison is performed in Table 4 between a fault situation with EFCLC and that without EFCLC, in terms of maximum fault current and fault interruption time. As mentioned in Section 4.3, L_{FCL_min} and R_{FCL} are set as 250 mH and 20 Ω in the test circuit. The test results shown in Table 3 reflect that the peak fault current needed to interrupt at DCCB operation is reduced from 12.4 kA to 5.1 kA with the help of EFCLC. Meanwhile, the time taken for the whole fault interruption process decreases from 34.8 ms to 13.6 ms. In summary, the effectiveness of the proposed circuit is verified, and reduced peak fault current and accelerated fault interruption would contribute to lower cost in relay and fast fault clearance.

Table 4. Effectiveness verification of enhance fault current limiting circuit.

Term	Requirement of Fault Current Interruption	Fault Interruption Time
Without EFCLC	12.4 kA	34.8 ms
With EFCLC	5.1 kA	13.6 ms
Improvement	41.1%	39.1%

6. Conclusions

An EFCLC has been proposed and investigated in this study to reduce the DCCB requirement in terms of fault interruption capability and breaking speed. The EFCLC mainly consists of the energy dissipation resistor and FCL reactor. These devices are plugged into the fault loop after fault detection to limit the fault current rising speed and fault current level. Thus, while the DCCB operates, the fault current level is restrained, and the energy stored in the smoothing reactor is also reduced. Consequently, the fault current extinguishment stage can be accelerated given the increased energy dissipation resistor and decreased energy storage. Furthermore, the FCL reactor can be bypassed to accelerate the decaying of the freewheeling current. Moreover, the AC feeding current is eliminated via the bidirectional parallel-connected thyristor, whose feasibility and effectiveness have been verified in

existing works. Thus, this study focused on the methods for limiting fault current caused by capacitor discharging in the FCLC design. The proposed EFCLC has been verified to limit fault current under an expected level with a proper parameter setting on components. However, the performance tradeoff and additional cost of the EFCLC must be considered in terms of the cooling system, surge arrester, and overvoltage protection. The development of the EFCLC in the multi-terminal HVDC system, the related fault protection scheme, and the FRT strategy will be investigated in future research.

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