

Supplementary Information

From chip size to wafer-scale nanoporous gold reliable fabrication using low currents electrochemical etching

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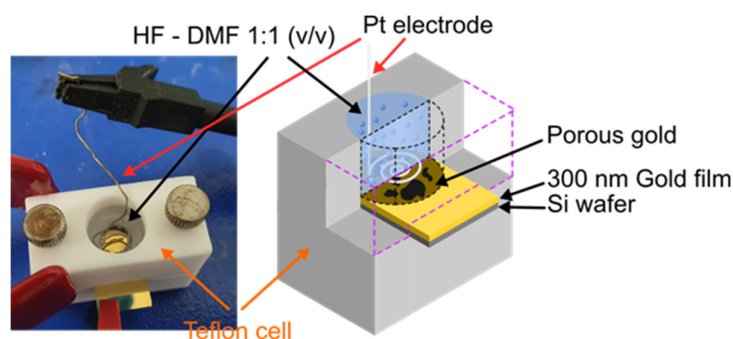


Figure S1. Experimental setup for nanoporous gold fabrication; schematic representation of the NPG etching system – cross-sectional view.

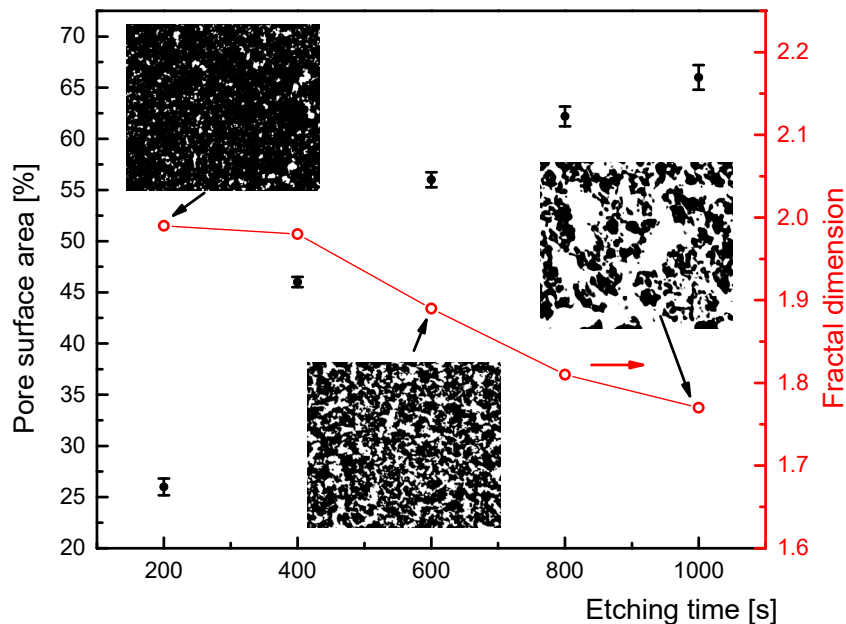


Figure S2. The calculated average gold solid area (from SEM micrographs) for different etching time durations and the binarized images (insets), which were used Figure 3. (a) 4 inch NPG on Si fabrication using AMMT system; (b) Photography of the resulted on wafer NPG film in comparison with the one obtained using microcell. Insets represents SEM top views of NPG in two distinct regions of the wafer.

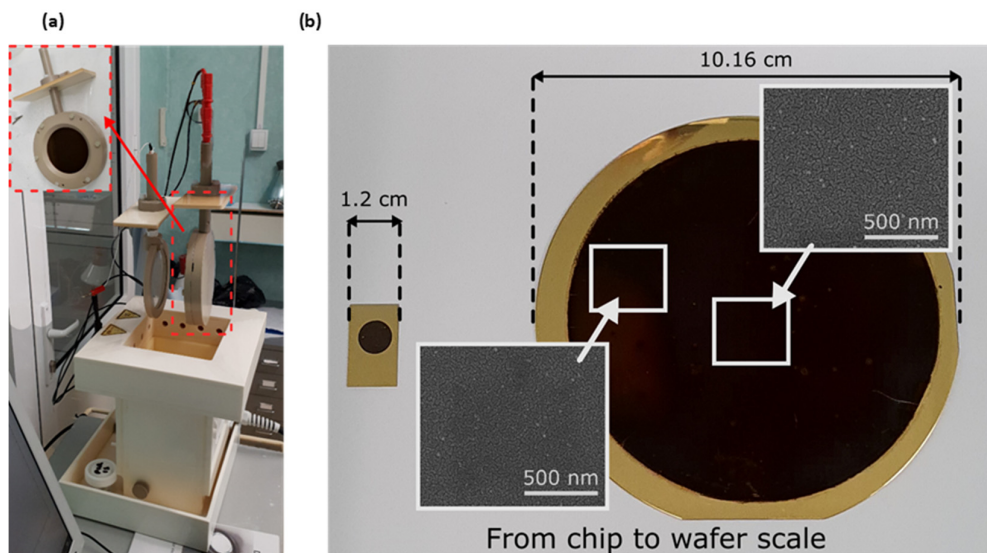


Figure S3. (a) 4 inch NPG on Si fabrication using AMMT system; (b) Photography of the resulted on wafer NPG film in comparison with the one obtained using microcell. Insets represents SEM top views of NPG in two distinct regions of the wafer.

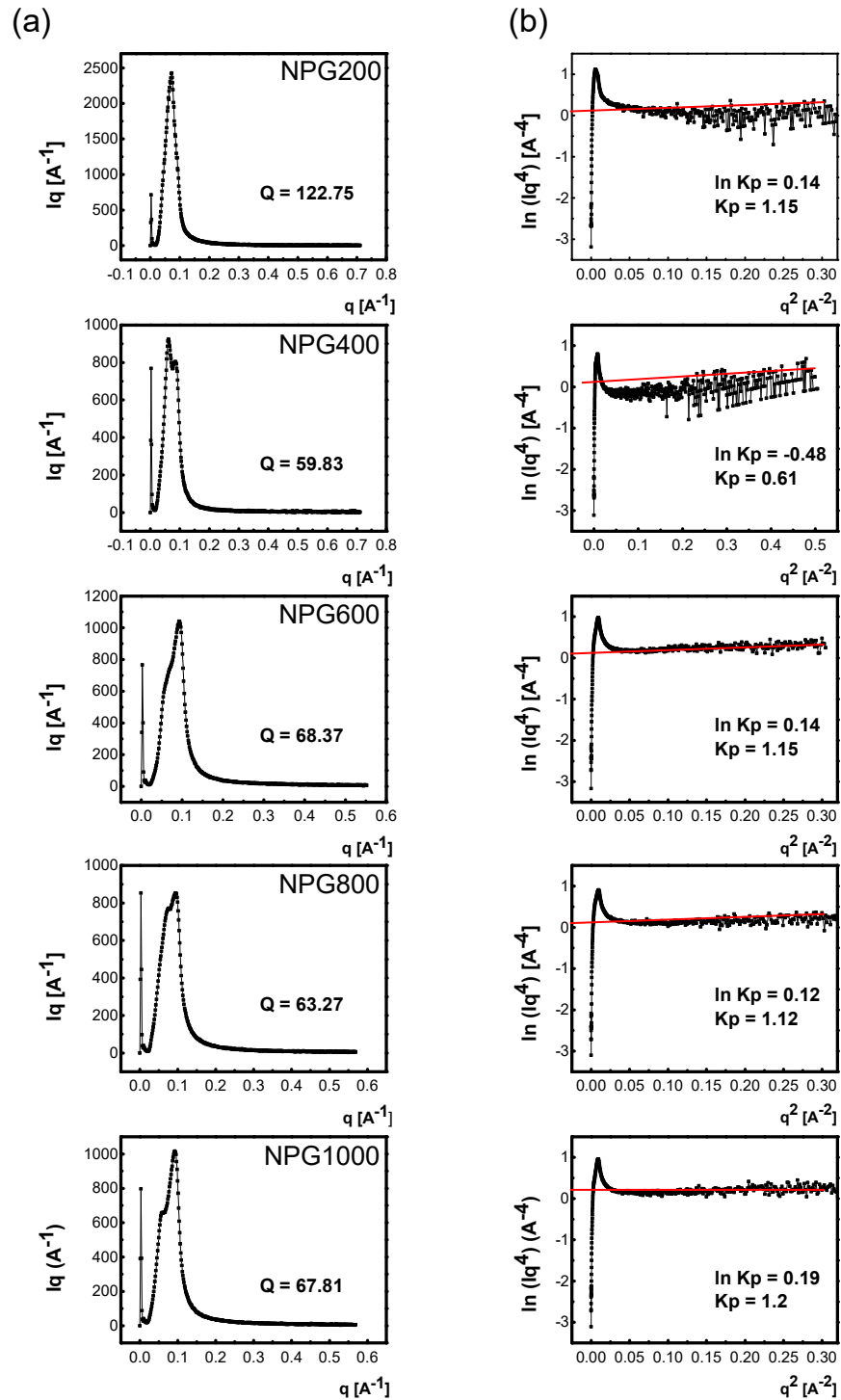


Figure S4: Iq vs. q and $\ln(Iq^4)$ vs. q^2 dependences for the: (a) Porod integral and (b) Porod constant.