



Article

Exceedingly High Performance Top-Gate P-Type SnO Thin Film Transistor with a Nanometer Scale Channel Layer

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Abstract: Implementing high-performance n- and p-type thin-film transistors (TFTs) for monolithic three-dimensional (3D) integrated circuit (IC) and low-DC-power display is crucial. To achieve these goals, a top-gate transistor is preferred to a conventional bottom-gate structure. However, achieving high-performance top-gate p-TFT with good hole field-effect mobility (μ_{FE}) and large on-current/off-current (I_{ON}/I_{OFF}) is challenging. In this report, coplanar top-gate nanosheet SnO p-TFT with high μ_{FE} of $4.4 \text{ cm}^2/\text{Vs}$, large I_{ON}/I_{OFF} of 1.2×10^5 , and sharp transistor's turn-on subthreshold slopes (SS) of 526 mV/decade were achieved simultaneously. Secondary ion mass spectrometry analysis revealed that the excellent device integrity was strongly related to process temperature, because the HfO_2/SnO interface and related μ_{FE} were degraded by Sn and Hf inter-diffusion at an elevated temperature due to weak Sn–O bond enthalpy. Oxygen content during process is also crucial because the hole-conductive p-type SnO channel is oxidized into oxygen-rich n-type SnO_2 to demote the device performance. The hole μ_{FE} , I_{ON}/I_{OFF} , and SS values obtained in this study are the best-reported data to date for top-gate p-TFT device, thus facilitating the development of monolithic 3D ICs on the backend dielectric of IC chips.



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1. Introduction

Metal-oxide Thin film transistors (TFTs) [1–35] have drawn considerable attention due to their high mobility, low fabrication temperature, and simple fabrication process, making them suitable for advanced display [1–6] and monolithic three-dimensional (3D) integrated circuit (IC) [15–21] on amorphous inter-metal-dielectric (IMD) of a Si chip. To reach low DC power consumption, both high performance n- and p-type TFTs are necessary to form the complementary metal-oxide-semiconductor (CMOS) logic. Although high-performance n-TFTs with high field-effect mobility (μ_{FE}), sharp subthreshold swing (SS), and large on-current/off-current (I_{ON}/I_{OFF}) values [12–15] have been reported, achieving reasonable performance p-TFTs is much more challenging [16,17,36,37]. Moreover, a top-gate structure is more suitable than a conventional bottom-gate device for high integration density and easy fabrication [24–26]. Previously, we have reported the bottom-gate SnO p-TFT, which has higher μ_{FE} than Cu_2O p-TFT [16,17]. In the current study, we further used the SnO channel to fabricate top-gate coplanar nanosheet p-TFT. Because the gate insulator was deposited after the SnO layer, the deposition and post-annealing conditions are crucial to device performance. This is because the p-type SnO is highly sensitive to oxygen partial pressure (O_{pp}) and annealing temperature, and can be easily oxidized into oxygen-rich Sn_2O_3 , Sn_3O_4 , or SnO_2 [27–29]. Moreover, the weak Sn–O bond enthalpy [38] facilitates Sn diffusion into high-dielectric-constant (high- κ) HfO_2 insulator at elevated temperature,

thus degrading device performance. In this study, the above challenges were successfully overcome, and high-performance top-gate nanosheet SnO p-TFT was achieved with high μ_{FE} of $4.4 \text{ cm}^2/\text{Vs}$, large I_{ON}/I_{OFF} of 1.2×10^5 , and sharp SS of 526 mV/decade, indicating a high potential for future monolithic 3D and brain-mimicking IC applications [15,17–21].

2. Materials and Methods

The coplanar top-gate nanosheet SnO p-TFTs were fabricated on the Si wafer with a 500-nm-thick SiO_2 IMD layer on Si wafer. The 7-nm-thick nanosheet SnO layer was deposited through reactive sputtering with 50 W DC power from a Sn target under O_{pp} values of 14.2%, 25%, and 33.3% ambient, respectively. All the SnO p-TFT samples were annealed under 200 °C in N_2 ambient for 45 min. Next, 40-nm high work-function Ni was deposited using an e-gun evaporator for the Schottky-barrier source and drain electrodes [39,40]. Subsequently, 50-nm HfO_2 gate dielectric was deposited by e-beam evaporation with a rate of 0.2 Å/sec. HfO_2 post-annealing was performed in N_2 ambient at 100 °C and 200 °C. Finally, 50-nm gate electrode Al was deposited and patterned. The transistor's length and width were 50 and 400 μm , respectively. The current-voltage characteristics of top-gate SnO p-TFT were measured through the HP4155B parameter analyzer and a probe station. The field-effect mobility values (μ_{FE}), subthreshold slope (SS) and on-current/off-current (I_{ON}/I_{OFF}) values were extracted at a standard and small $V_{DS} = -0.1 \text{ V}$. The cross-sectional image of device structure was obtained from FEI Talos F200X high-resolution transmission electron microscope (TEM). The surface roughness of HfO_2 films were obtained via Atomic Force Microscope (AFM) using DIMENSION 3100. The X-ray photoelectron spectroscopy (XPS) analyses of HfO_2 films and SnO films were executed by Thermo Nexsa. The secondary ion mass spectrometry (SIMS) depth profiles of Sn, Hf and O atoms were obtained by CAMECA IMS-6fE7.

3. Results

Figure 1a illustrates the top-view photograph of top-gate nanosheet SnO p-TFT, where the light-reflective Al metal-gate is on the top of the device. Figure 1b depicts the cross-sectional transmission electron microscope (TEM) image of the device structure with top Al-metal-gate, HfO_2 gate-dielectric, and p-type channel SnO on SiO_2 IMD. The thickness of Al, HfO_2 , and nanosheet SnO is 50, 50, and 7 nm, respectively.

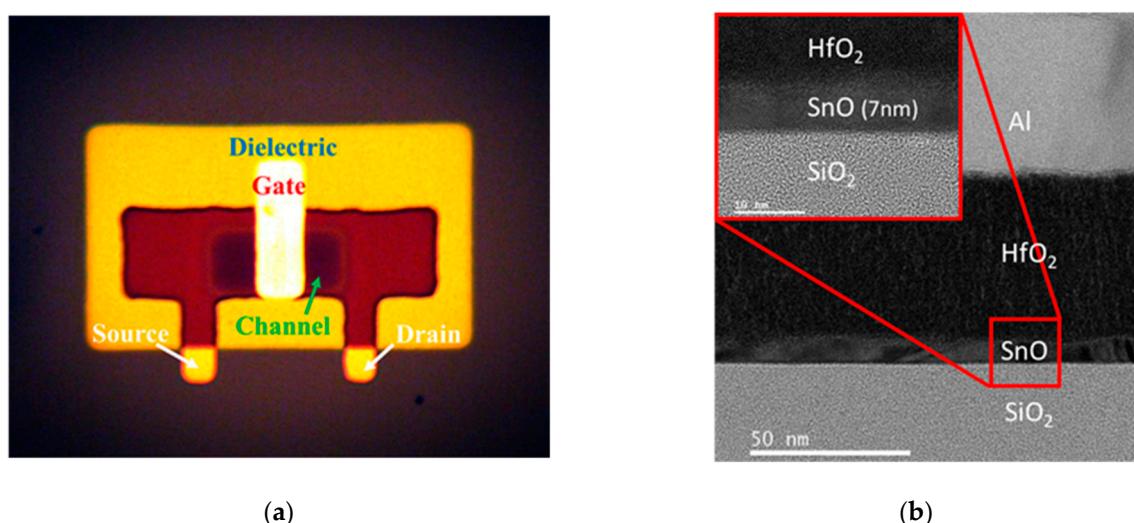


Figure 1. (a) top-view photograph and (b) cross-sectional TEM image of the top-gate nanosheet SnO p-TFT device. The “white”-color gate on top of the device is due to the light-reflective Al metal.

The O_{pp} is critical for top-gate nanosheet SnO p-TFT, where the SnO channel was made by sputtering from a metal Sn target under different O_{pp} conditions. This is because the SnO can be oxidized into oxygen-rich SnO_2 [16]. The O_{pp} can be expressed as follows:

$$O_{pp} = \frac{P_{O_2}}{P_{O_2} + P_{Ar}} \times 100\%, \quad (1)$$

where P_{O_2} and P_{Ar} are the pressures of O_2 and Ar in a sputtering system, respectively. For comparison, the O_{pp} values were adjusted to 14.2%, 25% and 33.3% during sputtering. Figure 2a,b show the drain-source current versus gate-source voltage ($|I_{DS}| - V_{GS}$) and μ_{FE} - V_{GS} characteristics of top-gate nanosheet SnO p-TFT devices, respectively, under different O_{pp} values. The top-gate p-type SnO device exhibits the highest I_{ON} and the lowest leakage I_{OFF} at the 25% O_{pp} condition. The device with the best I_{ON} and I_{OFF} is also consistent with the highest μ_{FE} . The μ_{FE} values were 1.5, 4.4 and $2.6 \text{ cm}^2/\text{Vs}$ at O_{pp} of 14.2%, 25% and 33.3%, respectively. Here the μ_{FE} values were obtained at the standard and a small V_{DS} of -0.1 V . Such abnormal μ_{FE} on O_{pp} is ascribed to the following reasons. The device μ_{FE} increases with the increase in O_{pp} from 14.2% to 25% due to the increased oxygen content in SnO_x , with $x \leq 1$, and device performance degrades at a high O_{pp} of 33.3% owing to the formation of oxygen-rich SnO_x , with $x > 1$. Under high O_{pp} , SnO_x becomes n-type electron-conductive SnO_2 [12–14], which lowers the hole μ_{FE} under negative V_{GS} .

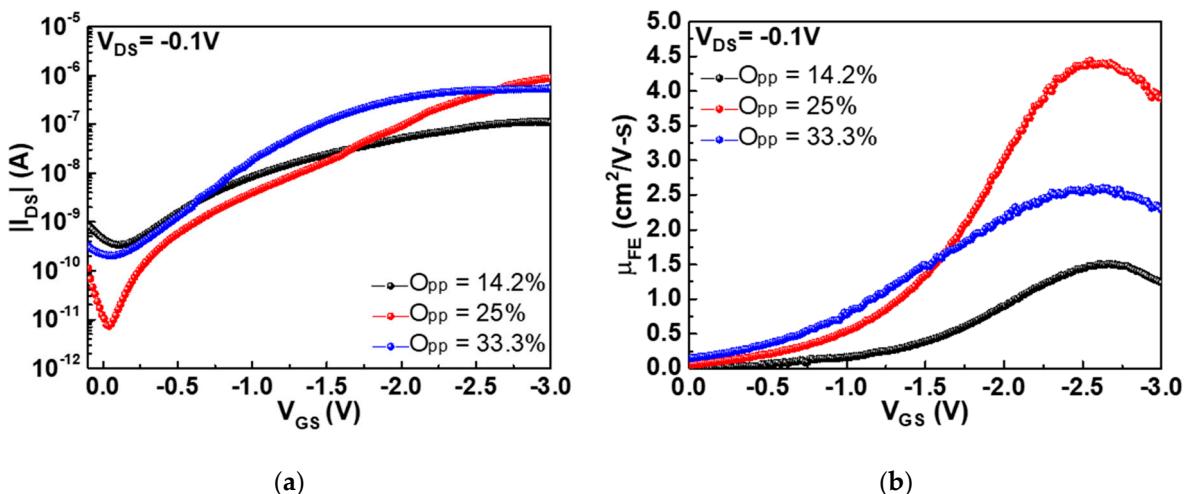


Figure 2. (a) $|I_{DS}| - V_{GS}$ and (b) μ_{FE} - V_{GS} characteristics of top-gate nanosheet SnO p-TFTs with SnO channel deposited at different O_{pp} conditions. The SnO layer was annealed at 200°C and HfO_2 layer was annealed at 100°C .

The device integrity in top-gate nanosheet SnO p-TFT is also dependent on HfO_2 annealing temperature. To avoid plasma damage to the SnO channel layer, the high- κ HfO_2 gate dielectric was deposited using an e-beam evaporator and subjected to post-annealing at 100 and 200°C for 30 min under N_2 ambient. Here the SnO layers were deposited under 25% O_{pp} and annealed at 200°C under N_2 ambient. Subsequently, the HfO_2 were deposited and annealed at 100°C or 200°C under the N_2 ambient. The $|I_{DS}| - V_{GS}$ and μ_{FE} - V_{GS} characteristics of SnO p-TFTs with 100 and 200°C post-annealing are shown in Figure 3a, b, respectively. The I_{ON}/I_{OFF} and μ_{FE} values of the SnO p-TFT at 100°C post-annealing are 1.2×10^5 and $4.4 \text{ cm}^2/\text{Vs}$, respectively, which are much better than those obtained at 200°C : 4.6×10^2 and $1.44 \text{ cm}^2/\text{Vs}$, respectively. The I_{ON}/I_{OFF} is even better than previous bottom-gate SnO p-TFT [16] possibly due to the thinner SnO channel used in this study, which slightly degrades the μ_{FE} . A thin channel layer is needed to fully deplete the conductive oxide semiconductor SnO, similar to the low I_{OFF} using ultra-thin body Si-on-Insulator (SOI) and Fin field-effect transistor (FinFET). However, the small sub-10

nm-scale channel thickness can increase the interface roughness scattering and decrease the mobility.

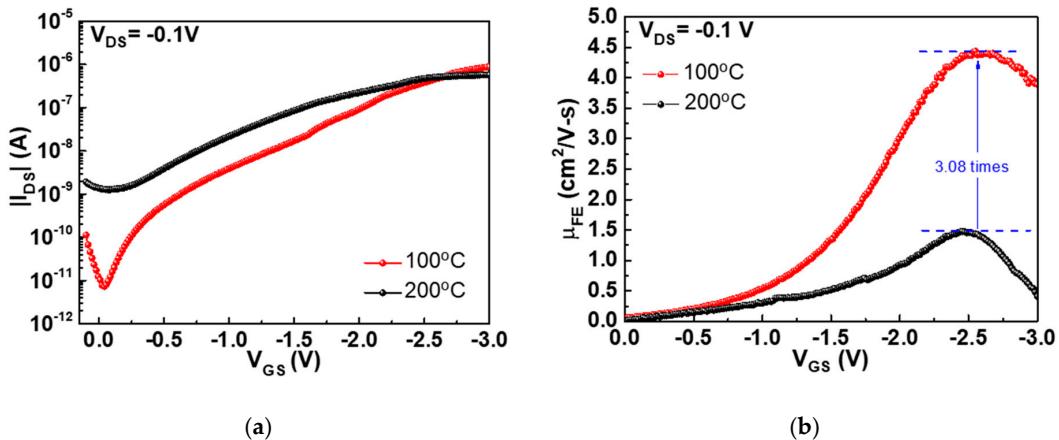


Figure 3. (a) $|I_{DS}|$ - V_{GS} and (b) μ_{FE} - V_{GS} characteristics of top-gate nanosheet SnO TFT annealed at 100 °C N₂ ambient and 200 °C N₂ ambient.

To investigate the mechanism of such annealing temperature dependence, Figure 4a,b plot the I_{DS} versus drain-source voltage (I_{DS} - V_{DS}) and the gate-source current versus gate-source voltage ($|I_{GS}|$ - V_{GS}) characteristics of top-gate SnO p-TFTs, respectively, at annealing temperatures of 100 and 200 °C. The p-TFT device at 100 °C annealing shows higher $|I_{DS}|$ than that at 200 °C annealing, corresponding to the higher μ_{FE} (Figure 3b). In normal case, a high post-annealing temperature of high- κ gate dielectric is necessary to reduce the gate leakage current and improve the device performance. However, the measured $|I_{GS}|$ of HfO₂/SnO p-TFT annealed at 200 °C shows one order of magnitude higher gate leakage current than that in the device annealed at 100 °C. The as-deposited HfO₂ layer without annealing has too high gate leakage current due to defect conduction [41] and unsuitable for device application. To decrease the defect-conductive leakage current, even higher annealing temperature is required for metal-gate/high- κ /Si CMOS [39,42,43].

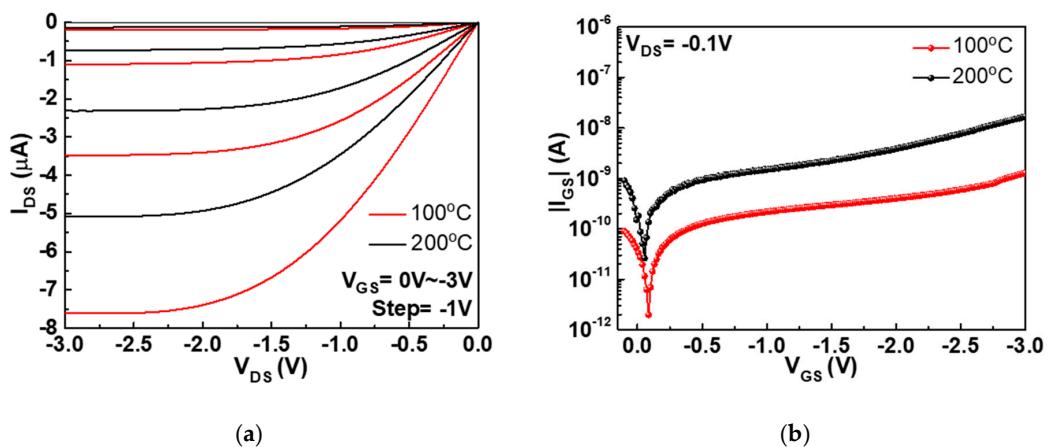


Figure 4. (a) I_{DS} - V_{DS} and (b) $|I_{GS}|$ - V_{GS} characteristics of top-gate nanosheet SnO TFTs annealed at 100 and 200 °C.

To further inspect the unusual annealing temperature dependence on device performance, material analysis of atomic force microscope (AFM), X-ray photoelectron spectroscopy (XPS), and secondary ion mass spectrometry (SIMS) were performed. In Figure S1, the surface roughness of the 50 nm HfO₂ films annealed at 100 °C, 200 °C and 400 °C were analyzed through AFM. The root mean square values of surface roughness show slightly decrease along with the increase of the annealing temperature. The HfO₂ dielectric

with different annealing temperatures were also analyzed by XPS. As shown in Figure S2, the binding energies of Hf-O and non-lattice O were 530 eV and 531.3 eV, respectively. The peak intensity of non-lattice O was related to the defects in HfO_2 dielectric, which decreased with increasing post-annealing temperature. From the AFM and XPS analysis, the good device performance at 100 °C annealing is not related to the tiny difference of HfO_2 layer.

To further investigate the O_{pp} effect on chemical composition of the SnO layer, the XPS analyses on channel SnO were performed at the O_{pp} of 14.2%, 25% and 33.3%. The HfO_2 layer of HfO_2/SnO stack were etched before the XPS analysis. The XPS data are depicted in Figure 5. The XPS spectra can be deconvoluted into three curves from the Sn^{2+}O , Sn^{4+}O_2 and Sn^0 signals, with their corresponding energies of 486.8, 486 and 484.4 eV, respectively. The composition x values of SnO_x deposited at $O_{pp} = 14.2\%$, 25% and 33.3% were 0.8, 0.95 and 1.3, respectively, which explains well the measured electrical data in Figure 2.

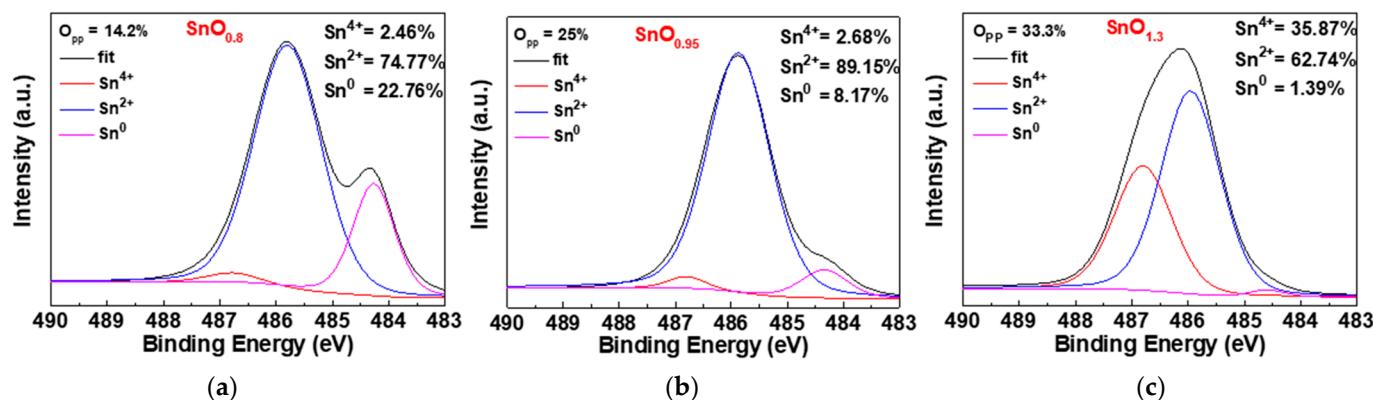


Figure 5. The Sn 3d_{5/2} spectra of SnO films deposited at O_{pp} of (a) 14.2%, (b) 25% and (c) 33.3%.

Figure 6a–c show the SIMS profiles of Hf, Sn and O atoms from the HfO_2/SnO device structure annealed at 100, 200 and 400 °C, respectively. Increasing the annealing temperature from 100 to 400 °C led to significant Sn diffusion from SnO into HfO_2 . This is attributed to the weak Sn–O band enthalpy [38], even though it also leads to high hole mobility [15,16]:

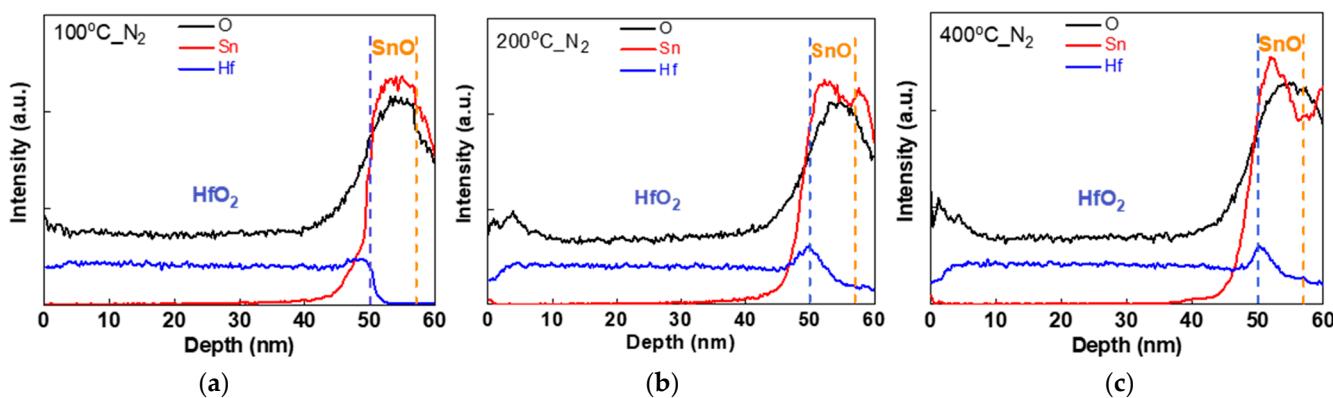


Figure 6. SIMS depth profiles of HfO_2/SnO stack annealed at (a) 100, (b) 200 and (c) 400 °C N_2 ambient.

The charged Sn^{2+} can diffuse into HfO_2 , create vacancies at elevated temperatures, and, together with charged O^{2-} ions, allow HfO_x diffusion into the SnO layer at 200 °C annealing temperature. The inter-diffusion of Sn and Hf atoms and the formed vacancies and charged ions further degrade the HfO_2 gate-dielectric and HfO_2/SnO interface that

cause poor $|I_{GS}|$, μ_{FE} , I_{ON} , and I_{OFF} . The amount of Hf diffusion into the SnO layer at 400 °C annealing temperature can be calculated by the area within SnO layer in Figure 6c, which is 1.15 times higher than the HfO₂/SnO annealed at 200 °C. The Sn atoms diffused into HfO₂ layer at 400 °C were 1.14 times more than the HfO₂/SnO annealed at 200 °C. Thus, the higher post-annealing temperature will cause more inter-diffusion between HfO₂ and SnO.

The diffused Sn²⁺ can behave as trap states in HfO₂ gate dielectric, provide extra transport paths for the carriers, and lead to higher gate leakage current (Figure 4b). To understand the conduction mechanism of gate leakage current, the measured data were fitted with various mechanisms. As shown in Figure 7a, the measured $|I_{GS}|$ - V_{GS} fits well with the hopping conduction [44–47], under an electric field (E) of <0.25 MV/cm, for 100 and 200 °C annealed top-gate SnO p-TFTs, where the slope of $\ln(|I_{GS}|)$ - E is 5.72 and 4.91, respectively. The hopping conduction mechanism is expressed as [45]:

$$|J| = qan\nu \times \exp\left[\frac{qaE}{kT} - \frac{E_a}{kT}\right], \quad (3)$$

where J , q , a , n , ν , and E_a are the current density, electron charge, mean hopping distance, carrier concentration, thermal vibration frequency of carriers at trap states, and activation energy, respectively. The hopping distances of 100 and 200 °C annealed devices calculated from Equation (3) are 1.48 and 1.27 nm, respectively. The smaller hopping distance is ascribed to the Sn diffusion in HfO₂, which increases the gate leakage I_{GS} . The mechanism of poor gate leakage current and interface at high annealing temperature is depicted schematically in Figure 7b. The trap-induced hopping conduction causes high $|I_{GS}|$. The degraded interface by Sn and Hf inter-diffusion and created vacancies increase the hole scattering from the source to drain, thus lowering the important I_{ON} and μ_{FE} . The created vacancies also increase the I_{OFF} through defect conduction. The device performance can be further evaluated by the $|I_{DS}|$ - V_{GS} hysteresis curves. The defect density formed by hysteresis curves, under forward and reverse sweep between 0 to −3 V, are 1.5×10^{12} and 5.4×10^{12} cm^{−2} for device annealed at 100 and 200 °C, respectively. This result is consistent to our conclusion: the higher post-annealing temperature creates more defects in the HfO₂/SnO gate capacitor, which leads to higher gate leakage current, lower hole mobility, and poorer hysteresis than the one annealed at lower 100 °C temperature.

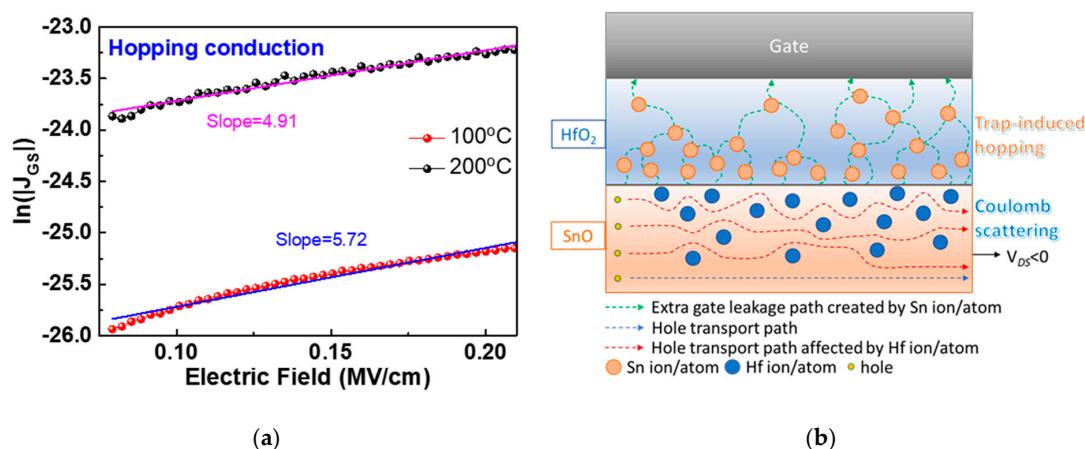


Figure 7. (a) $|I_{GS}|$ - V_{GS} characteristics of top-gate nanosheet HfO₂/SnO p-TFTs annealed at 100 and 200 °C. (b) Schematic diagram to show gate leakage and inter-diffusion of top-gate SnO TFT device annealed at 200 °C.

The sub-threshold slope is related to interface trap, which can be calculated [48]:

$$SS = \frac{KT}{q} \times \ln 10 \times \left(1 + \frac{C_{dep} + C_{it}}{C_{ox}}\right) \quad (4)$$

where the C_{dep} , C_{it} and C_{ox} are the depletion capacitance, interface trap capacitance and gate dielectric capacitance, respectively. The interface trap density (D_{it}) is $2.5 \times 10^{13} \text{ eV}^{-1}\text{cm}^{-2}$ that is higher than the metal-gate/high- κ /Si CMOS. Therefore, the hump of sub-threshold $|I_{DS}| - V_{GS}$ curve in Figure 2 is due to the charge modulation from the interface traps [49]. In comparison with SnO atomic density of $2.9 \times 10^{22} \text{ atoms/cm}^3$ or sheet atomic density of $9.4 \times 10^{14} \text{ atoms/cm}^2$, the D_{it} is only 2.7% of the sheet atoms of SnO. Thus, the electronic measurement is highly sensitive to defects compared with other measurements.

The μ_{FE} data increase to a peak value and decrease with increasing gate field. The detailed physical analysis in oxide semiconductor transistor is not reported yet. However, such hole mobility dependence is generally observed in SiO₂/Si [50], high- κ /Si [51–53], SiO₂/SiGe [54], high- κ /SiGe [55] and high- κ /Ge [56] p-MOSFETs. Because the Si, SiGe, Ge and SnO are all semiconductors and have the similar valance band structure, the decreased mobility at high electric field may be due to the similar mechanisms of phonon and interface roughness scatterings [57].

The La₂O₃ can achieve the excellent performance of low leakage current and high- κ value [55,58,59], but the moisture degradation is stronger than the HfO₂ and ZrO₂. The ZrO₂ [60] has a higher κ value than HfO₂ once crystallized, which is widely used for dynamic random-access memory (DRAM) capacitor. For gate dielectric application, orientation-independent amorphous material like conventional SiO₂ is needed [61]. The TiO₂ has the highest κ value but suffers from the small energy bandgap and high leakage current [62]. Thus, the TiO₂ is generally added to other high- κ dielectric to increase the overall κ value [63]. The Al₂O₃ has been used for gate dielectric due to its excellent stability [40], but suffers from relatively lower κ value than HfO₂. Therefore, the HfO₂ is used for CMOS application and also for this work.

To inspect the stability of the top-gate SnO TFT devices, the devices were measured at as-fabricated and after retention in air ambient for two months, as depicted in Figure 8. In comparison with the conventional bottom-gate structure, such top-gate device shows huge stability improvement after retention in air [32], which is due to fully covered channel layer by metal-gate and gate-dielectric. Therefore, both the 100 and 200 °C annealed top-gate transistors show only slight degradation after exposure in air for two months. The top-gate HfO₂/SnO p-TFT has slightly lower hole μ_{FE} of $4.4 \text{ cm}^2/\text{Vs}$ than our previously reported $7.6 \text{ cm}^2/\text{Vs}$ of bottom-gate HfO₂/SnO device, which is attributed to the HfO₂/SnO interdiffusion. Because of the larger SS of top-gate device than the bottom-gate one with the same HfO₂ and SnO, the HfO₂/SnO interface degradation is confirmed from Equation (4).

Table 1 presents a comparison of the essential device characteristics of top-gate SnO p-TFTs [11,33–35]. The merits of this work are the highest μ_{FE} of $4.4 \text{ cm}^2/\text{Vs}$, largest I_{ON}/I_{OFF} of 1.2×10^5 , and sharpest SS of 526 mV/decade reported to date at fabrication temperatures of only 100–200 °C. This device thus has high potential to be integrated into the IMD layer of Si chips for monolithic 3D and brain-mimicking IC applications.

Table 1. The device performances of various top-gate SnO p-TFTs.

Reference	SnO Thickness (nm)	Gate Insulator Materials	μ_{FE} ($\text{cm}^2/\text{V}\cdot\text{s}$) @ V_{DS} (V)	I_{ON}/I_{OFF}	SS (mV/Decade)	Process Temp. (°C)
11	15.4	Y ₂ O ₃	0.05 @-1	10^2	-	250
33	20	Al ₂ O ₃	1.3 @-2	10^2	7	575
34	15	HfO ₂	0.71 @-1	1.6×10^3	1.6	200
35	30	P(VDF-TrFE)	2.7 @-1	2.2×10^2	4	200
This work	7	HfO ₂	4.4 @-0.1	2×10^5	0.526	200

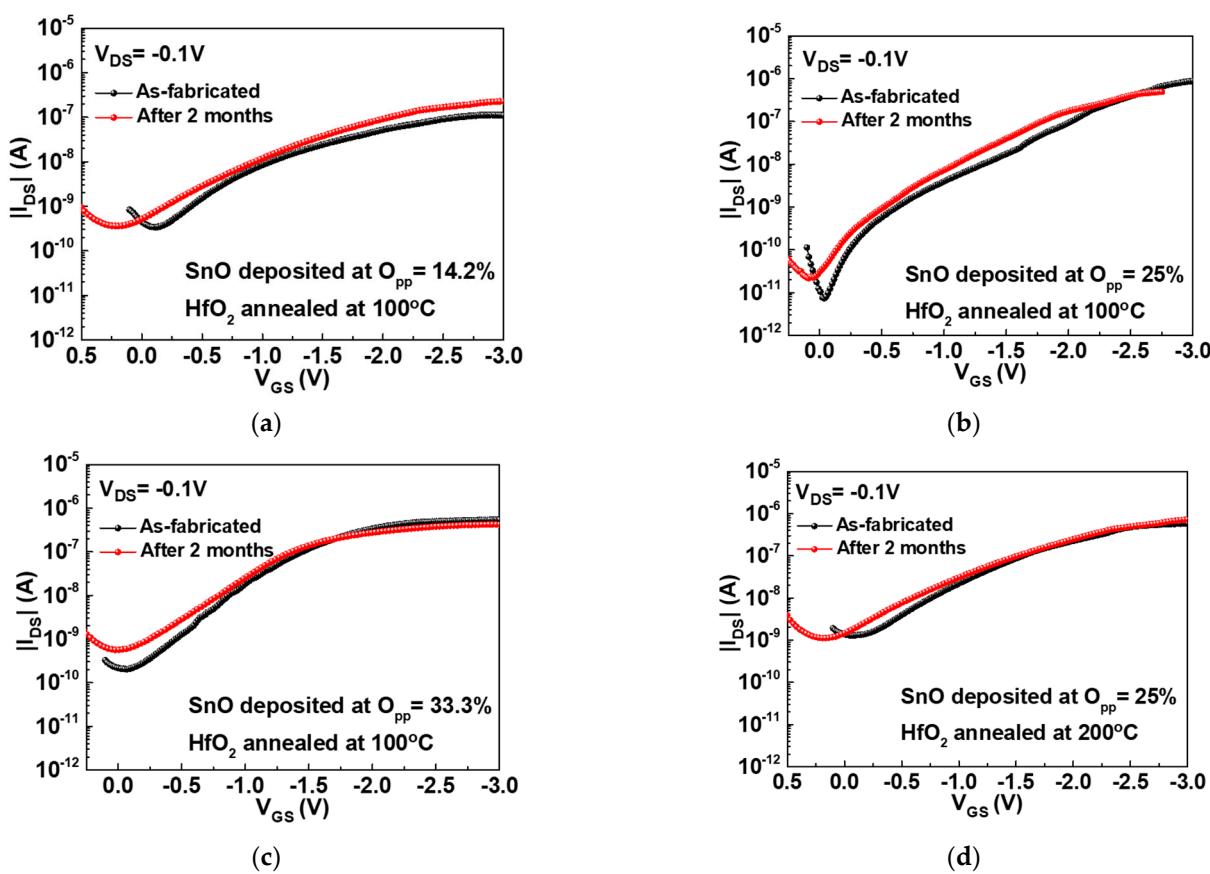


Figure 8. The $|I_{DS}|$ - V_{GS} characteristics of the top-gate nanosheet SnO TFT devices with (a) SnO deposited at $O_{pp} = 14.2\%$ and HfO_2 annealed at $100^\circ C$, (b) SnO deposited at $O_{pp} = 25\%$ and HfO_2 annealed at $100^\circ C$, (c) SnO deposited at $O_{pp} = 33.3\%$ and HfO_2 annealed at $100^\circ C$, and (d) SnO deposited at $O_{pp} = 25\%$ and HfO_2 annealed at $200^\circ C$. The devices were measured at as-fabricated and after 2 months' exposure to air ambient.

4. Conclusions

While SnO has the advantage of high hole mobility, it also has low bond enthalpy. The key factor for good device integrity of top-gate HfO_2/SnO p-TFT is to maintain the low process temperature, which can preserve good HfO_2/SnO interface. Such a low-temperature fabrication ($100\text{--}200^\circ C$) and excellent device performance are crucial for monolithic 3D and brain-mimicking ICs made on the backend IMD layers of Si chips.

Supplementary Materials: The following are available online at <https://www.mdpi.com/2079-4991/11/1/92/s1>; Figure S1: The surface roughness analysis of HfO_2 annealed at (a) $100^\circ C$, (b) $200^\circ C$ and (c) $400^\circ C$ through AFM. Figure S2: The O_{1s} spectra of HfO_2 films annealed at (a) $100^\circ C$, (b) $200^\circ C$ and (c) $400^\circ C$.

Author Contributions: T.J.Y. did the experiments; A.C. is the principle investigator (PI) to monitor the project; V.G. is the co-PI for this work. All authors reviewed the manuscript. All authors have read and agreed to the published version of the manuscript.

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Conflicts of Interest: The authors declare no conflict of interest.

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