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Characteristics and Electronic Band Alignment of a Transparent p-CuI/n-SiZnSnO Heterojunction Diode with a High Rectification Ratio

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Abstract: Transparent p-CuI/n-SiZnSnO (SZTO) heterojunction diodes are successfully fabricated by thermal evaporation of a (111) oriented p-CuI polycrystalline film on top of an amorphous n-SZTO film grown by the RF magnetron sputtering method. A nitrogen annealing process reduces ionized impurity scattering dominantly incurred by Cu vacancy and structural defects at the grain boundaries in the CuI film to result in improved diode performance; the current rectification ratio estimated at ± 2 V is enhanced from $\approx 10^6$ to $\approx 10^7$. Various diode parameters, including ideality factor, reverse saturation current, offset current, series resistance, and parallel resistance, are estimated based on the Shockley diode equation. An energy band diagram exhibiting the type-II band alignment is proposed to explain the diode characteristics. The present p-CuI/n-SZTO diode can be a promising building block for constructing useful optoelectronic components such as a light-emitting diode and a UV photodetector.

Keywords: copper iodide (CuI); SiZnSnO (SZTO); transparent diode; current rectification ratio; energy band alignment

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1. Introduction

The γ -phase of copper iodide (CuI) with a direct bandgap (E_g) of \approx 3.1 eV has been attracting increased attention as an emergent transparent p-type semiconductor with a high hole mobility (μ_h); for example, the μ_h value reaches up to \approx 44 cm²V-¹s-¹ in a single crystal, thereby being higher than that of any other conventional p-type oxides [1]. Even in a thin film form, CuI exhibits a relatively high μ_h of typically 6–7 cm²V-¹s-¹ at a hole concentration (p) of \approx 10¹9 cm-³ [2]. Moreover, with the additional heat treatment such as ex situ thermal annealing [3] or in situ thermal annealing during deposition [4], μ_h values of those films are further enhanced more up to \approx 26 cm²V-¹s-¹. Such thermal annealing processes are known to suppress not only Cu vacancy (V_{Cu}), which is the main source of acceptor in the CuI system, but also structural defects such as pinholes or grain boundaries. In this respect, the CuI thin films with proper heat treatment can play an important role of being a transparent p-type layer in various optoelectronic devices such

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as solar cells [5], a light-emitting diode [6], a field-effect transistor [7], and a UV photodetector [8,9].

In order to realize a transparent pn diode based on the CuI, we have been investigating various heterojunction diodes made of p-CuI and n-type semiconductors [2,8–11]; in our previous work, we have reported a transparent diode made of p-CuI/n-BaSnO_{3- δ} (BSO) films and its carrier transport behavior [12]. The realized p-CuI/n-BSO diode exhibited a high current rectification ratio (I_F/I_R) of 6.75×10^5 at an external voltage bias of ± 2 V. On the other hand, a high-quality BSO film often requires an epitaxial growth on a proper substrate such as SrTiO₃ (001), and its ideal growth temperature is rather high (≈ 800 °C). Therefore, for the applications in e.g., flexible UV photodetectors, it is desirable to test a heterojunction diode made of an alternative n-type film that can be grown at a relatively low-temperature condition comparable to that of the CuI film and without the constraint of epitaxy.

Along this line of reasoning, Yamada et al. have recently reported that a heterojunction diode made of p-CuI film and the well-known n-type amorphous semiconductor InGaZnO (IGZO) film exhibits a high rectification ratio of $\approx 10^9$ [8]. Independent of this promising approach, we have been focusing on a new n-type amorphous semiconductor SiZnSnO (SZTO) film that exhibits a high optical gap E_8 larger than 3.7 eV [13] and a field-effect mobility of ≈ 38 cm 2 V $^{-1}$ s $^{-1}$ [14]. It has been found that the n-type SZTO film maintains enhanced electrical stability as compared to the IGZO film [13], which is possibly due to reduced oxygen vacancies as controlled by Si concentration via strong Si=O bonding [15]. In addition, the n-type SZTO film has another advantage of being composed of non-toxic and abundant elements of Si and Sn. Therefore, we decided to adopt the SZTO as a transparent n-type layer to realize a new heterojunction diode with the p-CuI film.

Another potential merit of the p-CuI/n-SZTO diode lies in the capability of tuning the electronic energy diagram of the n-type amorphous ZnSnO layer by the control of Si concentration. Such a capability might provide an opportunity for improving the efficiency of a potential optoelectronic device such as a light-emitting diode. As an example, Baek et al. [6] have shown that the performance of the light-emitting diode made of p-CuI/n-Mg $_x$ Zn $_{1-x}$ O quantum dot (x = 0, 2.7, and 6 at %) has improved when the energy level difference between n-Mg $_x$ Zn $_{1-x}$ O and Al electrode is adjusted via the control of x. The imbalance between the injected hole and electron carriers at the interface of a light-emitting diode can potentially lead to the decreased device performance. Thus, the control of electron and hole injection ratios via a proper tuning of energy band diagram can be an effective way to improve performance of the given light-emitting diode.

Yet another promising application direction of the p-CuI/n-SZTO diode is a self-powered UV photodetector [16]. Recently, the photo-response of various pn diode structures made of p-CuI films (or nanoparticles) and various n-type materials are widely being tested; those n-type materials include IGZO films [8], CsPbBr $_3$ crystals [9], ZnO:Au films [17], and ZnO films [18], and β -Ga $_2$ O $_3$ single crystals [19]. Once realized, those photodetectors made of the pn diode are expected to have self-powered characteristics and reliable responsivity under UV light illumination [8,9,17,18]. Thus, the diode made of p-CuI and n-SZTO can be another promising platform for realizing a flexible, transparent UV photodetector with a capability of tuning electronic band diagram in the SZTO layer. To realize such a device, quantitative understandings on the diode performance and energy band alignment at the interface should be prerequisite.

With the above motivations, we here report the realization of transparent heterojunction diodes made of novel transparent polycrystalline p-CuI film and amorphous n-SZTO film that has resulted in a high rectification ratio I_F/I_R of $\approx 10^7$. To investigate the diode characteristics, various diode parameters, such as ideality factor, reverse saturation current, and series resistance, etc., are estimated from the diode curve fitting based on the Shockley diode equation. We propose an energy band diagram of the p-CuI/n-SZTO diode exhibiting type-II heterojunction and attribute the high rectification

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ratio to the improved transport properties of the CuI film, resulting from reduced ionized impurity scattering of Cu vacancies and enhanced diode interface via reduced structural defects. Our results show that the diode made of *p*-CuI/*n*-SZTO films exhibits an excellent electrical performance as a transparent *pn* diode with potential tunability of the energy band diagram, which can be useful for realizing flexible, cost-effective optoelectronic devices such as UV photodetectors and light-emitting diodes.

2. Experimental Section

 In_2O_3 :Sn (ITO, film thickness t = 50 nm) and SZTO (t = 27 nm) films were deposited on boro-aluminosilicate glass substrates (EAGLE XG slim glass, Corning) (t = 0.5 mm) by the DC and RF sputtering technique. The ITO ceramic disk was used as a target for the ITO film growth at a power of 30 W in Ar pressure of 4 mTorr at room temperature by a commercial DC magnetron sputtering (KVS-2002, Korea Vacuum Tech, Korea). After patterning with the photolithography methods, the SZTO film was subsequently deposited at a power of 60 W by the RF magnetron sputtering technique (KVS-2004, Korea Vacuum Tech, Korea) in a mixed gas of Ar and O2 at room temperature; the gas flow ratio of Ar and O₂ was set for 40:1 sccm. The as-deposited SZTO/ITO film was annealed at 500 °C for 2 h at ambient condition, and the detailed conditions for the target synthesis and the film growth were described in our earlier report [13]. A custom-made thermal evaporator was used for the deposition of the CuI films with the CuI powder (purity ≈99.998%) at room temperature on glass substrates (soda-lime glass for a microscope slide, Marienfeld) and SZTO/ITO/glass. For the fabrication of p-CuI/n-SZTO diodes, both CuI and Au/Ni films have been sequentially deposited with stencil masks that can produce 10 circular dots with a typical radius of 50 µm. The Au/Ni film (Figure 1a) was deposited to form ohmic contact between the CuI film and a tungsten probe tip; the Ni film (t = 5 nm) with a circular dot shape was first deposited on top of the CuI film, followed by the deposition of Au film (t = 50 nm) with the same circular dot size. It confirmed that two circular dots of the Au/Ni film grown on top of the CuI film exhibit linear behaviors in the current–voltage (*I-V*) curves by two tungsten probe tips connected to each dot (see, Figure S1). This implies that good ohmic contact was formed between Au/Ni films and CuI films as the *p*-type channel for a diode. Furthermore, the same measurements were performed with two tungsten probe tips connecting two respective circular dots of the ITO film grown on the SZTO film. It shows that good ohmic contact was formed between ITO and SZTO films as the *n*-type channel. The as-grown diodes were annealed at 50 °C for 125 h under the N₂ gas flowing condition of 20 mL/min. Optical transmittance and reflectance spectra measurements on the CuI/SZTO/ITO/glass were carried out by the UV-VIS-NIR spectrophotometer (Cary 5E, Varian). The crystallinity of films has been investigated by the θ -2 θ scans in a high-resolution X-ray diffractometer (EmpyreanTM, PANalytical, Korea). The structural characterizations were conducted using atomic force microscopy (AFM) (NX10, Park Systems, Korea). The current density-voltage (|j|-V) (or I-V) characteristics of the diodes were investigated by the semiconductor parameter analyzer (4200-SCS, Keithley, Korea); all the measurements were performed under dark and air conditions at room temperature.

3. Results and Discussion

Figure 1a shows a schematic structure of the fabricated p-CuI/n-SZTO diode for electrical measurements, in which the SZTO film is grown on the ITO/glass, followed by the subsequent deposition of the circular CuI film and the metallic (Au/Ni) electrode. Figure 1b is an actual photograph of the CuI/SZTO/ITO/glass film without the Au/Ni layer, demonstrating that all the layers are transparent in the visible spectral range. The CuI/SZTO films (the orange dashed line) were deposited with a lateral size of $10 \times 4 \text{ mm}^2$ on the ITO/glass substrate (the green dashed line); the thicknesses of the CuI, the SZTO, and the ITO films are 110, 27, and 50 nm, respectively. Hereafter, we denote the term CuI (x nm) as x nm-thick CuI film where x represents the thickness of the CuI film (tCuI).

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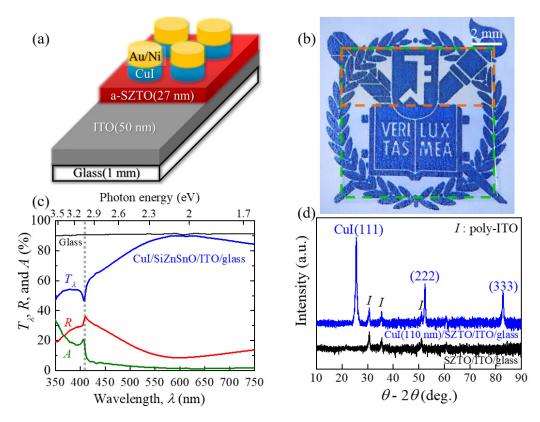


Figure 1. (a) A schematic structure of the *p*-CuI/*n*-SiZnSnO (SZTO) diode grown on the ITO deposited glass substrate, which was used for electrical characterization in this work. The CuI film of circular disk shape (with a diameter of 50 μm) were fabricated in two thicknesses of 140 and 20 nm while the thicknesses of SZTO and ITO films were 27 and 50 nm, respectively. Au/Ni (t = 50/5 nm) films were subsequently deposited on top of the CuI disk. (**b**) A separate film fabricated for optical characterization. The CuI(110 nm)/SZTO(27 nm) (the orange dashed line) were homogeneously deposited on top of the ITO/glass substrate (the green dashed line). All the regions exhibit clearly optical transparency. (**c**) Optical transmittance (T_{λ}), reflectance (R), and absorption (A) spectra of the CuI (110 nm)/SZTO/ITO/glass sample shown in (**b**). The black solid line represents T_{λ} of a glass substrate (t = 1 mm) only. (**d**) X-ray θ -2 θ scan results of the CuI (110 nm)/SZTO/ITO/glass film shown in (**b**) and of another SZTO/ITO/glass film. The CuI film exhibits the preferential orientation of a (111) plane, and additional peaks represent a polycrystalline ITO film indicated as I.

Figure 1c exhibits the optical transmittance (T_{λ}), reflectance (R), and absorption (A) spectra as a function of wavelength λ for the CuI/SZTO/ITO/glass (Figure 1b), and a black solid line represents T_{λ} of a bare glass substrate. The absorbance is obtained from the relationship of $A = 100 - T_{\lambda} - R$, exhibiting small values less than 5% at $\lambda \geq 450$ nm. The maximum T_{λ} of the CuI/SZTO/ITO/glass is indeed found to be as high as $\approx 90\%$ and is always larger than $\approx 80\%$ in the visible spectral region (500–750 nm). In addition, the transmittance of the glass substrate $T_{\lambda,\text{glass}}$ is a nearly constant of ≈ 0.9 (the black solid line). According to the relationship of $T_{\lambda,\text{film}} = T_{\lambda,\text{measured}}/T_{\lambda,\text{glass}}$, $T_{\lambda,\text{film}}$ of the remaining films (CuI/SZTO/ITO) is then likely to be higher than $\approx 88\%$ in the visible spectral region. All these results quantitatively demonstrate why the fabricated diode structure (CuI/SZTO/ITO/glass) maintains optical transparency, as shown in Figure 1b.

In addition, it is noteworthy that an exciton absorption peak is found at 407 nm (3.05 eV) (a gray dotted line in Figure 1c), as frequently observed in the CuI film [2,4,10,12]. Then, E_g of the CuI film is estimated as \approx 3.1 eV from the relationship of $E_g = E_{Z1,2} + E_{ex}$ where $E_{Z1,2}$ is an exciton absorption energy of CuI and E_{ex} is an exciton binding energy of 62 meV [20]. The obtained E_g value is similar to our previous result (\approx 3.08 eV) [12] and other reports [2–4]. Based on the observation of the similar optical bandgap, the optical spectra are likely to be expected as high enough regardless of t_{CuI} , as confirmed in the

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previous report [12]. Furthermore, the observation of such a sharp exciton absorption peak supports that the as-grown CuI film is of high quality.

The crystallinity of the as-grown films (CuI/SZTO/ITO/glass substrate) has been investigated by the X-ray θ 2 θ scan in Figure 1d. The CuI film exhibits a preferred orientation along the (111) plane, similar to the CuI/glass sample case (see, Figure S2 for the X-ray result). Since the nearest bottom layer is composed of an amorphous material, i.e., SZTO film or glass substrate, this (111) peak is unlikely to originate from the epitaxial CuI film [12]. It is well-known that the CuI system exhibits randomly oriented in-plane domains within the CuI (111) plane due to the low surface stability energy of the (111) plane [2]. The SZTO film cannot be identified in Figure 1d due to its amorphous nature, as confirmed by our previous transmission electron microscopy and X-ray photoelectron spectroscopy studies [21,22]. The extra peaks are the polycrystalline ITO film denoted as a symbol of I in Figure 1d.

To investigate the electrical transport of the diodes before and after the N_2 annealing, we measured the I-V curves of the diodes, which have the structure shown in Figure 1a using a two-point contact method. In this configuration, the two probe tips are connected to Au/Ni and ITO films for p-CuI and n-SZTO layers, respectively. Figure 2a shows the I-V curve (black solid line) of the as-grown CuI (140 nm)/SZTO diode in a linear scale. A turn-on voltage (Vturn-on), which is the on-set voltage for a large increase in the current level, has been determined from a linear extrapolation of the I-V curve in Figure 2a. The estimated Vturn-on of the as-grown diode was 1.73 V. Figure 2b presents the corresponding |j|-V curve in a semi-log scale. To extract the quantitative information on the diode parameters, we have tried to fit the data with the Shockley diode equation in the full range from -2 V to +2 V:

$$I(V) = I_{s} \left[\exp\left\{ \frac{e(V - IR_{s})}{\eta k_{B}T} \right\} - 1 \right] + \frac{V - IR_{s}}{R_{p}} + I_{o}$$
 (1)

where I_s is the reverse saturation current, η is the ideality factor, k_B is the Boltzmann constant, T is the absolute temperature, I_o is the offset current, R_s is the series resistance, and R_P is the parallel resistance [11]. The orange lines in Figure 2b represent the curve fitting results, which indeed well explain the measured data except for the irreversible charge trap effect near 0.8 V. We will discuss the resultant parameters in Figure 3.

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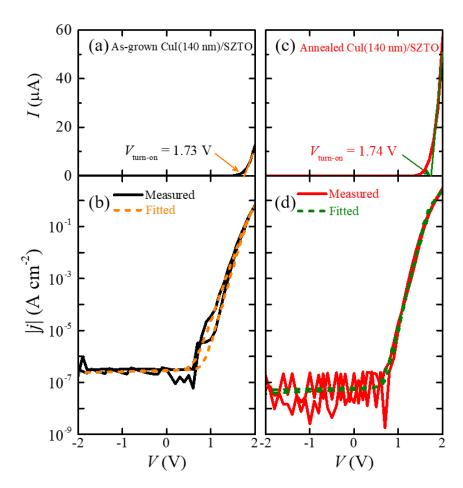


Figure 2. (a) The current–voltage I-V curve in a linear scale and (b) the current density–voltage |j|-V curve in a semi-log scale of the as-grown CuI (140 nm)/SZTO diode. (c) The I-V and (d) |j|-V curves of the annealed CuI(140 nm)/SZTO diode. The orange and the green solid lines in the I-V curves represent the linear extrapolation to determine the turn-on voltage of a diode, V-turn-on, while the orange and green dashed lines in the |j|-V curves correspond to the diode fitting results based on Equation (1).

Similarly, the measured I-V and |j|-V curves in the annealed CuI (140 nm)/SZTO diode are plotted as red solid lines in Figure 2c,d, respectively. The green dashed line of the |j|-V curve represents the curve fitting result. What is most conspicuous in the behavior of the annealed diode is the decrease (increase) of the current level in the negative (positive) bias region. This immediately points out that the current rectification ratio I_F/I_R , where I_F is the current value at +2 V and I_R is the current at -2 V, is enhanced after the annealing. As the SZTO layer is expected to be stable at the annealing condition (50 °C, 125 h), to understand the enhancement of I_F/I_R, one should understand first how the annealing process will affect the properties of CuI film. It is known that in the asgrown CuI film, Vcu is likely to exist, behaving as a dominant acceptor source and also as an ionized impurity scattering source. Upon the ex situ thermal annealing at 50 °C being performed for 125 h, iodine vacancies (Vi) can be additionally created, thereby compensating the native V_{Cu} . In addition to V_{Cu} compensation by V_{I} , thermal energy can provide extra energy for rendering the migration of existing Cu vacancies from the inside of the CuI film to the outside of the surface or grain boundary [3]. Therefore, the optimal thermal annealing can lead to suppression of ionized impurity scattering via the compensation of V_{Cu} by V_{I} and also by the reduction of V_{Cu} inside the CuI film. At the same time, a reduction of structural defects near the grain boundaries of the CuI film is also expected, which in turn can form a smooth and uniform interface to improve the pn diode Nanomaterials **2021**, 11, 1237 7 of 14

performance. Reduced grain boundaries after annealing can be verified in the AFM image of the CuI film/glass in Figure S3.

Several pieces of evidence supporting improved diode performance after annealing can be found in the I-V (or |j|-V) characteristics in Figure 2c,d; the hysteresis of the |j|-V curve between the forward and reverse sweeping directions decreases, V_{turn-on} slightly increases from 1.73 to 1.74 V, the offset current I0 decreases in the flat range from -2 to +0.7 V, and the |j|-V curve produces significant noise in the flat region. To better understand microscopically how the diode performance improves, we discuss here the supporting evidence in more detail. First, it should be reminded that irreversible charge traps mainly cause the diode hysteresis because the charged trap sites, such as Vcu, act as a slowly responding component under external voltage bias. Thus, the decreased hysteresis in the |j|-V curve demonstrates that the charged trap sites have been greatly reduced.

Second, the slight increase of $V_{\text{turn-on}}$ from 1.73 to 1.74 V also supports the improved diode performance. A threshold voltage (V_{th}), which is an ideal voltage to begin the current flow, is expected to become fairly high in this diode; it is expressed by $V_{\text{th-p}} = V_{\text{bi}} +$ $|\Delta E_{\rm V}/e|$ for a *p*-type carrier and by $V_{\rm th-n} = V_{\rm bi} + |\Delta E_{\rm C}/e|$ for an *n*-type carrier, where $V_{\rm bi}$ is the built-in potential of a diode, ΔE_V is the valence band offset, and ΔE_C is the conduction band offset between two semiconductors [2]. Based on the band diagram of the CuI/SZTO diode (vide infra, Figure 5), it turns out to be $V_{\rm bi} = 0.99 \text{ V}$, $|\Delta E_{\rm V}/e| = 2.55 \text{ V}$, and $|\Delta E_{\rm C}/e| =$ 1.90 V, resulting in $V_{\text{th-p}}$ = 3.54 V for the injection of holes from p-CuI to n-SZTO and $V_{\text{th-n}}$ = 2.89 V for the injection of electrons from *n*-SZTO to *p*-CuI. Thus, it is likely that electron injection is more probable than hole injection because the absolute conduction band offset $|\Delta Ec/e|$ is 0.66 V less than $|\Delta Ev/e|$. The obtained $V_{turn-on} = 1.74$ V in Figure 2c for the annealed diode is obviously smaller than the predicted $V_{\text{th-n}}$ = 2.89 V. Since the V_{Cu} creates an intermediate state that can form an additional current path at the diode interface, the actual $V_{\text{turn-on}}$ should be lower than V_{th} in general. Therefore, in turn, the increased $V_{\text{turn-on}}$ after annealing indicates reduced extra leakage current paths by the decrease of V_{Cu} or by the compensation of V_{Cu} .

Finally, the reduced I_0 after annealing also supports the improved diode performance. I_0 can be generated by other leakage sources irrelevant to the bias voltage such as instrumental effects or pinholes that can exist across two electrodes. Once I_0 was formed at a diode, it appears as a constant current in the flat region of the |j|-V curve; for instance, the I_0 level is ≈ 5.9 pA in the bias range from -2 to +0.7 V in Figure 2b. Therefore, the reduced I_0 level from 5.9 to 1.1 pA after the annealing in Figure 2d indicates that such a side effect has been mitigated by the annealing, too. As the I_0 decreased after annealing, the current noise in the negative bias range concurrently increased. It implies that the actual current is small enough to reach the resolution limit of the instrument (Keithley 4200-SCS, ± 1 pA).

Figure 3 compares all the obtained diode parameters for both CuI (20 nm)/SZTO and CuI (140 nm)/SZTO diodes before and after annealing. Here, we remind the physical meaning of each diode parameter except for I_F/I_R and I_O already explained above. I_S represents the reverse saturation current, which occurs by the minority carriers located at the depletion region of a pn diode. η describes a diode transport model; η is known to change by diffusion (η = 1), recombination (η = 2), and numerous defects region (η > 2). R_S is determined by the contact resistance of several junctions between two films and between the electrode/film, and R_P represents the parasitic parallel resistance formed by an additional leakage path. In the case of the CuI (140 nm)/SZTO diode, the annealing process results in the increase of I_F/I_R from 2.7 × 106 to 6.6 × 107 by ≈25 times, the decrease of I_O from 5.9 to 1.1 pA, the nearly same I_S being a quite low level of ≈0.07 fA, the decrease of η from 2.96 to 2.66, the decrease of R_S from 6.1 to 3.9 kΩ, and the slight increase of R_P from ≈2 to ≈5 TΩ shown in Figure 3.

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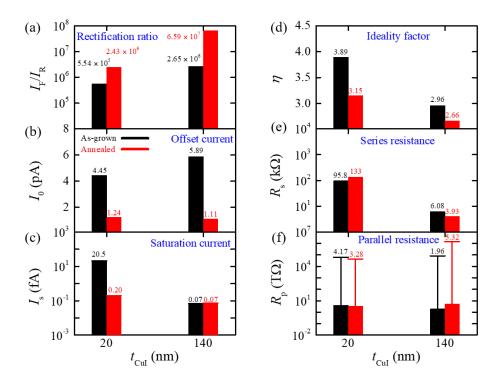


Figure 3. Summary of various diode parameters; (a) current rectification ratio I_F/I_R , (b) offset current I_o , (c) reverse saturation current I_s , (d) ideality factor η , (e) series resistance R_s , and (f) parallel resistance R_p . Black and red colors represent the data of the as-grown and annealed diode, respectively. All the parameters are estimated by fitting the results in Figure 2b,d with Equation (1). Error bars in (f) represent the least square fitting error. Error bars from the least square fitting were less than 5% for the other parameters (b–e).

The thermal annealing process, as explained in Figure 2, is likely to induce several physical processes; (1) the decrease of charged trap sites by Vcu, (2) a reduction of grain boundaries from the out-diffusion of V_{Cu} , and (3) a reduced ionized impurity scattering with reduced p-type carriers (see, Figure S5 for the CuI/glass Hall effect results). All the processes (1)–(3) can result in a decreasing tendency, as observed in the parameters I₀ and R_s. The decrease of I_0 implies that other leakage sources such as the pinholes across two electrodes are reduced as a result of reduced vacancies, p-type carriers, and grain boundaries. Furthermore, with reduced grain boundaries, the contract resistance R_s between the CuI and the Au/Ni film is likely reduced, too. In addition, the η = 2.96 before annealing (Figure 3d) suggests the presence of numerous defects at the diode depletion region. Thus, the decrease of η from 2.96 to 2.66 after thermal annealing suggests reduced V_{Cu} and improved diode interface to become more homogeneous. The increase of R_P by ≈ 3 T Ω , albeit having a large least square fitting error close to the instrumental measurement limit, is also consistent with the reduced V_{Cu} . The thermal annealing did not affect the saturation current, producing the nearly same value of $I_s = \approx 0.07$ fA, which is close to the instrumental resolution limit. This implies that $I_s = \approx 0.07$ fA is indeed close to an ideal value expected in this diode configuration. All the positive effects reflected in those parameters in Figure 3b-f after the annealing process coherently explains why I_F/I_R has been improved by ≈ 25 times from 2.7 × 10^6 to 6.6×10^7 in the CuI (140 nm)/SZTO diode (Figure 3a).

To compare how the annealing can affect the characteristics of the diode made of a thinner CuI film, we have similarly studied the electrical properties of the CuI (20 nm)/SZTO diode before and after applying the same thermal annealing conditions, of which I-V (|j|-V) curves are provided in Figure S6. All the parameters obtained from the curve fitting results based on Equation (1) are also summarized in Figure 3; in the CuI (20 nm)/SZTO diode, the thermal annealing results in the decrease of I0 from \approx 4.5 to 1.2 pA, the decrease of I0 from 20.5 fA to 0.20 fA, the decrease of η from 3.89 to 3.15, and the nearly

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same of R_P of ≈ 4 T Ω . The initial values of I_s and η after the growth seem to be all larger than the corresponding values in the CuI (140 nm)/SZTO diode, while I_o and R_P are comparable. This indicates that the contribution of V_{Cu} and related grain boundaries are larger in the thin (20 nm) films to cause the numerous defect regime in the diode, i.e., $\eta = 3.89$. After annealing, all the parameters of I_o , I_s , and η exhibit improvement, as similarly observed in the thick diode. Therefore, the thermal annealing seems to be also effective in improving the physical properties of the CuI (20 nm) film by reducing V_{Cu} , grain boundaries, and ionized impurity scattering.

The most notable difference between the CuI (20 nm) and the CuI (140 nm) diode is found in the variation of R_s and I_F/I_R ; after annealing, R_s increases from 95.8 to 133 k Ω , while I_F/I_R exhibits a slight increase from 5.5×10^5 to 2.4×10^6 . Note that $I_F(+2V)/I_R(-2V)$ was calculated from the fitting curves in this case to avoid the noise-induced errors in the estimation of I_R (-2V). In general, R_s is a main limiting factor for I_F , as the forward bias voltage dropped by the interface contact resistance; I_F is supposed to decrease, being roughly proportional to R_s . Therefore, the moderate increase of I_F/I_R by a factor of ≈ 4 in the CuI (20 nm) diode, as compared with the factor of ≈25 increase in the CuI (140 nm) diode should be mainly attributed to the unexpected increase of R_s. Without the deterioration of R_{s} , the improvements of the other parameters I_{o} , I_{s} , and η should have produced much more enhanced I_F/I_R. The undesirable increase of R_s upon annealing indicates that the CuI (20 nm) film just starts to degrade due to the formation of a large amount of V₁. The thermal degradation of the CuI has been known in the thin films with $t_{CuI} < 100$ nm [3] and even in a crystal [23]. If the CuI is subject to excessive thermal annealing, out-diffusion of V_{Cu} and the excessive formation of V_{I} can give rise to degradation in the physical properties of CuI; it becomes porous, exhibits yellowish-brown colors, and eventually develops many cracks [3]. Therefore, for a very thin film limit of tcuI < 100 nm, it is expected that a shorter time or a lower temperature for annealing might be suitable to achieve a higher I_F/I_R . Thus, our results indicate that an optimal annealing condition should be carefully searched for each thin film with a different thickness.

It is emphasized that $I_F/I_R = 6.6 \times 10^7$ is quite a high value among the heterojunction diodes consisting of the p-CuI film. Figure 4 compares I_F/I_R of the p-CuI/n-SZTO diodes with those of other CuI-based transparent heterojunction diodes that have a high $I_F/I_R > \approx 10^5$; 2 × 10 7 at ±2 V for p-CuI/n-ZnO (a polycrystalline CuI film) [2], 2 × 10 9 at ±2 V for p-CuI/n-ZnO (an epitaxial CuI film) [11], 7 × 10 5 at ±2 V for p-CuI/n-BaSnO_{3- δ} [12], 6 × 10 6 at ±2 V for p-CuI/n-IGZO [3], and $\approx 10^9$ at ±1.5 V for p-CuI/n-BaSnO_{3- δ} [12], 6 × 10 6 at ±2 V for p-CuI/n-IGZO (x = 0.0 - 1.0) [10]. Albeit the highest value of $I_F/I_R = \approx 2 \times 10^9$ realized in the p-CuI/n-ZnO diode is higher than that of the present p-CuI/n-SZTO diode by ≈ 30 times, to realize such a diode requires a special growth condition, i.e., an epitaxial growth of the CuI film on top of an epitaxial ZnO film. This implies that such a high I_F/I_R is hard to achieve in a flexible device. Although the $I_F/I_R = \approx 1 \times 10^9$ in the p-CuI/n-IGZO diodes looks also higher than that of the p-CuI/n-SZTO diode, a proper comparison of I_F/I_R might be required as the work used the measured I_F and the fitted I_S [10].

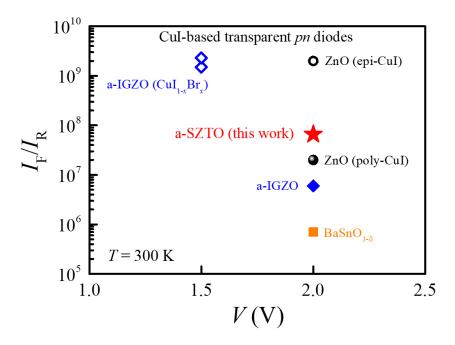


Figure 4. Summary of current rectification ratios I_F/I_R of various heterojunction diodes consisting of the p-CuI film. The color indicates different n-type films for the pn diodes, and here only the cases of a high $I_F/I_R > \approx 10^5$ are provided. I_F/I_R of the CuI/SZTO diode is estimated by the fitted I_F at +2 V and I_R at -2 V in this work. I_F/I_R of the CuI_{1-x}Br_x/IGZO diode is estimated by the measured I_F at +1.5 V and the fitted reverse saturation current [10]. I_F/I_R of CuI/ZnO [2,11], CuI/a-IGZO [3], and CuI/BaSnO₃₋₈ [12] diodes are obtained from the measured current at ± 2 V.

To quantitatively compare the performance of various diodes made of the p-type CuI and n-type materials, several diode parameters and photo-response results are also summarized in Table 1. The main parameter that characterizes the one-way electrical transport of a diode is I_F/I_R . Most of the diode exhibit I_F/I_R larger than $\approx 7 \times 10^5$ except recent two devices with rather large interface areas as they focus on the increase of photocurrent in the pn diode [9,19]. The ideality factor η seems to be lower than 2 when the n-type materials are epi-films of ZnO or amorphous IGZO film while the η of the p-CuI/n-SZTO is as large as 2.7–3.0, indicating that disorder effects in the CuI film can be further reduced by better annealing or growth conditions. The I_s of the p-CuI/n-SZTO diode is much lower than those of the p-CuI/n-ZnO and the p-CuI_{1-x}Br_x/n-IGZO diodes due to the inclusion of offset current in the fitting process. The R_s value of the p-CuI/n-SZTO is still higher than those of other diodes, leaving rooms for improvement by reducing interface resistance at the pn junction and p- or n-type films/electrodes. Therefore, if the R_s and the η can be further improved in the p-CuI/n-SZTO, the I_F/I_R is likely to be enhanced more. Finally, in Table 1, to illustrate a direction of future applications, we have also listed several recent cases where the photo responsivity has been tested in the transparent pn diode made of the p-CuI. Based on these recent related studies, it is expected that flexible, optically transparent, cheap UV photodetectors can be fabricated by the *p*-CuI/*n*-SZTO diode.

Table 1. Summary of diode parameters for various different pn junctions, consisting of the p-type CuI.

pn Diode	Current Rectification Ratio I _F /I _R	Saturation Current (A) Is	Ideality Factor η	Series Resistance (Ω) Rs	Parallel Resistance (Ω) $R_{ m P}$	Responsivity (Wavelength) (mA W ⁻¹)
pc-CuI/epi-ZnO [2]	$2 \times 10^7 \pm 2 \text{ V}$	1.3×10^{-11}	1.7	2.9×10^{2}	>10 ¹²	-
pc-CuI/epi-ZnO [2]	$4 \times 10^7 \pm 2 \text{ V}$	6.2×10^{-15}	1.6	2.0×10^{2}	>10 ¹²	-
pc-CuI/epi-ZnO [2]	$2 \times 10^7 \pm 2 \text{ V}$	3.2×10^{-13}	1.8	2.5×10^{2}	>10 ¹²	-
epi-CuI/epi-ZnO [11]	$2\times10^9\pm2~\mathrm{V}$	1.1×10^{-12}	1.7	1.7×10^{2}	3×10^{12}	-
pc-CuI/epi-BaSnO _{3-δ} [12]	$7 \times 10^5 \pm 2 \text{ V}$	9.9×10^{-13}	1.5	$\sim 5.5 \times 10^2$	2 × 10 ⁹	-
pc-CuI/a-InGaZnO [3]	$6\times10^6\pm2~\mathrm{V}$	-	1.6	2.0×10^{2}	-	0.3 (365 nm)
pc-CuI _{1-x} Br _x /a-InGaZnO [10]	$\sim 2 \times 10^9 \pm 1.5 \text{ V}$	$\sim 2 \times 10^{-12}$	1.9	-	-	-
np-CuI/sc-CsPbBr ₃ [9]	$3 \times 10^2 \pm 2 \text{ V}$	-	-	-	-	1.4 (540 nm)
pc-CuI/sc-Ga ₂ O ₃ [19]	$6 \times 10^3 \pm 2 \text{ V}$	-	3.7	-	-	2.49 (254 nm)
pc-CuI(20 nm)/a-SiZnSnO (this work)	$2 \times 10^6 \pm 2 \text{ V}$	2.0×10^{-16}	3.2	1.3×10^5	3×10^{12}	-
pc-CuI(140 nm)/a-SiZnSnO (this work)	$7 \times 10^7 \pm 2 \text{ V}$	0.7×10^{-16}	2.7	3.9×10^3	5×10^{12}	-

^{*} epi: epitaxial film, pc: polycrystalline film, sc: single crystal, a: amorphous, np: nanoparticle.

Figure 5a compares the energy band alignment of several wide bandgap materials, including CuI [2,12], SZTO [13,22], IGZO [8,24], BaSnO₃ [12,25], and ITO [26]. Based on the experimental results from previous reports, the band energies of those materials are aligned at the vacuum energy level $E_{\rm vac} = 0$. The top (red) and bottom (blue) columns present conduction and valance bands, respectively. In order to investigate the energy band diagram of the annealed CuI (140 nm)/SZTO diode shown in Figure 5b, first of all, several energies such as $E_{\rm vac}$, valance band maximum ($E_{\rm v}$), and conduction band minimum ($E_{\rm c}$) are determined from Figure 5a. Subsequently, the Fermi energy level ($E_{\rm F}$) is calculated from the Anderson diode model for heterojunction [27]; various input parameters of valance band maximum $E_{\rm v}$, conduction band minimum $E_{\rm c}$ [2,13], dielectric constant [2,22], and effective masses [22,28] of both CuI and SZTO are adopted from the literature. $E_{\rm g}$ and n of SZTO are estimated from our previous work [13], while $E_{\rm g}$ and p of CuI are obtained in this work. Basic parameters and related references are summarized in Table 2.

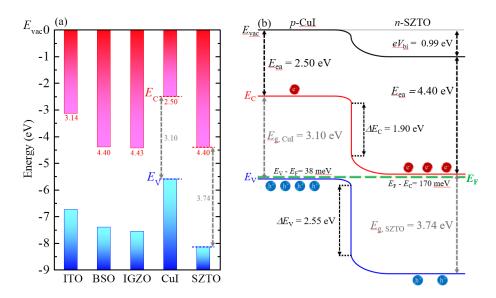


Figure 5. (a) Energy band alignment of several wide bandgap materials, including ITO, BSO, IGZO, CuI, and SZTO. The band energies of those materials are aligned at the vacuum energy level $E_{\text{vac}} = 0$. (b) A proposed energy band diagram of the annealed CuI (140 nm)/SZTO diode based on the Anderson heterojunction diode model, exhibiting the type-II band alignment.

The resultant band diagram is consistent with the type-II band alignment (or staggered gap type), in which E_C of the n-type material is located at the energy window between E_C and E_V of the p-type material. The predicted eV_{bi} , the depletion width of CuI, and the depletion width of SZTO are found as $0.99 \, \text{eV}$, $0.03 \, \text{nm}$, and $37.1 \, \text{nm}$, respectively. The present CuI/SZTO diode is indeed the one-side abrupt junction, of which the depletion region is mostly formed at, in this case, the SZTO layer. It is noted that the n-type depletion width of $37.1 \, \text{nm}$ is larger than the thickness of the SZTO film itself (27 nm). In this condition, an effective negative bias might be formed at the interface, and consequently, a finite forward bias should be required to reduce the electric field and to start the current flow across the pn diode. Consistent with this scenario, relatively high voltages for the current onset in the |j|-V curves have been indeed found at $\approx 0.7 \, \text{V}$ in Figure 2b,d.

Table 2. Input parameters of the Anderson heterojunction diode model for the annealed p-CuI/n-SiZnSnO (SZTO) diode where m_0 is the electron mass.

Film	Bandgap (eV)	Electron Affinity (eV)	Carrier Density (cm ⁻³)	Dielectric Constant	Effective Mass
p-CuI	3.1	^a 2.5	9.4×10^{18}	a5.1	b1.4 <i>m</i> o
n-SZTO	°3.7	°4.4	c6.8 × 10 ¹⁵	d4.75	^d 0.2 <i>m</i> ₀

^a Ref. [2]., ^b Ref. [28]., ^c Ref. [13]., ^d Ref. [22].

4. Conclusions

We have studied the electrical characteristics of transparent p-CuI/n-SiZnSnO (SZTO) heterojunction diodes with a variation of CuI film thicknesses (20 nm and 140 nm), for which thermal evaporation and RF magnetron sputtering techniques have been utilized to deposit the (111) oriented CuI and amorphous SZTO films, respectively. Upon applying a thermal annealing condition of 125 h at 50 °C under N₂ gas atmosphere, we have found that the current rectification ratio (I_F/I_R) is enhanced by ≈25 times up to 6.6 × 10 7 in the thick CuI (140 nm)/SZTO diode due to the improvement of all the diode parameters as

systematically obtained by the curve fitting to the Shockley diode equation. On the other hand, the thin CuI (20 nm)/SZTO diode exhibits a moderate increase of I_F/I_R by ≈ 4 times up to 2.4×10^6 due to the increase of contact resistance of the electrode. Changes of the diode parameters with a variation of the p-CuI film thickness or by the thermal annealing and their physical implications have been discussed in the two kinds of the transparent p-CuI/n-SZTO diode. Based on the comparison with the energy band alignment of various semiconductors, we have proposed the realization of the type-II band diagram in the p-CuI/n-SZTO diode. The present p-CuI/n-SZTO diode can be potentially used as a valuable transparent component in various optoelectronic applications such as a light-emitting diode or a UV photodetector.

Supplementary Materials: The following are available online at www.mdpi.com/2079-4991/11/5/1237/s1, Figure S1: Current-voltage curves for *p*- and *n*-type films to check ohmic contact. Figure S2: Structural properties of CuI films on glass substrates measured by the high-resolution X-ray diffractometer. Figure S3: AFM images of CuI films on glass substrates before and after thermal annealing. Figure S4: Surface topography images of CuI/glass, SZTO/ITO/glass, and CuI/SZTO/ITO/glass measured by AFM. Figure S5: Hall effect results as a function of the thickness of CuI films on glass substrates. Figure S6: The current–voltage and the current density–voltage curves measured by the semiconductor analyzer in the CuI (20 nm)/SZTO diode before and after the N2 annealing.

Author Contributions: J.H.L. carried out diode fabrication, characterization, analysis, and manuscript writing. B.H.L. provided specimens and experimental data. J.K. supported scientific discussions of overall results. M.D. contributed to characterization. K.J. and C.J. collaborated and provided resources. S.Y.L. and K.H.K. supervised and proposed the experiments. All authors have read and agreed to the published version of the manuscript.

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