nanomaterials

MDPI

Article

Mechanisms of Scaling Effect for Emerging Nanoscale Interconnect Materials

Kai Zhao [1,2], Yuanzhao Hu [3,*], Gang Du [4], Yudi Zhao [1] and Junchen Dong [1,*]

[1] Key Laboratory of the Ministry of Education for Optoelectronic Measurement Technology and Instrument, Beijing Information Science and Technology University, Beijing 100101, China; zhaokai@bistu.edu.cn (K.Z.); zhaoyd@bistu.edu.cn (Y.Z.)
[2] Huantian Technology (Kunshan) Electronics Co., Ltd., Kunshan 215300, China
[3] School of Software and Microelectronics, Peking University, Beijing 100871, China
[4] School of Integrated Circuits, Peking University, Beijing 100871, China; gangdu@pku.edu.cn
* Correspondence: huyuanzhao@stu.pku.edu.cn (Y.H.); jcdong@bistu.edu.cn (J.D.)

Abstract: The resistivity of Cu interconnects increases rapidly with continuously scaling down due to scatterings, causing a major challenge for future nodes in M0 and M1 layers. Here, A Boltzmann-transport-equation-based Monte Carlo simulator, including all the major scattering mechanisms of interconnects, is developed for the evaluation of electron transport behaviors. Good agreements between our simulation and the experimental results are achieved for Cu, Ru, Co, and W, from bulk down to 10 nm interconnects. The line resistance values of the four materials with the inclusion of liner and barrier thicknesses are calculated in the same footprint for a fair comparison. The impact of high aspect ratio on resistivity is analyzed for promising buried power rail materials, such as Ru and W. Our results show that grain boundary scattering plays the most important role in nano-scale interconnects, followed by surface roughness and plasma excimer scattering. Surface roughness scattering is the origin of the resistivity decrease for high-aspect-ratio conductive rails. In addition, the grain sizes for the technical nodes of different materials are extracted and the impact of grain size on resistivity is analyzed.

Keywords: Monte Carlo method; scattering mechanism; scaling effect; interconnect; resistivity; grain boundary

Citation: Zhao, K.; Hu, Y.; Du, G.; Zhao, Y.; Dong, J. Mechanisms of Scaling Effect for Emerging Nanoscale Interconnect Materials. *Nanomaterials* **2022**, *12*, 1760. https://doi.org/10.3390/nano12101760

Academic Editors: Andrea Orsini and Stefano Salvatori

Received: 24 March 2022
Accepted: 20 May 2022
Published: 21 May 2022

1. Introduction

Cu has been introduced to replace Al in the back end of line (BEOL) of integrated circuit (IC) fabrication as an interconnect material since 1997. Since then, the aggressive down-scaling of Cu BEOL dimensions has led to exponentially increased resistivity [1], which is referred to as the "size effect" [2]. This effect increases the resistance–capacitance (RC) delay, current-resistance (IR) drop, and power consumption at M0 and M1, and thus deteriorates BEOL's performance [3]. Many efforts have been devoted to improving the BEOL's performance, from metallization to the structures' perspective, respectively [3–10].

A straightforward solution is to replace conventional Cu with new materials to meet the conductivity and reliability requirements. The increasing resistivity derives not only from metallic interconnects but also from their diffusion barriers and adhesion liners [7]. Therefore, alternative materials with less contamination, a larger metal-to-barrier volume ratio, better anti-electromigration properties, and acceptable resistivity are desired to replace Cu at M0 and M1 [1,11–18]. Co [1,11–14], Ru [1,15–17], and W [18] are the three promising candidates to meet the above challenges for their better anti-electromigration properties and lower contamination risks, which makes barrierless metallization possible [11].

Besides metallization optimization, structural innovation is deemed a performance booster as well. A typical attempt is to bury the power rails under shallow trench isolation (STI) and Si substrate, which is referred to as buried power rail (BPR) [8]. For example,

a power distribution network (PDN) with BPR may achieve a 20% smaller area at the same technology node [10]. In the cases of front-side with buried power rails (FS-BPR), the power rails usually have larger aspect ratios (ARs) to lower their resistivity due to the limitation in the width direction. Abnormal ARs impact the internal grain size and thus affect the resistivity.

There are several theoretical studies with ab initio approaches to explain the resistivity-raising phenomena. However, treating electron transport as one-dimensional coherent scattering processes is rather computationally extensive for interconnect simulations. Simplifications must be made to make this approach practical. For example, normalized full-band relaxation time approximation for the linearized Boltzmann transport equation (BTE) [19] is used to derive the scattering rate in a density-functional-theory (DFT) calculation for metal resistivity [20]. First-principles predictions can be used to determine the product of the bulk resistivity times the bulk electron mean-free-path without calculating the electron scattering explicitly [21,22]. In this approximation, the metal wire resistivity is analytically predicted from the approximate forms of the classical Fuchs and Sondheimer (FS) [23,24] and Mayadas and Shatzkes (MS) [25,26] models. The aforementioned two approaches are all with less rigorous simplifications either in scattering terms or in the transport process.

In the deca-nanometer region, the drift diffusion (DD) approach no longer meets the accuracy requirements in the state-of-art technology nodes. Solving BTE under a semiclassical frame is the most appropriate way to investigate carrier transport behaviors in semiconductors and metals because it may include various scattering mechanisms explicitly instead of a relaxation time approximation at acceptable computational costs. Unfortunately, unlike the BTE approach, which has been widely applied in semiconductor device simulation, its applications in promising M0, M1, and BPR metallic lines with explicit scattering terms have not been reported yet. In Refs. [27,28], the BTE is solved with a relaxation time approximation to calculate the metallic nanowire resistivity, but the estimations are very rough.

In this paper, the BTE is solved with explicit scattering terms by the Monte Carlo (MC) approach to investigate the electron transport properties in Cu, Ru, Co, and W. Our MC simulator is redeveloped and validated based on our previous work for interconnects [29] and for semiconductors [30]. To extend the simulator down to deca-nanometer range, as well as to include the emerging materials, such as Ru, Co, and W, grain boundary scattering (GBS) and surface roughness scattering (SRS) models are modified and their parameters are calibrated with the experimental results (Section 2). The contribution of major scattering mechanisms for bulk materials is evaluated in Section 3.1. For deca-nanometer linewidth interconnects, the influence of GBS and SRS on resistivity is investigated, and the scaling effect is also elaborated in Section 3.2. Our results demonstrate GBS is the major mechanism of the scaling effect, and grain size has a significant influence on resistivity. Section 3.3 is devoted to evaluating the BPR materials with different aspect ratios. SRS is demonstrated to be the dominating mechanism for the resistivity drop in high-aspect-ratio rails.

2. Simulation Method and Scattering Mechanisms

Solving the BTE without using the relaxation time approximation [27,28] is a tough job. There are mainly two technical genres to solve it, namely deterministic methods [31–33] and the Monte Carlo approach [34,35]. Solving the BTE deterministically is advantageous to implement the Schrödinger equation (SE), Poisson equation (PE), and BTE self-consistent iterations in semiconductor device simulations; however, it has not been applied to the interconnect for the following reasons: (a) the SE-PE-BTE self-consistent iterative solver is very time-consuming and program-extensive; (b) the linewidth of interconnects is usually one order of magnitude larger than the channel thickness in FinFETs or ultra-thin-body devices, and, therefore, the quantum confinement effect in metallic lines is less conspicuous for the linewidth thicker than 6–8 monolayers [36]. For a typical linewidth of deca-nanometer scale, the Monte Carlo approach is the ideal solution to solve the BTE.

In our Monte Carlo method, the electron transport process is divided into free flight and scattering mechanisms, which occur alternatively. Numerous artificial particles, which act like electrons in the semiclassical frame, are planted into the simulated structure to experience the free flight and scattering processes. Stochastic numbers are used to determine which process or scattering event will happen. After the convergence, all macroscopic quantities, such as density and current, can be generated statistically. Five major scattering mechanisms are considered in our MC simulator, including acoustic phonon scattering (APS), electron to electron scattering (EES), plasma excimer scattering (PES), grain boundary scattering, and surface roughness scattering. The maximum time step will be determined as 2×10^4 to achieve a balance between time consumption and simulation accuracy. Each simulation task requires roughly 4 GB of memory and takes about 48 h at AMD (Santa Clara, CA, USA) Ryzen ^{TM} 4800H processors.

Considering the average electron energy is several orders of magnitude higher than that of acoustic phonons under high electric fields, APS can be regarded as an elastic process approximately with a scattering rate for both absorption and emission processes [34]:

$$\lambda_{APS} = \frac{\sqrt{2} m^{\frac{3}{2}} \Xi^2 k_B T}{\pi \hbar^4 \rho v_s^2} \epsilon^{\frac{1}{2}} \tag{1}$$

where m is the effective mass, Ξ the acoustic deformation potential, k_B the Boltzmann constant, T the lattice temperature, $\hbar$ the reduced Planck constant, ρ the density, and v_S the speed of sound in solids, and ϵ the initial energy. The effective mass of the four materials is extracted from the reported band structure, respectively [37–40].

Collisions between free electrons in metals redistribute their energy and momentum, but the total energy and momentum remain the same statistically. This Coulomb-potential-caused elastic scattering can be expressed as follows [41]:

$$\lambda_{EES} = \frac{e^2 m n}{4\sqrt{2}\pi \hbar \varepsilon_h N_i} \sum_{\boldsymbol{k}} \frac{|\boldsymbol{k} - \boldsymbol{k}_0|}{(|\boldsymbol{k} - \boldsymbol{k}_0| + \beta^2)\beta^2} \tag{2}$$

where n is the electron concentration, N_i the total number of the involved scattering electrons, ε_h the high-frequency dielectric constant, $\boldsymbol{k}$ the final state wave vector, $\boldsymbol{k_0}$ the initial wave vector, and β the reciprocal of Debye's length.

Besides EES, the fluctuation of local electron concentration will cause a rapid change in the electron distribution proportionally. This fluctuation-induced scattering is referred to as plasma excimer scattering. For PES with the total number of the involved scattering electrons N_i and fluctuation frequency ω_p, the scattering rate can be expressed as:

$$\lambda_{PES} = \frac{e^2 m^{\frac{1}{2}} \omega_p}{4\sqrt{2}\pi \hbar \varepsilon_h \epsilon^{\frac{1}{2}}} \left(N_i + \frac{1}{2} \mp \frac{1}{2} \right) \ln \left| \frac{\epsilon'^{\frac{1}{2}} + \epsilon^{\frac{1}{2}}}{\epsilon'^{\frac{1}{2}} - \epsilon^{\frac{1}{2}}} \right| \tag{3}$$

Grain boundaries in conductive materials are becoming a major roadblock for electrons to transit through interconnects as the linewidth scales down to the electron mean-free-path region [7,25]. To simulate the grain boundary scattering in metal lines, a Sinc function is employed to reproduce the barrier potential, and, thus, the scattering rate can be written as:

$$\lambda_{GBS} = \frac{\sqrt{2} m^{\frac{3}{2}} V P\left(sinc^2(x - x_i)\right)}{\pi \hbar^4} \left(\epsilon \mp \hbar \omega_g\right)^{-\frac{1}{2}} \tag{4}$$

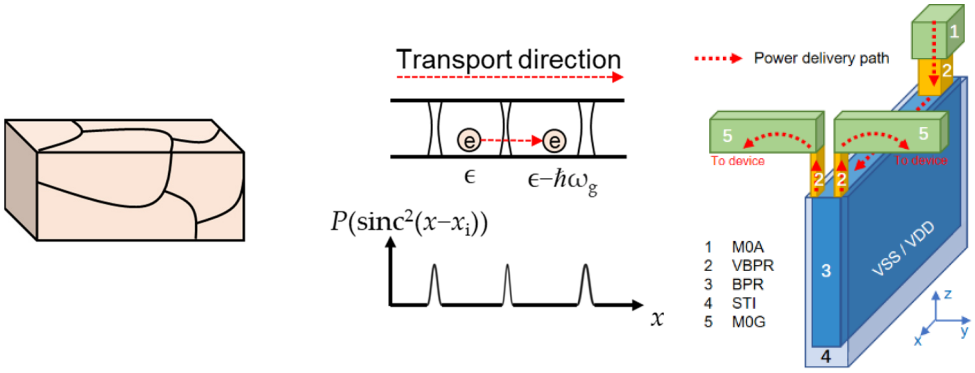
where P, calibrated to 0.1 eV, is the barrier potential amplitude, m the effective mass, V the volume, and x_i the position of the grain boundary. Here, we let $x_i = i \times a + (i - 1) \times r$, where r, a random number between 10^{-9} and 10^{-8}, represents the thickness of the grain boundary, and a the grain size. The adoption of the Sinc^2 function rather than the δ function can avoid numerical issues.

Metal surface roughness has a strong influence on interconnect resistivity by changing the electron momentum during SRS [23]. In our program, a specular parameter [23,42] and a roughness coefficient [23,42] are employed to characterize the surface shape, and, thus, the scattering rate is:

$$\lambda_{SRS} = \frac{2\pi m(1-\mu)^2\sigma^2}{\hbar^3}\left(\frac{e^2}{\varepsilon_h}\right)^2\left(\frac{N_s}{2}\right)^2\frac{1}{\pi}\int_0^{\pi} r(e^{\frac{q^2\Lambda^2}{4}})(1-\cos\theta)d\theta \quad (5)$$

where μ is the specular parameter between irreflexive ($\mu = 0$) and specular ($\mu = 1$) surface scattering based on the Fuchs–Sondheimer model [23], σ^2 the roughness coefficient of the surface, and N_S the sheet electron density calculated from the density of states and Fermi–Dirac distribution function. In the electron energy-related integration core, $q = |\boldsymbol{k'} - \boldsymbol{k}|$ is the wave vector difference between initial and final states, r a random number between 0.1 and 1, θ the scattering angle, and Λ the correlation length of surface roughness.

The APS, EES, and PES rates are bulk-like and are assumed to be linewidth-independent. Schematic diagrams of our simulated structure are shown in Figure 1. A phonon emission process caused by grain boundaries is illustrated in Figure 1b, as well as the potential of grain boundaries.



(**a**) (**b**) (**c**)

Figure 1. Schematic diagrams of simulated structures: (**a**) the simulated bulk-like structure and its grain boundaries, (**b**) the nanoscale interconnect grain boundaries and their Sinc function potential barriers, and (**c**) a schematic diagram of FS-BPR (front-side BPR) structure and power delivery path. In (**b**), an electron travels across a grain boundary and emits a phonon with energy $\hbar\omega_g$ to lattice. In (**c**), electric power distributes along 1. M0A (metal contact to active), 2. VBPR (via to the BPR), 3. BPR, and 5. M0G (metal contact to gate). A BPR is surrounded by STI and buried partially in STI oxide and Si substrate.

3. Results and Discussion

3.1. Analysis of Bulk Materials

For the validation of our program and the calibration of the parameters, electron transport in bulk materials is simulated with the presence of APS, EES, and PES. In bulk materials, the grain size is approximately two orders of magnitude larger than the thickness of the grain boundaries [43,44]. Therefore, GBS can be ignored because the electron mean-free-path is much smaller than the typical grain size. In addition, interconnect linewidths are much larger than the electron mean-free-path in metals; therefore, the influence of SRS can be neglected. Figure 2 depicts the convergence behavior of the bulk average resistivity of the four metals at room temperature. The simulation of all four materials experiences drastic fluctuations in the first 6×10^3 steps due to a poor initial guess of the electron distribution function, and then all converge steadily. A comparison between our simulation results and experimental bulk resistivities [45] is shown in Table 1. Good agreements are achieved for all four materials at room temperature with calibrated scattering parameters.

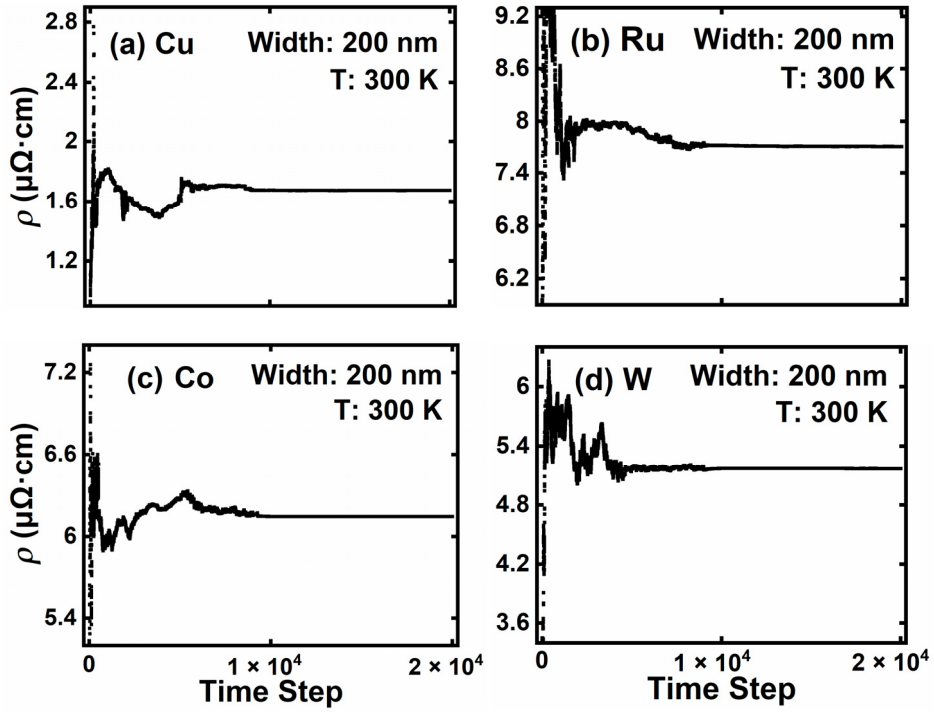


Figure 2. Bulk resistivity of (**a**) Cu, (**b**) Ru, (**c**) Co, and (**d**) W interconnect with the increase in time steps.

Table 1. Comparison between simulation and experiment at 300 K.

Material	Simulation (μΩ·cm)	Experiment (μΩ·cm)
Cu	1.676	1.678
W	5.168	5.28
Co	6.145	6.2
Ru	7.71	7.8

To evaluate the impact of each scattering mechanism on electron transport, the scattering rate of electron energy ranging up to 0.3 eV is taken into account, as shown in Figure 3. As the electron energy increases from 0.013 eV, the scattering rate of EES and PES increase sharply first and almost remain the same at higher energy levels. Although the APS rate keeps increasing with energy, it is still at least an order of magnitude smaller than the other three. The scattering rate of PES is about 35 times larger than that of EES and plays a key role in bulk materials among the four scattering mechanisms.

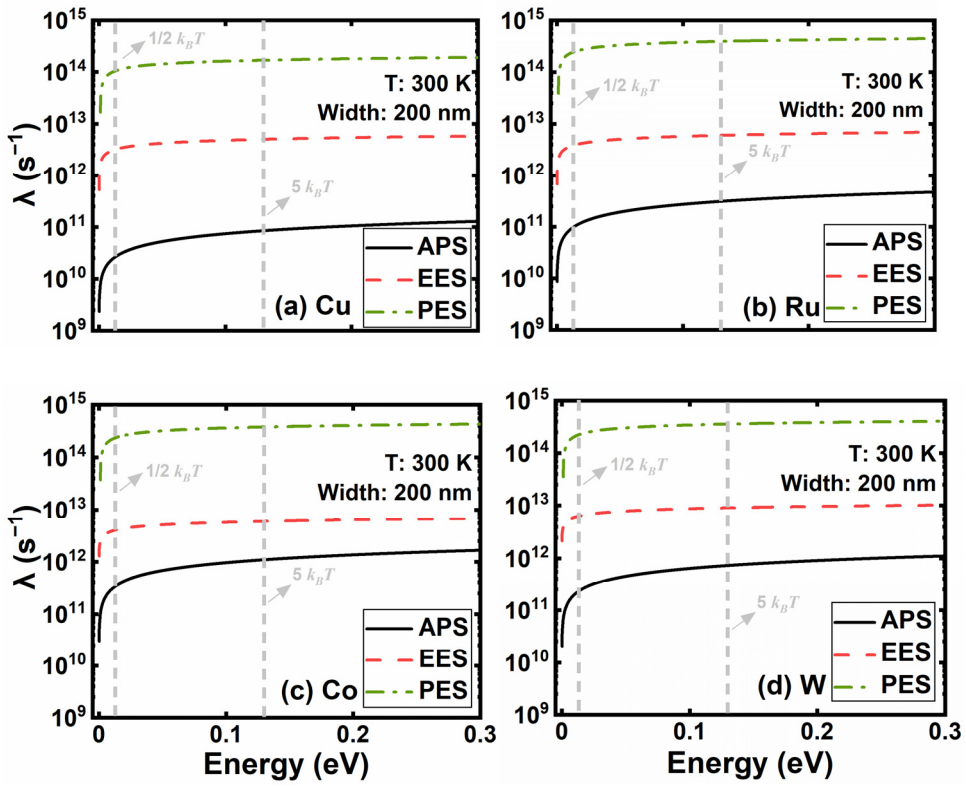


Figure 3. The scattering rates of bulk (**a**) Cu, (**b**) Ru, (**c**) Co, and (**d**) W with the electron energy ranging up to 0.3 eV.

3.2. Evaluation of the Scaling Effect

Electron scatterings at rough surfaces and grain boundaries are major causes of the resistivity increase in nanoscale interconnects. To evaluate the impacts of GBS and SRS, we further simulated a series of deca-nanometer metal lines, with their width varying from 48 nm down to 10 nm. According to the International Roadmap for Devices and Systems (IRDS) [46], the M0 layer should be at least 14 nm wide to preserve sufficient logic interconnect space for the middle end of line (MEOL). Hence, the minimum linewidth of the M0 layer is set to be 10 nm in this paper. The scattering rates of APS, EES, and PES are assumed to be linewidth-independent, while those of GBS and SRS are linewidth-related. Therefore, the scattering mechanisms for resistivity evaluation can be divided into these two cases.

Assuming electrons mainly undergo diffusive scattering processes at interconnect surfaces, μ, σ^2, and Λ in Equations (5) and (6) can be set to 0.2, 5, and 0.6. Figure 4 depicts the resistivity of each metal, with a linewidth ranging from 48 down to 10 nm at room temperature. The average grain sizes for simulations from Figures 4–6 are listed in Table 2.

Table 2. Average grain sizes for Cu, Ru, Co, and W for simulations from Figures 4–6.

Width (nm)	10	12	16	20	24	26	36	40	48
Average GS (nm)	9.5	11.5	15	19	24	26	36	40	48

The cases without SRS or GBS are simulated in contrast to the case with all the scatterings to evaluate the impact of the two linewidth-dependent mechanisms. As the linewidth scales down, both GBS and SRS influence resistivity significantly. The absence of GBS results in much lower resistivities compared to the cases without SRS, suggesting GBS is the primary cause of the scaling effect, followed by SRS. For the case with all the scattering mechanisms, W shows the most dramatic resistivity rise and Ru the least.

Although Cu shows the lowest resistivity at 10 nm, its scaling effect is one of the worst. Among the four materials, the scaling effect has the least impact on Ru.

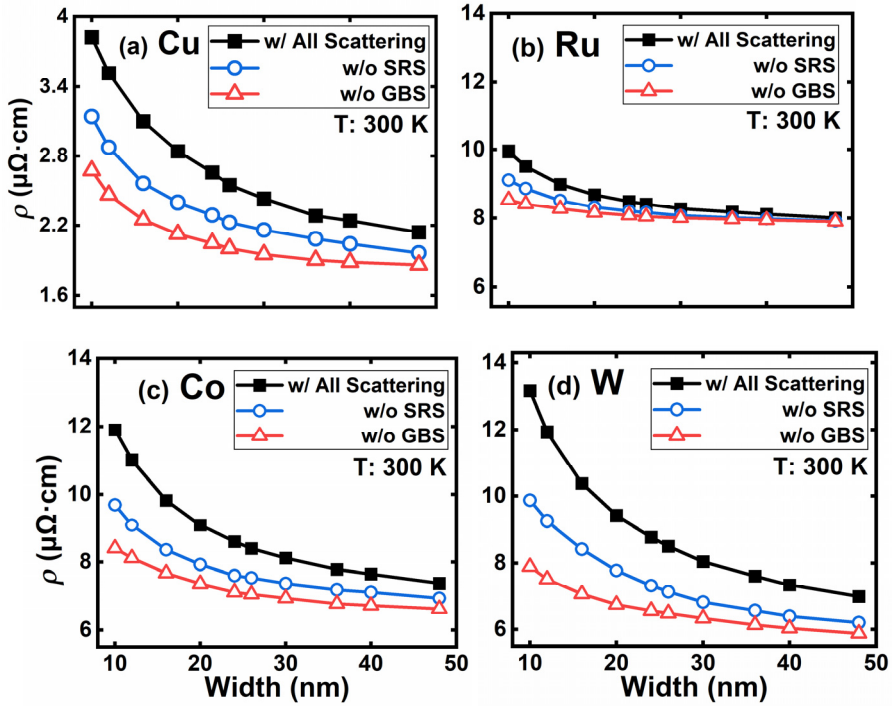


Figure 4. The resistivity of (**a**) Cu, (**b**) Ru, (**c**) Co, and (**d**) W interconnects with a linewidth ranging from 10 to 48 nm.

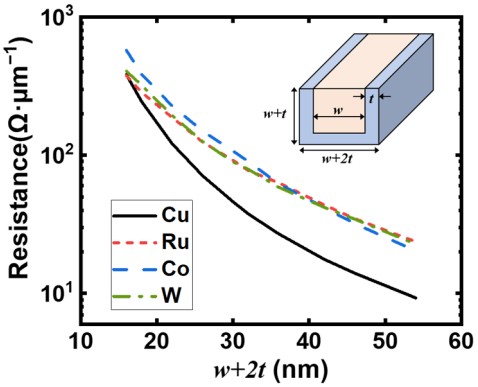


Figure 5. The calculated resistance per μm with liner thickness t^{Cu} = 3 nm, t^{Ru} = 0.3 nm, t^{Co} = 1 nm, and t^{W} = 0 nm. The inset demonstrates the structure of interconnect with the presence of liners and barriers. w is the width of the metallic lines, t the thickness of liner and barrier. All scattering mechanisms are included.

The actual interconnects' resistance depends not only on their resistivity but also on the volume occupied by the adhesion and wetting layers [47]. We hereby simulate the line resistance for the four materials with the presence of liners and barriers in Figure 5. Unlike the references [21,22] calculating the resistance analytically from the product of the bulk resistivity times the bulk electron mean-free-path, we implement all the scattering mechanisms inherently in the BTE by the Monte Carlo processes. The aspect ratio of the calculated interconnects is 1, and the state-of-the-art liner and barrier thickness is assumed for a fair comparison. The liner thickness for Cu, Ru, and Co are 3 nm, 0.3 nm, and 1 nm, respectively [48–50]. W has been reported for its linerless deposition, so no liner is added in this calculation [51]. For large linewidths, Cu still offers lower line resistance than its

alternatives, as is expected due to its much lower resistivity and higher copper proportion in the total volume. However, with the decrease in linewidth ($w + 2t$), the copper proportion reduces rapidly and its resistance is finally analogous to the other three. As for Ru, Co, and W, although their resistivities show different trends with respect to linewidth, their resistance is surprisingly analogous to all the linewidths. Below about 20 nm, the superiority of Cu in resistance is significantly weakened, and anti-electromigration properties become a major concern in this region.

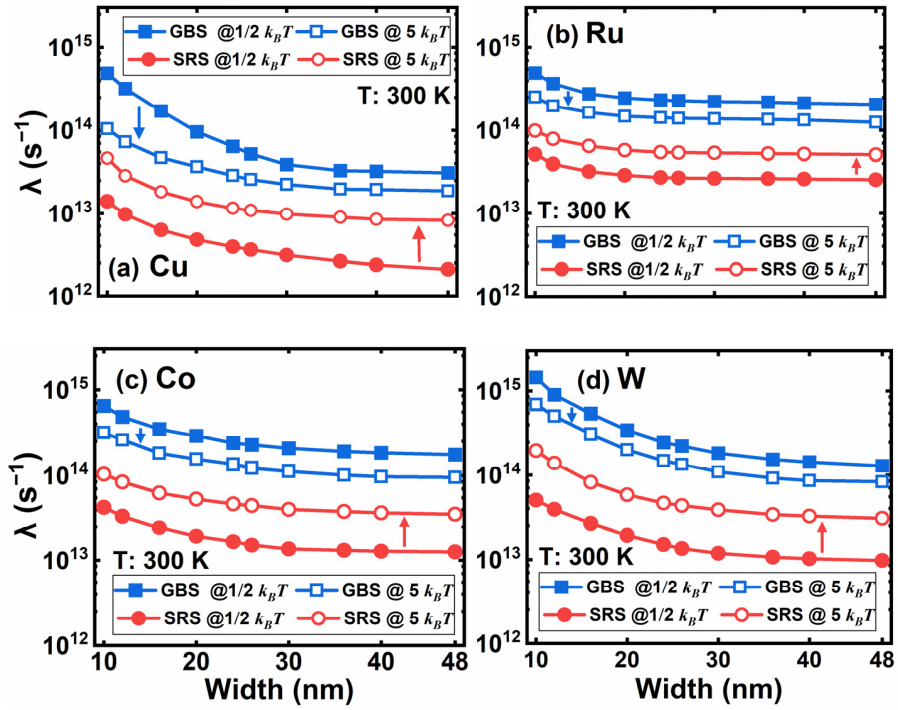


Figure 6. The scattering rate of GB and SR in (**a**) Cu, (**b**) Ru, (**c**) Co, and (**d**) W lines at electron energy levels of $k_BT/2$ and 5 k_BT. The linewidth varies from 48 down to 10 nm.

To further explore the origin of the scaling effect, we extracted the scattering rate of GBS and SRS with respect to electron energy in Figure 6. Considering most electrons are populated at lower energy states, the scattering rates of GBS and SRS at $k_BT/2$ and 5 k_BT are representative. In contrast to the four scattering mechanisms in Figure 3, the scattering rates of grain boundaries and surface roughness increase dramatically at lower energy levels and surpass those four scattering mechanisms at the energy level of k_BT approximately.

It is worth noting that the GBS rate decreases with energy, and the SRS rate increases. The SRS rate is still one order of magnitude lower than the GBS rate at 5 k_BT, where the electron distribution starts to be scarce. The reason is that electrons with higher energy are prone to be less affected by the potential energy of grain boundaries; however, the probability of a collision between hot electrons and the surface increases notably. Therefore, the scattering rate of GBS has larger magnitudes than SRS for the four metals and dominates the resistivity rises as linewidth scaling. As linewidth shrinks from 24 to 10 nm, the GBS and SRS rates at $k_BT/2$ of W increase the most among the four materials, while the rates of Ru are much better, followed by Co. Consequently, in terms of the scaling effect, Ru is a good candidate for replacing Cu in M0 and M1, followed by Co.

A comparison between the simulated resistivity and experimental data [22,52] at different temperatures is presented in Figure 7a. Good agreements between the simulation and available measured data at 273 K and 298 K are achieved, indicating our program is accurate for different metals at various temperatures at the deca-nanometer scale. Among the four materials, the temperature dependence of Cu is the least significant, followed by Ru. W is very sensitive to the change in temperature and linewidth.

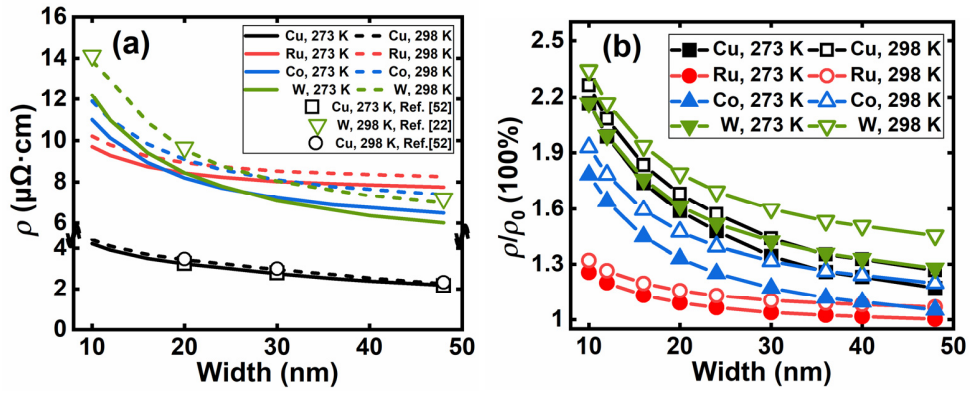


Figure 7. (**a**) Comparison of simulated resistivity and measured data at 273 and 298 K; (**b**) the ratio of the nanoscale interconnects resistivity ρ to bulk resistivity ρ_0 as width scaling down at 273 and 298 K.

Figure 7b illustrates the relationship between linewidth and ρ/ρ_0 at different temperatures, where ρ_0 is the bulk resistivity. W and Cu are both affected remarkably by scaling, while Ru is the least. Therefore, from the perspective of resistivity, Ru is a good alternative to Cu as a BEOL metallization material. However, the choice of M0, M1, and BPR metal is a complex compromise between resistivity, electromigration, contamination, etc.

The grain size determines the behavior of GBS in nanocrystalline metals. In this work, the grain sizes are extracted from the experimental results [53–58]. The grain sizes of those reported epitaxial films are limited by their thickness, and the electron transport behaviors between electrodes are quasi-one-dimensional. Figure 8 presents the experimental resistivities and our simulation results with the corresponding fitted grain sizes of the four metals. The dashed lines are simulation results with the assumption of a full diffusive surface scattering ($\mu = 0$). Very good agreements with the experimental data [36–41] are achieved for all four materials. The average grain sizes extracted from the fitted curves are listed in Table 3. Two sets of grain size (GS) curves for Cu, Ru, and Co correspond to two different process parameters, respectively.

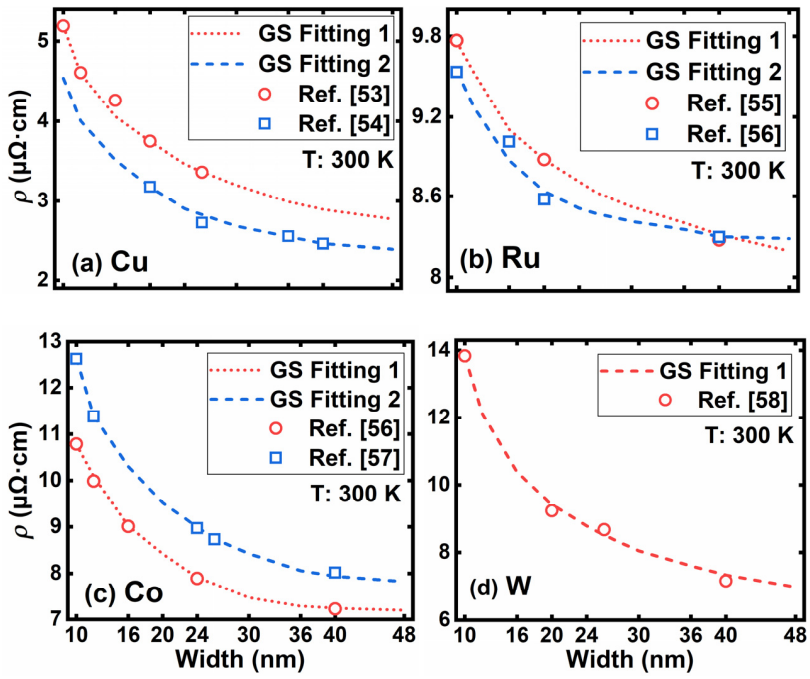


Figure 8. The fitting results of (**a**) Cu, (**b**) Ru, (**c**) Co, and (**d**) W with linewidth scaled from 48 nm to 10 nm. Hollow dots represent the experimental data, and the dashed lines are the simulation results with fitted grain sizes.

Table 3. Extracted grain sizes for Cu, Ru, Co, and W from experimental data.

Width (nm)	Grain Size (nm)						
	Cu^{GS1}	Cu^{GS2}	Ru^{GS1}	Ru^{GS2}	Co^{GS1}	Co^{GS2}	W^{GS1}
10	8.7		8.3	9.1	10	8.7	8.8
12	10.3				12	10.5	
16	14.1			15.6	14.5		
20	17.9	18.6	18.5	19.7			18.8
24					22	19	
26	24	25				23	25.1
36		35					
40		38	37	37.5	40	35	38

3.3. Evaluation of BPR Materials

Ru and W are the two promising materials for BPR [8–10] for their high thermal budgets, relatively low resistance, and superior anti-electromigration properties. It has been reported that high-aspect-ratio (AR) Ru BPR demonstrates excellent resistivity reduction [8]. In this section, we will focus on the impact of AR from the perspective of resistivity and its physical mechanisms behind.

The electron transport behavior in BPR is slightly different from BEOL, particularly for SRS. A schematic diagram of FS-BPR is shown in Figure 1c. A remarkable feature of BPR is its high AR, which is designed to enable further scaling by burying under the transistors to replace the above MEOL, and to boost performance by reducing the resistance and I-R drop of the power rail. The grain size is usually determined by the shorter edge of the rail, and, thus, a higher AR cannot alleviate the adverse impact of GBS on resistivity. Meanwhile, considering the VBPRs connecting the BPR to M0A and M0G from the top surface, SRS occurs mainly at the top, upper-left, and upper-right STI-BPR surfaces. Therefore, the SRS rate in BPR can be modified as follows:

$$\lambda_{SRS} = \frac{2\pi m(1-\mu)^3\sigma^2 d}{\hbar^3 n\sqrt{(1-r)L}}\left(\frac{e^2}{\varepsilon_h}\right)^2\left(\frac{N_s}{2}\right)^2\frac{1}{\pi}\int_0^{\pi} r\left(e^{\frac{q^2\Lambda^2}{4}}\right)(1-cos\theta)d\theta \quad (6)$$

where n is the aspect ratio, d the electron-mean-path of the studied material, and L the height of the BPR structure in the z-direction. In this paper, the electron mean-free-paths are chosen as 39.9 nm, 6.59 nm, 7.77 nm, and 11.2 nm for Cu, Ru, Co, and W, respectively [45].

The resistivity of Ru and W with linewidth = 18 nm and ARs ranging from 1 to 7 are simulated in Figure 9. A bulk resistivity ρ_0 is taken as a reference, and the ratio of simulated BPR resistivity ρ to ρ_0 is extracted to evaluate the scaling effect of BPR in Figure 9a. Ru demonstrates a superior scaling nature at all ARs, even for GS = 9 nm. However, the resistivity of W with GS = 18 nm is almost two times larger than ρ_0, and even exceeds three times for the case with GS = 9 nm. Grain size shows a significant influence on resistivity for both materials. In Figure 9b, the resistance of the two BPR candidates is calculated for different ARs. Considering the conductor volume is proportional to the AR with the same footprint (w + 2t = 18 nm), we use the AR times resistance product for a more intuitive comparison. The liner thickness of Ru is 0.3 nm, and W is linerless. The AR times resistance product benefits from the AR increase with both GS = 9 and 18 nm, which means the total BPR resistance may drop significantly. The key for a smaller BPR IR-drop is to keep its GS as large as possible.

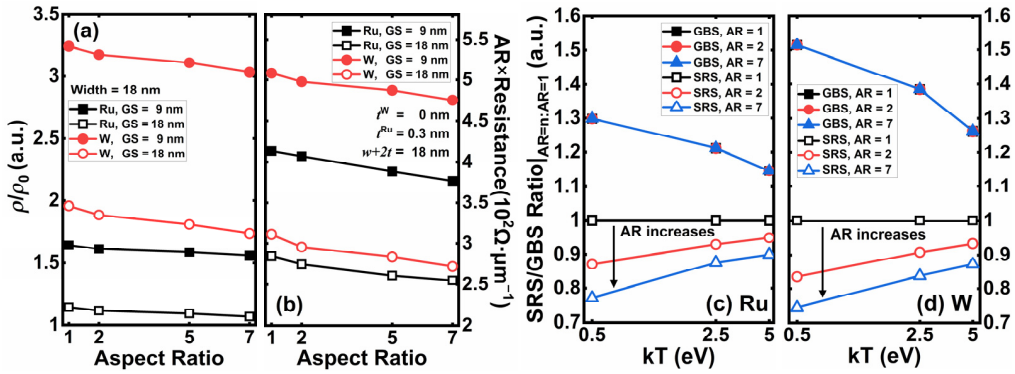


Figure 9. The impact of AR for Ru and W with a linewidth of 18 nm: (**a**) the ratio of the deca-nanoscale resistivity ρ to bulk resistivity ρ_0 with GS = 9 and 18 nm; (**b**) the product of AR times resistance of Ru and W with GS = 9 and 18 nm; the scattering rate ratio of AR = n to AR = 1 as energy increases for (**c**) Ru and (**d**) W.

Figure 9c,d shows the $AR_{GBS} = n/AR_{GBS} = 1$ and $AR_{SRS} = n/AR_{SRS} = 1$ (n = 1, 2, 7) for Ru and W in the energy space. As expected, the GBS rates are independent of AR for both Ru and W because GS is only determined by the short edge of the rail. However, the SRS rates are associated with the AR due to the shift in the surface area to volume ratio. A high AR reduces the SRS rates significantly at lower energy states, where the electron concentration is higher.

For high AR cases (e.g., AR = 7), the upper and lower surfaces are far enough apart and are separated by several grains. Electrons with lower energy can hardly cross n grains from one short edge and are affected by the opposite short edge's SRS and, thus, behave like transporting in a three-surface rail. Only those electrons with rather high energy may have a chance to cross the vertical direction of the BPR and reach the opposite surface. In other words, the rail can be regarded as a four-surface conductor only for very hot electrons. That is the reason why $AR_{SRS} = n/AR_{SRS} = 1$ are both approximately 3/4 at low energy levels and converge to 1 as the energy increases for both Ru and W.

To further evaluate the influence of GS on resistivity, we select 12 and 40 nm linewidth and vary the GS down to half-linewidth, respectively, in Figure 10. As the GS shrinks, the resistivity increases significantly, especially for smaller linewidth with smaller GS. With the decrease in GS, electrons face, accordingly, increased grain boundary barriers and lose energy during each GBS. Considering that the other scattering mechanisms (APS, EES, PES, and SRS) of Cu are relatively lower than those of Ru, W, and Co, the resistivity rise of Cu with a 12 nm linewidth and small GS are most notable. Among the four materials, the impact of GS on Ru is the least and W is the most, which is consistent with their scattering rate in Figure 6. Consequently, Ru is the most promising metal to replace Cu for further scaling. To achieve an ideal resistivity at future nodes, Ru metallization should be optimized for a larger GS and high AR.

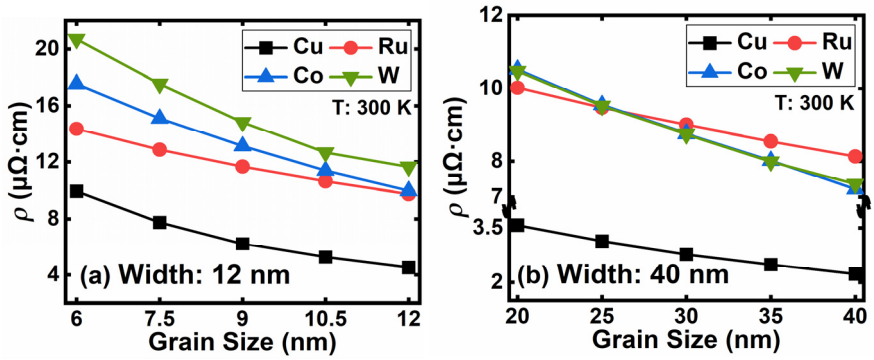


Figure 10. The resistivity of Cu, Ru, Co, and W at different GS with (**a**) 12 nm and (**b**) 40 nm linewidth.

4. Conclusions

The scaling effect of nanoscale MEOL and BPR interconnects was investigated by a self-developed BTE simulator based on the Monte Carlo approach. All the major scattering mechanisms, including APS, EES, PES, SRS, and GBS, were implemented in the simulator explicitly to capture the origin of resistivity of Cu, Ru, Co, and W. Good agreements of bulk resistivity between our calculations and experimental results were achieved. For nanoscale interconnects, GBS is the dominating mechanism of resistivity rises, followed by SRS and PES. The grain sizes of the reported experiments were extracted by our program for a better understanding of the grain-size-dependent resistivity for further scaling. The impact of AR was examined for the BPR application, and SRS was found to be the major cause of the resistivity decrease. The high-aspect-ratio SRS rates reduce by about 1/4 for the low energy states because high-AR rails act like a three-surface material for electron transport. The resistance with consideration of liners and barriers was simulated numerically instead of the previously reported analytical approximations. Ru, Co, and W demonstrate similar resistances at the deca-nanometer scale, whereas the Cu resistance is comparable to the other three below 20 nm linewidth due to its thicker liner requirements, although it exhibits much lower resistivity from bulk to nanoscale linewidth. Ru is the most promising MEOL and BPR metallization solution to replace Cu because of its better anti-electromigration properties, thinner liner requirement, and relatively lower resistivity. The key point to depressing the IR-drop of the power delivery network is to optimize the metallization process and AR to achieve larger grain sizes.

Author Contributions: Conceptualization, K.Z. and G.D.; methodology, K.Z. and Y.H.; software, Y.H.; validation, K.Z., G.D., Y.Z. and J.D.; formal analysis, K.Z. and Y.H.; writing—original draft preparation, K.Z. and Y.H.; writing—review and editing, K.Z., G.D., Y.Z. and J.D.; supervision, G.D.; funding acquisition, K.Z. and Y.Z. All authors have read and agreed to the published version of the manuscript.

Funding: This research was funded by the National Natural Science Foundation of China (Grant No. 62074017, 62004005), and Science and Technology Project of Beijing Municipal Education Commission (Grant No. KM202111232016).

Data Availability Statement: The data presented in this study are available on request from the corresponding authors.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Edelstein, D.; Heidenreich, J.; Goldblatt, R.; Cote, W.; Uzoh, C.; Lustig, N.; Roper, P.; McDevitt, T.; Motsiff, W.; Simon, A. Full Copper Wiring in a Sub-0.25/Spl Mu/m CMOS ULSI Technology. In Proceedings of the International Electron Devices Meeting, IEDM Technical Digest, Washington, DC, USA, 7–10 December 1997.
2. Kapur, P.; McVittie, J.P.; Saraswat, K.C. Technology and Reliability Constrained Future Copper Interconnects. I. Resistance Modeling. *IEEE Trans. Electron Devices* **2002**, *49*, 590–597. [CrossRef]
3. Koike, J.; Haneda, M.; Iijima, J.; Wada, M. Cu alloy metallization for self-forming barrier process. In Proceedings of the International Interconnect Technology Conference, Burlingame, CA, USA, 5–7 June 2006.
4. Ogawa, E.T.; Lee, K.D.; Blaschke, V.A.; Ho, P.S. Electromigration reliability issues in dual-damascene Cu interconnections. *IEEE Trans. Reliab.* **2002**, *51*, 403–419. [CrossRef]
5. Hau-Riege, C.S.; Thompson, C.V. Electromigration in Cu Interconnects with Very Different Grain Structures. *Appl. Phys. Lett.* **2001**, *78*, 3451–3453. [CrossRef]
6. He, M.; Zhang, X.; Nogami, T.; Lin, X.; Kelly, J.; Kim, H.; Spooner, T.; Edelstein, D.; Zhao, L. Mechanism of Co Liner as Enhancement Layer for Cu Interconnect Gap-Fill. *J. Electrochem. Soc.* **2013**, *160*, D3040. [CrossRef]
7. Chen, F.; Gardner, D. Influence of Line Dimensions on the Resistance of Cu Interconnections. *IEEE Electron Device Lett.* **1998**, *19*, 508–510. [CrossRef]
8. Gupta, A.; Kundu, S.; Teugels, L.; Bommels, J.; Adelmann, C.; Heylen, N.; Jamieson, G.; Pedreira, O.V.; Ciofi, I.; Chava, B.; et al. High-Aspect-Ratio Ruthenium Lines for Buried Power Rail. In Proceedings of the 2018 IEEE International Interconnect Technology Conference, Santa Clara, CA, USA, 4–7 June 2018.
9. Ryckaert, J.; Gupta, A.; Jourdain, A.; Chava, B.; Vsan der Plas, G.; Verkest, D.; Beyne, E. Extending the Roadmap beyond 3 nm through System Scaling Boosters: A Case Study on Buried Power Rail and Backside Power Delivery. In Proceedings of the 2019 Electron Devices Technology and Manufacturing Conference, Singapore, 12–15 March 2019.

10. Gupta, A.; Pedreira, O.V.; Arutchelvan, G.; Zahedmanesh, H.; Devriendt, K.; Mertens, H.; Tao, Z.; Ritzenthaler, R.; Wang, S.; Radisic, D.; et al. Buried Power Rail Integration with FinFETs for Ultimate CMOS Scaling. *IEEE Trans. Electron Devices* **2020**, *67*, 5349–5354. [CrossRef]
11. Tu, K.-N. Recent Advances on Electromigration in Very-Large-Scale-Integration of Interconnects. *J. Appl. Phys.* **2003**, *94*, 5451–5473. [CrossRef]
12. Lu, K. Stabilizing Nanostructures in Metals Using Grain and Twin Boundary Architectures. *Nat. Rev. Mater.* **2016**, *1*, 16019. [CrossRef]
13. Adelmann, C.; Wen, L.G.; Peter, A.P.; Siew, Y.K.; Croes, K.; Swerts, J.; Popovici, M.; Sankaran, K.; Pourtois, G.; Van Elshocht, S. Alternative Metals for Advanced Interconnects. In Proceedings of the IEEE International Interconnect Technology Conference, San Jose, CA, USA, 20–23 May 2014.
14. Auth, C.; Aliyarukunju, A.; Asoro, M.; Bergstrom, D.; Bhagwat, V.; Birdsall, J.; Bisnik, N.; Buehler, M.; Chikarmane, V.; Ding, G. A 10 nm High Performance and Low-Power CMOS Technology Featuring 3 Rd Generation FinFET Transistors, Self-Aligned Quad Patterning, Contact over Active Gate and Cobalt Local Interconnects. In Proceedings of the 2017 IEEE International Electron Devices Meeting, San Francisco, CA, USA, 2–6 December 2017.
15. Dutta, S.; Sankaran, K.; Moors, K.; Pourtois, G.; Van Elshocht, S.; Bömmels, J.; Vandervorst, W.; Tőkei, Z.; Adelmann, C. Thickness Dependence of the Resistivity of Platinum-Group Metal Thin Films. *J. Appl. Phys.* **2017**, *122*, 025107. [CrossRef]
16. Zhang, X.; Huang, H.; Patlolla, R.; Wang, W.; Mont, F.W.; Li, J.; Hu, C.-K.; Liniger, E.G.; McLaughlin, P.S.; Labelle, C. Ruthenium Interconnect Resistivity and Reliability at 48 Nm Pitch. In Proceedings of the 2016 IEEE International Interconnect Technology Conference/Advanced Metallization Conference (IITC/AMC), San Jose, CA, USA, 23–26 May 2016.
17. Huynh-Bao, T.; Ryckaert, J.; Tokei, Z.; Mercha, A.; Verkest, D.; Thean, A.V.-Y.; Wambacq, P. Statistical Timing Analysis Considering Device and Interconnect Variability for BEOL Requirements in the 5-Nm Node and Beyond. *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.* **2017**, *25*, 1669–1680. [CrossRef]
18. Choi, D.; Barmak, K. On the Potential of Tungsten as Next-Generation Semiconductor Interconnects. *Electron. Mater. Lett.* **2017**, *13*, 449–456. [CrossRef]
19. Gunst, T.; Markussen, T.; Stokbro, K.; Brandbyge, M. First-Principles Method for Electron-Phonon Coupling and Electron Mobility: Applications to Two-Dimensional Materials. *Phys. Rev. B* **2016**, *93*, 035414. [CrossRef]
20. Philip, T.M.; Lanzillo, N.A.; Gunst, T.; Markussen, T.; Cobb, J.; Aboud, S.; Robison, R.R. First-Principles Evaluation of Fcc Ruthenium for Its Use in Advanced Interconnects. *Phys. Rev. Appl.* **2020**, *13*, 044045. [CrossRef]
21. Gall, D.; Jog, A.; Zhou, T. Narrow Interconnects: The Most Conductive Metals. In Proceedings of the 2020 IEEE International Electron Devices Meeting (IEDM), Online, 12–16 December 2020.
22. Gall, D. The Search for the Most Conductive Metal for Narrow Interconnect Lines. *J. Appl. Phys.* **2020**, *127*, 050901. [CrossRef]
23. Fuchs, K. The Conductivity of Thin Metallic Films According to the Electron Theory of Metals. In *Mathematical Proceedings of the Cambridge Philosophical Society*; Cambridge University Press: Cambridge, UK, 1938; pp. 100–108.
24. Sondheimer, E.H. The Mean Free Path of Electrons in Metals. *Adv. Phys.* **2001**, *50*, 499–537. [CrossRef]
25. Mayadas, A.F.; Shatzkes, M. Electrical-Resistivity Model for Polycrystalline Films: The Case of Arbitrary Reflection at External Surfaces. *Phys. Rev. B* **1970**, *1*, 1382. [CrossRef]
26. Mayadas, A.F.; Shatzkes, M.; Janak, J.F. Electrical Resistivity Model for Polycrystalline Films: The Case of Specular Reflection at External Surfaces. *Appl. Phys. Lett.* **1969**, *14*, 345–347. [CrossRef]
27. Moors, K.; Sorée, B.; Tőkei, Z.; Magnus, W. Resistivity Scaling and Electron Relaxation Times in Metallic Nanowires. *J. Appl. Phys.* **2014**, *116*, 063714. [CrossRef]
28. Moors, K.; Sorée, B.; Magnus, W. Resistivity Scaling in Metallic Thin Films and Nanowires Due to Grain Boundary and Surface Roughness Scattering. *Microelectron. Eng.* **2017**, *167*, 37–41. [CrossRef]
29. Yan, W.Z.; Gang, D.; Feng, K.J.; Yan, L.X.; Ruqi, H. Monte Carlo Simulation of Cu-Resistivity. In Proceedings of the 2008 International Conference on Simulation of Semiconductor Processes and Devices, Hakone, Japan, 9–11 September 2008.
30. Liu, X.; Wei, K.; Yin, L.; Du, G.; Jiang, H.; Zhao, K.; Zeng, L.; Zhang, X. Three Dimemsional Electro-Thermal Coupled Monte Carlo Device Simulation. In Proceedings of the 2014 12th IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT), Guilin, China, 28–31 October 2014.
31. Jin, S.; Hong, S.-M.; Jungemann, C. An Efficient Approach to Include Full-Band Effects in Deterministic Boltzmann Equation Solver Based on High-Order Spherical Harmonics Expansion. *IEEE Trans. Electron Devices* **2011**, *58*, 1287–1294. [CrossRef]
32. Zhao, K.; Hong, S.-M.; Jungemann, C.; Han, R.-Q. Stable Implementation of a Deterministic Multi-Subband Boltzmann Solver for Silicon Double-Gate NMOSFETs. In Proceedings of the 2010 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD), Bologna, Italy, 6–8 September 2010.
33. Di, S.; Zhao, K.; Lu, T.; Du, G.; Liu, X. Investigation of Transient Responses of Nanoscale Transistors by Deterministic Solution of the Time-Dependent BTE. *J. Comput. Electron.* **2016**, *15*, 770–777. [CrossRef]
34. Jacoboni, C.; Reggiani, L. The Monte Carlo Method for the Solution of Charge Transport in Semiconductors with Applications to Covalent Materials. *Rev. Mod. Phys.* **1983**, *55*, 645–705. [CrossRef]
35. Jungemann, C.; Meinerzhagen, B. *Hierarchical Device Simulation: The Monte-Carlo Perspective*; Springer Science & Business Media: New York, NY, USA, 2003.

36. Shikin, A.M.; Adamchuk, V.K. Quantum Confinement Effects in Thin Metal Layers on the Surface of Single Crystals and Their Analysis. *Phys. Solid State* **2008**, *50*, 1170–1185. [CrossRef]
37. Burdick, G.A. Energy Band Structure of Copper. *Phys. Rev.* **1963**, *129*, 138–150. [CrossRef]
38. Bagayoko, D.; Ziegler, A.; Callaway, J. Band Structure of Bcc Cobalt. *Phys. Rev. B* **1983**, *27*, 7046–7049. [CrossRef]
39. Jepsen, O.; Andersen, O.K.; Mackintosh, A.R. Electronic Structure of Hcp Transition Metals. *Phys. Rev. B* **1975**, *12*, 3084–3103. [CrossRef]
40. Mattheiss, L.F. Fermi Surface in Tungsten. *Phys. Rev.* **1965**, *139*, A1893–A1904. [CrossRef]
41. Lugli, P.; Ferry, D.K. Effect of Electron-Electron Scattering on Monte Carlo Studies of Transport in Submicron Semiconductors Devices. *Physica B+C* **1983**, *117*, 251–253. [CrossRef]
42. Yamakawa, S.; Ueno, H.; Taniguchi, K.; Hamaguchi, C.; Miyatsuji, K.; Masaki, K.; Ravaioli, U. Study of Interface Roughness Dependence of Electron Mobility in Si Inversion Layers Using the Monte Carlo Method. *J. Appl. Phys.* **1996**, *79*, 911–916. [CrossRef]
43. Kim, C.-U.; Park, J.; Michael, N.; Gillespie, P.; Augur, R. Study of Electron-Scattering Mechanism in Nanoscale Cu Interconnects. *J. Electron. Mater.* **2003**, *32*, 982–987. [CrossRef]
44. Simões, S.; Calinas, R.; Vieira, M.T.; Vieira, M.F.; Ferreira, P.J. In Situ TEM Study of Grain Growth in Nanocrystalline Copper Thin Films. *Nanotechnology* **2010**, *21*, 145701. [CrossRef]
45. Gall, D. Electron Mean Free Path in Elemental Metals. *J. Appl. Phys.* **2016**, *119*, 085101. [CrossRef]
46. Moore, M. International Roadmap for Devices and Systems (IRDSTM) Edition 2020. Available online: https://irds.ieee.org/images/files/pdf/2020/2020IRDS_MM.pdf (accessed on 23 July 2020).
47. Clarke, J.S.; George, C.; Jezewski, C.; Caro, A.M.; Michalak, D.; Torres, J. Process Technology Scaling in an Increasingly Interconnect Dominated World. In Proceedings of the 2014 Symposium on VLSI Technology (VLSI-Technology), Honolulu, HI, USA, 9–12 June 2014.
48. Lanzillo, N.A.; Yang, C.-C.; Motoyama, K.; Huang, H.; Cheng, K.; Maniscalco, J.; Van Der Straten, O.; Penny, C.; Standaert, T.; Choi, K. Exploring the Limits of Cobalt Liner Thickness in Advanced Copper Interconnects. *IEEE Electron Device Lett.* **2019**, *40*, 1804–1807. [CrossRef]
49. Bekiaris, N.; Wu, Z.; Ren, H.; Naik, M.; Park, J.H.; Lee, M.; Ha, T.H.; Hou, W.; Bakke, J.R.; Gage, M.; et al. Cobalt Fill for Advanced Interconnects. In Proceedings of the 2017 IEEE International Interconnect Technology Conference (IITC), HsinChu, Taiwan, 16–18 May 2017.
50. Wen, L.G.; Adelmann, C.; Pedreira, O.V.; Dutta, S.; Popovici, M.; Briggs, B.; Heylen, N.; Vanstreels, K.; Wilson, C.J.; Van Elshocht, S.; et al. Ruthenium Metallization for Advanced Interconnects. In Proceedings of the 2016 IEEE International Interconnect Technology Conference/Advanced Metallization Conference (IITC/AMC), San Jose, CA, USA, 23–26 May 2016.
51. Bakke, J.; Lei, Y.; Xu, Y.; Daito, K.; Fu, X.; Jian, G.; Wu, K.; Hung, R.; Jakkaraju, R.; Breil, N. Fluorine-Free Tungsten Films as Low Resistance Liners for Tungsten Fill Applications. In Proceedings of the 2016 IEEE International Interconnect Technology Coference/Advanced Metallization Conference (IITC/AMC), San Jose, CA, USA, 23–26 May 2016.
52. Timalsina, Y.P.; Horning, A.; Spivey, R.F.; Lewis, K.M.; Kuan, T.-S.; Wang, G.-C.; Lu, T.-M. Effects of Nanoscale Surface Roughness on the Resistivity of Ultrathin Epitaxial Copper Films. *Nanotechnology* **2015**, *26*, 075704. [CrossRef]
53. Zheng, P.; Zhou, T.; Gall, D. Electron Channeling in TiO_2 Coated Cu Layers. *Semicond. Sci. Technol.* **2016**, *31*, 055005. [CrossRef]
54. Chawla, J.S.; Gstrein, F.; O'Brien, K.P.; Clarke, J.S.; Gall, D. Electron Scattering at Surfaces and Grain Boundaries in Cu Thin Films and Wires. *Phys. Rev. B* **2011**, *84*, 235423. [CrossRef]
55. Milosevic, E.; Kerdsongpanya, S.; Zangiabadi, A.; Barmak, K.; Coffey, K.R.; Gall, D. Resistivity Size Effect in Epitaxial Ru(0001) Layers. *J. Appl. Phys.* **2018**, *124*, 165105. [CrossRef]
56. Milosevic, E.; Kerdsongpanya, S.; Gall, D. The Resistivity Size Effect in Epitaxial Ru(0001) and Co(0001) Layers. In Proceedings of the 2018 IEEE Nanotechnology Symposium (ANTS), Albany, NY, USA, 14–15 November 2018.
57. Milosevic, E.; Kerdsongpanya, S.; McGahay, M.E.; Zangiabadi, A.; Barmak, K.; Gall, D. Resistivity Scaling and Electron Surface Scattering in Epitaxial Co(0001) Layers. *J. Appl. Phys.* **2019**, *125*, 245105. [CrossRef]
58. Zheng, P.; Gall, D. The Anisotropic Size Effect of the Electrical Resistivity of Metal Thin Films: Tungsten. *J. Appl. Phys.* **2017**, *122*, 135301. [CrossRef]