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High-Efficiency Switched-Capacitor DC-DC Converter with Three Decades of Load Current Range Using Adaptively-Biased PFM

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Abstract: A fully-integrated switched-capacitor (SC) DC-DC converter that steps down 2.0 V to 0.9 V with a peak efficiency of 80% is implemented in a 0.18 µm CMOS process. An ultra-low-power voltage-controlled oscillator that generates a wide range of switching frequencies is proposed to extend battery runtime. An efficiency >70% for load currents in the range of 12 µA to 17.8 mA is achieved by implementing a novel adaptively-biased pulse frequency modulation (ABPFM) technique in the controller. A symmetric charge-discharge topology with two-phase time interleaving is used as a power stage to reduce the output voltage ripple to <72 mV over the entire load current range.

Keywords: switched-capacitor; level shifter; pulse-frequency modulation; adaptive biasing; voltage-controlled oscillator (VCO)

1. Introduction

Recent developments in personal wearable devices, such as smart watches, offer more intelligent capabilities in an effort to satisfy consumer demand. High-performance CPUs are integrated into wearable devices to handle tasks such as collecting measurements from sensors and transmitting data over wireless networks. As wearable devices develop, the concerns of battery size and runtime become paramount for enhancing the user's experience. Though continuous shrinking of the transistor has helped to reduce power loss to a certain extent, the market always demands improved design to further extend battery runtime.

A system-on-chip (SoC) uses power, thermal, and performance (PTP) detectors that are distributed within the CPU in order to monitor operating conditions. The use of PTP technology for an SoC in [1] demonstrated a 23% increase in clock speed or up to 41% in power savings. Given PTP input data, SoCs in generic portable devices use several power-saving techniques, such as (a) dynamic power management (DPM), where system blocks are turned off during standby state, and (b) dynamic voltage and frequency scaling (DVFS), where the supply voltage and operating frequency are adjusted based on the workload [2].

Switched-capacitor (SC) DC-DC converters are gaining attention for the advantage of monolithic integration of the converter and no off-chip inductors for low-power applications [3]. Pulse frequency modulation (PFM) is a popular control technique used in SC converters to maintain high efficiency over a wide load current range [4].

Switched-capacitor (SC) DC-DC converters have the advantage of monolithic integration of the converter with no off-chip inductors. SC converters achieve efficiency greater than an LDOwhen the

output voltage is not close to the input voltage [5]. The peak theoretical efficiency of a step-down SC converter can be described using the relation [6]:

$$\eta_{PK} \approx \frac{P_{OUT}}{P_{OUT} + P_{BP} + P_{SW} + P_{DR} + P_{LK} + P_{CTRL}} \quad (1)$$

where P_{OUT} is the output power, P_{BP} is power loss from the parasitic bottom-plate (BP) capacitance of the charge transfer capacitor, P_{DR} is the gate driver loss, P_{SW} is the switch loss, P_{LK} is the power loss due to subthreshold leakage current through the power switches in the off-state, and P_{CTRL} is the power loss in the controller. P_{BP} is technology dependent and is the most important parameter limiting peak efficiency. Charge recycling techniques proposed in [7,8] reduce P_{BP}.

P_{CTRL} is a summation of the controller's dynamic switching power loss and static power loss, as in:

$$P_{CTRL} = P_{CTRL,DY} + P_{CTRL,ST} \quad (2)$$

At low load conditions, $P_{CTRL,DY}$ scales with frequency. However, static power loss in the controller, $P_{CTRL,ST}$, is largely unaddressed in the literature. η_{PK} is approximately constant as a function of switching frequency if $P_{CTRL,ST}$ is scaled along with $P_{CTRL,DY}$, until P_{LK} is comparable with other loss mechanisms.

With the objective to reduce the power consumption in the controller during low load conditions, we propose adaptively-biased pulse frequency modulation (ABPFM). The proposed ABPFM technique used along with DVFS and DPM is illustrated in Figure 1. Observe that ABPFM used in conjunction with DVFS has lower power consumption than DVFS by itself, since ABPFM greatly reduces power consumption during the sleep state. As such, the lower the load current requirements, the higher the power savings using ABPFM.

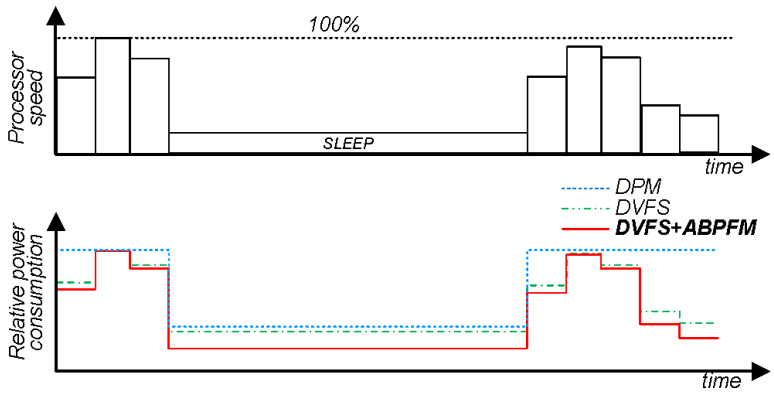

Figure 1. Comparison of relative power consumption at different processor speeds for dynamic power management (DPM) and dynamic voltage and frequency scaling (DVFS) with the proposed novel adaptively-biased pulse frequency modulation (ABPFM) technique. Adapted from [9].

The design of an SC converter with the proposed controller is described in Section 2. This includes a detailed description of the adaptively-biased folded-cascode amplifier and the ultra-low-power voltage-controlled oscillator (VCO) with level shifter. The converter implementation and measurement results are presented in Section 3, along with a comparison to state-of-the-art SC converters published in the literature.

2. SC DC-DC Converter Design and Controller

A conventional 2:1 SC DC-DC converter consists of a single charge transfer capacitor, called the flying capacitor, that delivers charge to the output load capacitor, called the tank capacitor. This conventional topology suffers from asymmetric output voltage ripple and poor load transient response. A symmetric charge-discharge 2:1 SC topology [10,11] divides the flying capacitor into two equal halves, such that each half is operated in anti-phase in order to charge the tank capacitor during both clock phases.

A symmetric charge-discharge topology with the proposed ABPFM controller is shown in Figure 2. The topology employs two-phase time-interleaving to reduce the output voltage ripple. The controller consists of an adaptively-biased error amplifier, an ultra-low-power VCO, an adaptively-biased level shifter (LS), a non-overlapping clock (NOC) generator, and gate drivers. Observe that the output of the error amplifier, V_{CTRL}, is used as a bias input to the error amplifier itself, as well as to the VCO and LS. As in a conventional PFM controller, the output of the amplifier drives the VCO, thereby tuning the frequency. Additionally, in the proposed ABPFM converter, the output of the error amplifier adjusts the bias current in the error amplifier itself and sets the bias current in the LS that follows the VCO.

ABPFM is performed in the control loop to achieve high efficiency at low load currents. The output voltage is sensed by the folded-cascode amplifier, which compares the output voltage, V_{OUT}, with a reference voltage, V_{REF}. This amplifier produces a control voltage, V_{CTRL}, that encodes the SC converter output load current. Load currents from low to high generate low to high V_{CTRL} voltages, respectively.

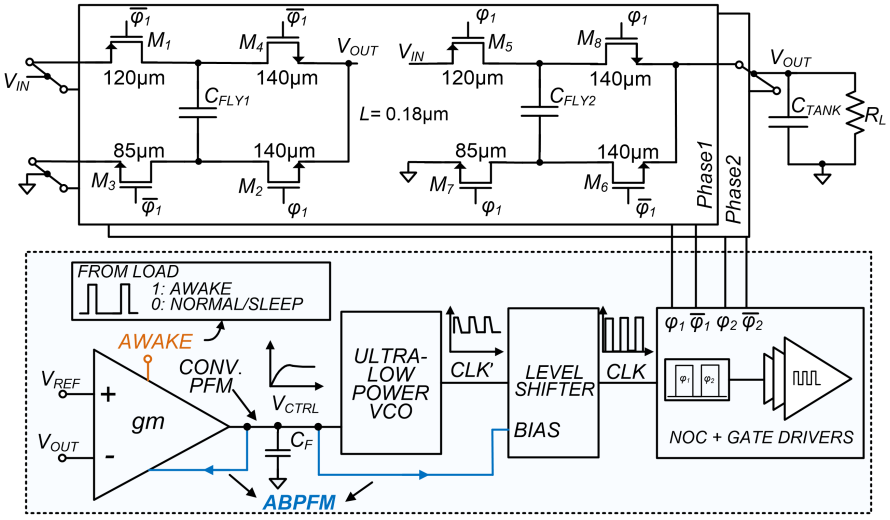

Figure 2. A two-phase time interleaved 2:1 symmetric charge-discharge switched-capacitor (SC) DC-DC converter with the proposed adaptively-biased pulse frequency modulation (ABPFM) controller.

2.1. Adaptively-Biased Folded-Cascode Amplifier

Figure 3 shows an adaptively-biased folded-cascode amplifier. NMOS mirror $M_{N1} - M_{N4}$ is a self-biased cascode current mirror such that $(W/L)_{M_{N1,2}} >> (W/L)_{M_{N3,4}}$. Bias voltages V_{BP}, V_{CP} and V_{BN} are generated using a conventional bias voltage generator [12]. The output of the amplifier, V_{CTRL}, reaches a maximum voltage $V_{CTRL,MAX} \approx V_{DD} - 2V_{DS,SAT}$ at high load currents and a minimum output voltage of $V_{CTRL,MIN} \approx V_{SS} + V_{DS,SAT}$ at low load currents. The amplifier bandwidth must be much less than switching frequency f_{SW} [13], so that the average output voltage is regulated at a desired value and the output ripple is minimized. If the bandwidth of the amplifier approaches the output voltage ripple frequency, the amplifier samples the ripple information instead of the average output voltage, causing the loop to be unstable. Low bandwidth is achieved through low input bias current. However, high bias

current enables faster transient response. Hence, moderate bias current is normally selected to achieve fast transient response, but at a bandwidth well below f_{SW}.

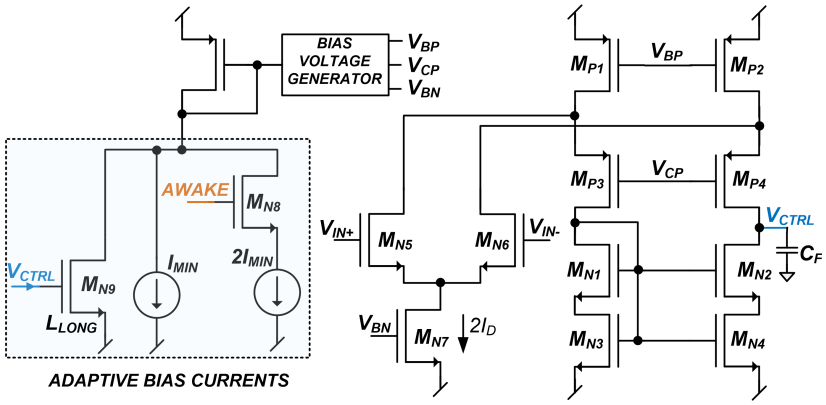

Figure 3. Adaptively-biased folded-cascode amplifier, showing the bias control input, V_{CTRL}, and digital awake sense input, *AWAKE*.

Referring to Figure 3, output voltage V_{CTRL} contains the SC converter load current information. It is used by the amplifier to increase or decrease its bias current at high or low converter load currents, respectively, through long-L transistor M_{N9}. The ability of the amplifier to set its bias current continuously permits a huge reduction in static power loss when the converter is driving ultra-low current loads. The amplifier is designed for maximum load current conditions. The amplifier bias current is decreased as the load current decreases, reducing the bandwidth of the amplifier. A minimum bias current I_{MIN} must be maintained in the amplifier for stability.

The gain bandwidth product (GBW) of the folded-cascode amplifier of Figure 3 is given by [12]:

$$GBW = g_m R_{OUT} \cdot \frac{1}{2\pi R_{OUT} C_{OUT}} = \frac{g_m}{2\pi C_{OUT}} \tag{3}$$

where g_m is the input transconductance, R_{OUT} the output resistance, and C_{OUT} the output capacitance. GBW decreases with g_m. Using the long-channel approximation, $g_m = \sqrt{2 I_D k' W/L}$, g_m decreases with the square root of bias current. This decrease in g_m reduces the overall GBW of the amplifier and moves the dominant pole in order to reduce the amplifier bandwidth. This reduction in GBW is critical at low load currents, where the switching frequency is reduced, and the requirement $GBW << f_{SW}$ is maintained [13].

The amplifier has an additional digital input signal, *AWAKE*. When *AWAKE* is high, the amplifier bias current is made artificially large in anticipation of the load coming out of sleep mode. The *AWAKE* signal can be set externally by the PTP detectors in an SoC. These detectors know in advance that the load current requirements are about to increase. In this way, the converter has a much improved output load transient response.

2.2. Ultra-Low Power VCO and Level Shifter

A conventional current-starved VCO uses a fixed minimum bias current in each inverter stage in order to oscillate with a large output voltage swing. Using a fixed minimum bias current is a lossy method that limits the peak efficiency when the converter is operating at very low output power.

The proposed ultra-low power VCO shown in Figure 4 solves the above challenge by avoiding a current-starved implementation. The VCO is designed using a fifteen-stage ring oscillator, where the total current from all branches that sets the oscillation frequency is controlled by a single NMOS device M_{NC}. The length of M_{NC} is large to make the VCO linear and achieve a wide oscillation frequency range from a

few kHz to hundreds of MHz. Input V_{CTRL} sets the VCO oscillation frequency. Additional delay from transistors M_{P0} and M_{N0} in the first stage of the 15-stage ring allows one to obtain a 16-stage equivalent delay. In this way, it is possible to generate two 90°-phase time-interleaved clocks for the SC converter, labeled CLK_1 and CLK_2 in Figure 4. Variation in the phase of CLK_1 and CLK_2, due to mismatch in the VCO, increases the output voltage ripple, but does not affect efficiency.

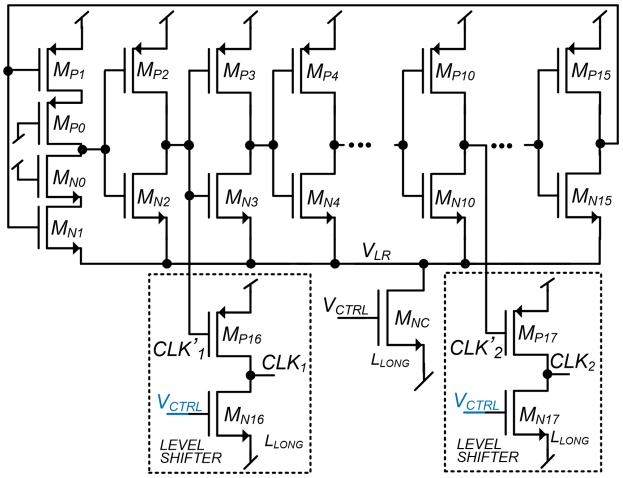

Figure 4. A 15-stage ultra-low-power VCO with added delay in the first stage to make a 16-stage equivalent. Two 90° phase difference clocks from the VCO are level-shifted with two adaptively-biased level shifters.

In general, low oscillation frequencies in the range of tens of kHz can be generated either by increasing the capacitance in each ring stage or reducing the branch current to a few nA. Increasing the ring stage capacitance limits the peak achievable frequency and also increases the dynamic switching losses. On the other hand, decreasing the branch currents makes the VCO suffer from poor low-side voltage swing.

When the converter is operating at the minimum load current, where the VCO is at the minimum frequency, the voltage swing of the VCO at nodes CLK_1' and CLK_2' is limited to approximately 200 mV. This voltage swing monotonically increases with the oscillation frequency. M_{NC} is a long-L device, which operates in the subthreshold, saturation, and triode regions to generate low, medium, and high frequency oscillations. Switching frequency is directly proportional to load current.

A level shifter (LS) is required to increase the VCO voltage swing and operate over the frequency range of a few kHz to hundreds of MHz. An LS design using conventional methods, such as differential cascode voltage switch (DCVS), current-mirror, and capacitive coupling, suffers from a narrow range of input voltages and/or requires complex circuits that consume significant power [14–16].

An LS implementation, which has an input range that swings close to V_{DD} in order to sense the output of the proposed VCO, is shown in Figure 4. The LS is a common-source amplifier with a bias current that is adaptively adjusted by the signal V_{CTRL}, the same signal that sets the VCO oscillation frequency. As V_{CTRL} increases, the bias current in the LS increases, allowing for faster transitions at higher frequencies. The delay of the LS is less significant as the delay of the error amplifier (labeled gm in Figure 2) is typically higher due to the integration operation. The power consumption of the LS is described below as part of Figure 5.

A simulated power breakdown of the proposed converter as a function of load current is shown in Figure 5. At high load currents, the major power loss contributors are the bottom-plate capacitor (P_{BP}), large switches (P_{SW}) in the power stage charging C_{FLY} and C_{TANK}, and gate drivers (P_{DRIVE}). A relatively small amount of power is consumed in the controller, which is the sum of losses in the amplifier (P_{AMP}), LS (P_{LS}), and VCO (P_{VCO}). As the load current decreases, f_{SW} reduces proportionally, decreasing dynamic

losses in P_{BP}, P_{SW}, P_{DRIVE}, and P_{VCO}. In this work, static power losses P_{AMP} and P_{LS} are also reduced with load current through the use of adaptive biasing, achieving high efficiency over a wide load current range. Observe that P_{LS} increases slightly for $I_{LOAD} < 50$ µA due to the power loss associated with slow transitions in CLK_1 and CLK_2 driving inverter loads, a solution for which is described in [17].

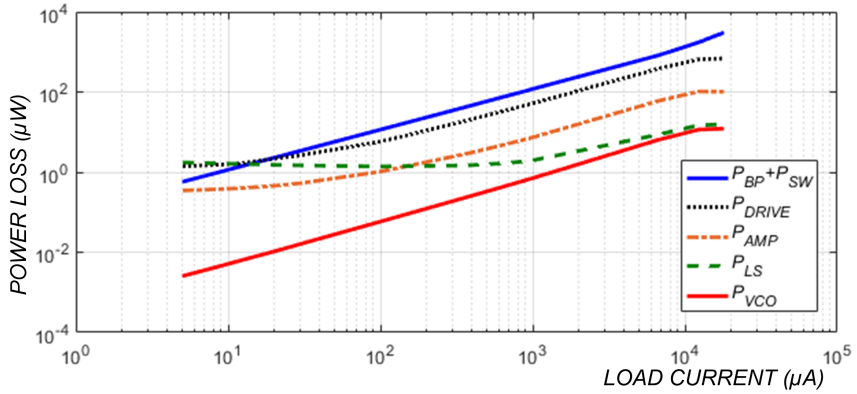

Figure 5. Simulated power breakdown over the load current range showing the power loss from the SC power stage, $P_{SW} + P_{BP}$, gate driver, P_{DRIVE}, error amplifier, P_{AMP}, level-shifter, P_{LS}, and VCO, P_{VCO}.

3. Implementation and Measurement Results

The block diagram of the fully-integrated 2:1 switched-capacitor DC-DC converter shown in Figure 2 was implemented in a 0.18-µm CMOS process with metal-insulator-metal (MIM) and dual-MIM capacitor options. A V_{IN} of 2.0 V was stepped down to 0.9 V while driving a maximum load current of 17.8 mA. A flying MIM capacitor of 515 pF was used for charge transfer [18,19]. An on-chip dual-MIM capacitor of 1.2 nF was used as the tank capacitor, limited by die area. All switches were sized with finite on-resistance to reduce the peak capacitor charging current, such that high efficiency was achieved at peak load current [20]. Signal V_{REF} was given externally.

The converter f_{SW} was set by the output of the folded-cascode amplifier, V_{CTRL}, by sensing the output voltage, V_{OUT}. The proposed VCO was designed to generate f_{SW} from 20 kHz to 49 MHz for applied gate voltages from $V_{CTRL,MIN}$ to $V_{CTRL,MAX}$. Two clocks at 90^o phase difference were derived from the VCO and level shifted. These clocks were given as input to NOC generators, which produced non-overlapping clocks with at least 1 ns dead time. These clocks went to gate drivers and then powered the switches.

3.1. Hardware Measurements

The measured output voltage while driving a peak 17.8 mA current load had an average voltage, $<V_{OUT}>$, of 0.898 V and ripple, ΔV_{OUT}, of 15 mV. The measured efficiency was 76.7% at a switching frequency of 47 MHz. A peak efficiency of 80.1% was achieved at 10 mA of load current.

The measured efficiency while driving a load current from 4 µA to 17.8 mA is shown in Figure 6a. The measured efficiency was greater than 70% for load currents in the range of 12 µA to 17.8 mA and greater than 60% from 8 µA to 12 µA. The sudden drop in efficiency below 17 µA was due to the dominance of static power loss. The measured switching frequency as a function of load current is shown in Figure 6b. Observe the slope of 5 kHz/μA, equivalent to the rate of change in frequency with respect to load current.

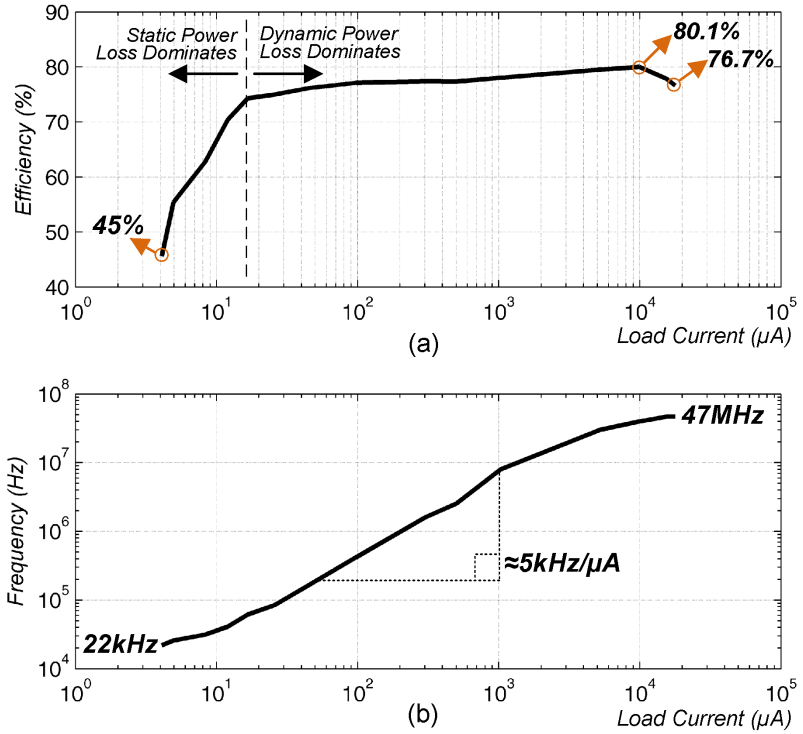

Figure 6. Measurement results showing (**a**) efficiency vs. load current with an illustration of relative static and dynamic power losses and (**b**) switching frequency vs. load current.

A load transient between 10 mA and 100 µA is shown in Figure 7. An overshoot of 70 mV and undershoot of 200 mV were observed. The change in average output voltage during the load transient was 36 mV. When driving 100 µA of load current, the bias currents in the controller were reduced using ABPFM, which lowered the bandwidth of the error amplifier. Prior to a load transient event from 100 µA to 10 mA, the bias current in the error amplifier was increased in order to sense the transient event quickly by setting *AWAKE* high. The *AWAKE* signal could be set externally by PTP detectors in an SoC. When *AWAKE* went high, this increase in bias current reduced the DC gain of the amplifier, causing a slight increase in average output voltage. On the other hand, a large dip of 350 mV in the output voltage occurred if *AWAKE* was held at zero, as shown with dashed lines in Figure 7. In order to reduce this dip in V_{OUT} to 200 mV, *AWAKE* was set high several microseconds before the 100 µA to 10 mA transient. No *AWAKE* pulse was required during the high-to-low load current transient as the bias currents were already high.

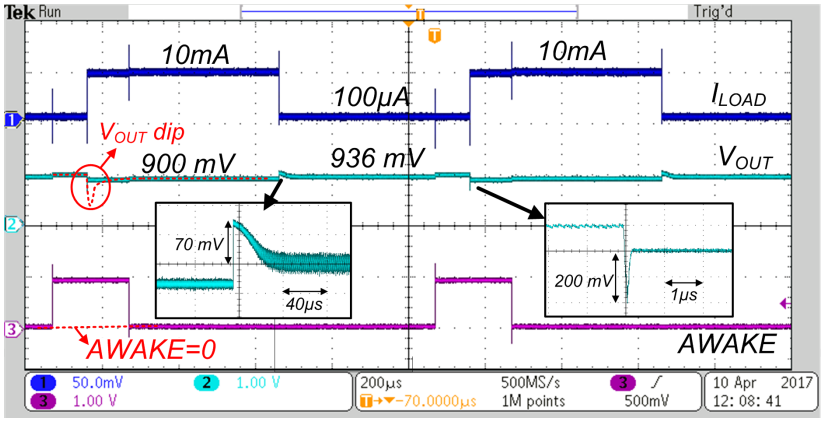

Figure 7. Load transients between 100 µA and 10 mA showing the *AWAKE* signal. The dip for V_{OUT} illustrates the behavior of V_{OUT} if *AWAKE* = 0 during a low-to-high load transient.

A micrograph of the fabricated integrated-circuit is shown in Figure 8a and the test PCB in Figure 8b. The converter measured 990 × 966 µm^2 without bond pads.

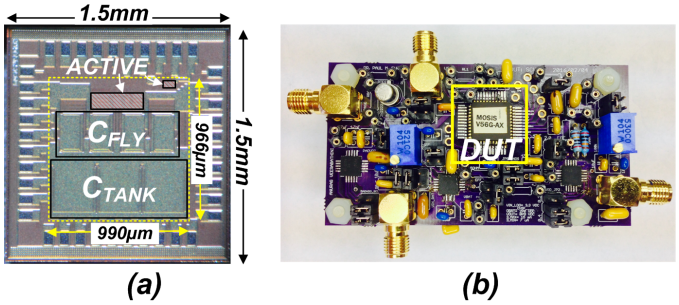

Figure 8. (**a**) Micrograph of the fabricated chip and (**b**) PCB used for hardware measurements showing the device-under-test (DUT).

3.2. Comparison

A comparison of the proposed work with the state-of-the-art of recently published SC converters is shown in Table 1. The proposed converter maintained less than a 10% drop from its peak efficiency over three decades of load current (17.8 mA/12 µA = 1483) and had the highest load current range compared to others. The use of a charge recycling technique in every time-interleaved phase in [8] helped to achieve the record peak efficiency of 94.6% for all fully-integrated SC converters in the literature. However, this converter's efficiency dropped below 60% for load currents <167 µA. On the other hand, our proposed converter had the lowest peak efficiency due to the process limitation in bottom-plate parasitic capacitance. The addition of a charge recycling technique to an ABPFM converter would noticeably improve its peak efficiency. Finally, the proposed converter had the highest power density compared to others except [18], where an area-efficient and costly deep-trench (DT) capacitor was used along with a 33 nF off-chip tank capacitor.

To emphasize the importance of high efficiency over a wide load current range, we propose the following figure-of-merit (FOM):

$$FOM = \sqrt{\eta_{MAX}\eta_{MIN}}\ \log_{10}\left(\frac{I_{MAX}}{I_{MIN}}\right) \quad (4)$$

This FOM is the geometric mean of the efficiency limits times the number of decades of load current range. Overall, the proposed converter had the highest FOM, widest load current range, highest minimum efficiency, and highest power density amongst the fully-integrated SC converters in Table 1.

Table 1. Comparison with the state-of-the-art.

Parameter	[8]	[18]	[21]	[22]	This Work
Process	40 nm	32 nm SOI	0.35 µm	0.35 µm	**0.18 µm**
C_{FLY}	metal-oxide-metal	deep trench	MIM	Off-chip	**MIM**
C_{TANK}	NO	Off-chip	-	Off-chip	**dual MIM**
Conversion Ratio	1/2	1/2	5/13 -5/2	2/1, 3/1	**1/2**
Control Scheme	Hysteretic	PFM	PFM	Adaptive-on-time	**ABPFM**
V_{IN} (V)	1.85–2.07	1.8	2–13	1.1–1.8	**2.0**
$<V_{OUT}>$ (V)	0.9	0.836	5	2, 3	**0.9**
$I_{L,MAX}$ (A)	4.25 m	19.1 m †	4 m	12 m	**17.8 m**
$I_{L,MIN}$ (A)	167 µ †	5.2 m †	500 µ †	500 µ	**12 µ**
$\eta_{I_{L,MAX}}$ (%)	94.6	86	81.5	89.5	**80**
$\eta_{I_{L,MIN}}$ (%)	60 †	80	60 †	75	**70**
C_{FLY}(F)	10 n	690 p	-	4.7 µ	**515 p**
C_{TANK}(F)	0	33 n	3.64 n *	1 µ	**1.2 n**
Area (mm^2)	2.4	0.00344 $^+$	6.8	6.9 $^+$	**0.96**
P_D (W/mm^2)	1.6 m	4.6 $^+$	3.0 m	5.2 m $^+$	**16.8 m**
FOM	1.06	0.47	0.63	1.13	**2.37**

† Calculated value; * $C_{FLY} + C_{TANK}$ reported; $^+$ off-chip capacitor not included.

4. Conclusions

Adaptively-biased pulse-frequency modulation (ABPFM) was introduced in this paper to reduce the static power loss in a low-power DC-DC converter operating in standby/sleep mode. An ultra-low-power VCO was implemented to generate a wide range of frequencies suitable for switching converters. The proposed converter maintained >70% efficiency over three decades of load current range. The proposed ABPFM was implemented with a 2:1 voltage conversion ratio fully-integrated SC DC-DC converter in a 0.18-µm CMOS process. This technique could be applied to extend the battery runtime of wearable devices, which are designed to operate in sleep mode the vast majority of the time.

Author Contributions: The research problem was identified, executed, and solved by both authors. A.V. conducted the literature review, architecture research, feasibility study, and methodology investigation. He also designed, simulated, performed the layout, tested, and wrote the original draft manuscript. He is the main author of the paper. P.M.F. supervised the research that includes and is not limited to: conceptualization, project administration, architecture design, circuit design, simulation and measurement results review, manuscript review, and extensive manuscript corrections. Both authors contributed significantly to this work.

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Conflicts of Interest: The authors declare no conflict of interest.

References

1. Wang, A.; Lin, T.; Ouyang, S.; Huang, W.; Wang, J.; Chang, S.; Chen, S.; Hu, C.; Tai, J.C.; Tan, K.; et al. 10.3 Heterogeneous Multi-processing quad-core CPU and dual-GPU Design for optimal performance, power, and thermal tradeoffs in a 28nm mobile application processor. In Proceedings of the 2014 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC), San Francisco, CA, USA, 9–13 February 2014; pp. 180–181, doi:10.1109/ISSCC.2014.6757390.

2. Jiang, J.; Lu, Y.; Ki, W.H.; Seng-Pan, U.; Martins, R.P. A dual-symmetrical-output switched-capacitor converter with dynamic power cells and minimized cross regulation for application processors in 28nm CMOS. In Proceedings of the 2017 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 5–9 February 2017; pp. 344–345, doi:10.1109/ISSCC.2017.7870402.
3. Jevtić, R.; Le, H.P.; Blagojević, M.; Bailey, S.; Asanović, K.; Alon, E.; Nikolić, B. Per-Core DVFS With Switched-Capacitor Converters for Energy Efficiency in Manycore Processors. *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.* **2015**, *23*, 723–730, doi:10.1109/TVLSI.2014.2316919.
4. Kilani, D.; Alhawari, M.; Mohammad, B.; Saleh, H.; Ismail, M. An Efficient Switched-Capacitor DC-DC Buck Converter for Self-Powered Wearable Electronics. *IEEE Trans. Circuits Syst. I Reg. Pap.* **2016**, *63*, 1557–1566, doi:10.1109/TCSI.2016.2586117.
5. Furth, P.M.; Veerabathini, A.; Saifullah, Z.M.; Rivera, D.T.; Elkanishy, A.; Badawy, A.A.; Michael, C.P. Supervisory Circuits for Low-Frequency Monitoring of a Communication SoC. In Proceedings of the 2019 IEEE 62nd International Midwest Symposium on Circuits and Systems (MWSCAS), Dallas, TX, USA, 4–7 August 2019; pp. 17–20, doi:10.1109/MWSCAS.2019.8885315.
6. Krihely, N.; Ben-Yaakov, S.; Fish, A. Efficiency Optimization of a Step-Down Switched Capacitor Converter for Subthreshold. *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.* **2013**, *21*, 2353–2357, doi:10.1109/TVLSI.2012.2231888.
7. Andersen, T.M.; Krismer, F.; Kolar, J.W.; Toifl, T.; Menolfi, C.; Kull, L.; Morf, T.; Kossel, M.; Brändli, M.; Buchmann, P.; et al. A 4.6W/mm2 power density 86% efficiency on-chip switched capacitor DC-DC converter in 32 nm SOI CMOS. In Proceedings of the IEEE Applied Power Electronics Conference and Exposition (APEC), Long Beach, CA, USA, 17–21 March 2013; pp. 692–699, doi:10.1109/APEC.2013.6520285.
8. Butzen, N.; Steyaert, M.S.J. Scalable Parasitic Charge Redistribution: Design of High-Efficiency Fully Integrated Switched-Capacitor DC-DC Converters. *IEEE J. Solid-State Circuits* **2016**, *51*, 2843–2853, doi:10.1109/JSSC.2016.2608349.
9. Ma, D.; Bondade, R. *Reconfigurable Switched-Capacitor Power Converters— Principles and Designs for Self-Powered Microsystems*; Springer: Berlin/Heidelberg, Germany, 2013.
10. Veerabathini, A.; Furth, P.M. A Low Output Voltage Ripple Fully-Integrated Switched-Capacitor DC-DC Converter. In Proceedings of the 2019 IEEE 62nd International Midwest Symposium on Circuits and Systems (MWSCAS), Dallas, TX, USA, 4–7 August 2019; pp. 937–940, doi:10.1109/MWSCAS.2019.8884904.
11. Patounakis, G.; Li, Y.W.; Shepard, K.L. A fully integrated on-chip DC-DC conversion and power management system. *IEEE J. Solid-State Circuits* **2004**, *39*, 443–451, doi:10.1109/JSSC.2003.822773.
12. Baker, R. *CMOS: Circuit Design, Layout, and Simulation*, 2nd ed.; Wiley: Hoboken, NJ, USA, 2011; pp. 796–808.
13. Mattingly, D. Designing Stable Compensation Networks for Single Phase Voltage Mode Buck Regulators. Available online: https://e2echina.ti.com/cfs-file/__key/telligent-evolution-components-attachments/00-24-01-00-00-03-73-41/Compensation-Network.pdf (accessed on 19 April 2019).
14. Wen, L.; Cheng, X.; Tian, S.; Wen, H.; Zeng, X. Subthreshold Level Shifter With Self-Controlled Current Limiter by Detecting Output Error. *IEEE Trans. Circuits Syst. II Exp. Briefs* **2016**, *63*, 346–350, doi:10.1109/TCSII.2015.2504025.
15. Lanuzza, M.; Crupi, F.; Rao, S.; Rose, R.D.; Strangio, S.; Iannaccone, G. An Ultralow-Voltage Energy-Efficient Level Shifter. *IEEE Trans. Circuits Syst. II Exp. Briefs* **2017**, *64*, 61–65, doi:10.1109/TCSII.2016.2538724.
16. Abdelmoaty, A.; Al-Shyoukh, M.; Fayed, A. A high-voltage level shifter with sub-nano-second propagation delay for switching power converters. In Proceedings of the 2016 IEEE Applied Power Electronics Conference and Exposition (APEC), Long Beach, CA, USA, 20–24 March 2016; pp. 2437–2440, doi:10.1109/APEC.2016.7468207.
17. Veerabathini, A.; Eshappa, N.B.; Furth, P.M. Low-power pulse width modulation (PWM) for high-frequency DC–DC converters. *Electron. Lett.* **2018**, *54*, 585–587, doi:10.1049/el.2018.0572.
18. Andersen, T.M.; Krismer, F.; Kolar, J.W.; Toifl, T.; Menolfi, C.; Kull, L.; Morf, T.; Kossel, M.; Brändli, M.; Francese, P.A. Modeling and Pareto Optimization of On-Chip Switched Capacitor Converters. *IEEE Trans. Power Electron.* **2017**, *32*, 363–377, doi:10.1109/TPEL.2016.2529501.
19. Le, H.P.; Sanders, S.R.; Alon, E. Design Techniques for Fully Integrated Switched-Capacitor DC-DC Converters. *IEEE J. Solid-State Circuits* **2011**, *46*, 2120–2131, doi:10.1109/JSSC.2011.2159054.

20. Evzelman, M.; Ben-Yaakov, S. Average-Current-Based Conduction Losses Model of Switched Capacitor Converters. *IEEE Trans. Power Electron.* **2013**, *28*, 3341–3352, doi:10.1109/TPEL.2012.2226060.
21. Lutz, D.; Renz, P.; Wicht, B. A 10mW fully integrated 2-to-13V input buck-boost SC converter with 81.5% peak efficiency. In Proceedings of the 2016 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 31 January–4 February 2016; pp. 224–225, doi:10.1109/ISSCC.2016.7417988.
22. Hua, Z.; Lee, H. Adaptive-on-time control technique for output ripple reduction and light-load efficiency enhancement in low-power switched-capacitor DC-DC regulators. In Proceedings of the 2015 IEEE Applied Power Electronics Conference and Exposition (APEC), Charlotte, NC, USA, 15–19 March 2015; pp. 1930–1933, doi:10.1109/APEC.2015.7104610.