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A 28 nm CMOS 100 MHz 67 dB-Dynamic-Range 968 μW Flipped-Source-Follower Analog Filter †

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Abstract: This paper presents a fourth-order continuous-time analog filter based on the cascade of two flipped-source-follower (FSF) biquadratic (biquad) cells. The FSF biquad adopts two interacting loops (the first due to the classic source-follower, and the second to the additional gain path) which lower the impedances of all circuit nodes with relevant benefits in terms of noise power reduction and linearity enhancement. The presented device was integrated in 28 nm CMOS and featured 100 MHz −3 dB bandwidth with 67 dB Dynamic-Range. Input IP3 was 12 dBm at 10 and 11 MHz input tone frequencies. Total power consumption was 0.968 mW (0.484 mW per cell). Hence, the filter performed one of the highest figures-of-merit (160.7 dBJ-1) compared with analog state-of-the-art filters.

Keywords: analogue circuits; analogue integrated circuits; analogue filters

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1. Introduction

Source-follower (SF) analog filters are a well-established and popular topic in analog filter design [1–5]. They exploit the intrinsic features of source follower stages, such as large bandwidths at low noise powers, low harmonic distortion, and limited power consumption. These features make SF filters very attractive for new-generation telecommunication transceivers [6] and front-end analog sensors [7] where analog filter bandwidths have been raised up to 50/100 MHz to fit the increasing communication rate.

These innovative applications force analog filters to comply with stringent noise power spectral density (PSD) requirements because the noise is spread over a wider bandwidth, imposing lower in-band noise PSD at constant integrated noise power [8]. Nonetheless, lower in-band noise PSD should be accompanied by an (almost) rail-to-rail output swing to avoid dynamic range drops for the following A-to-D converter.

Dedicated analog solutions based on open-loop g_m-C filters [9] have intrinsic low-noise and low-power performances that partially fit the telecommunications requirements. On the other hand, g_m-C filters are not able to preserve linearity, unless to increase overdrive voltage that is often not an option in nanometer-range technologies where voltage headroom ($V_{DD} - V_{TH}$; supply and threshold, respectively) is significantly smaller. Nonetheless, increasing overdrive leads to increasing power at constant transconductance (g_m) and, moreover, intrinsically limits the available output voltage swing (and thus dynamic range, which is further reduced by scaled-down V_{DD}, not higher than 1 V for standard-process (SP) MOS transistors (MOST) in CMOS 65 nm and below).

For these reasons, several studies in the literature [10–14] exploit closed-loop active-RC solutions that meet linearity specifications, and easily manage rail-to-rail output swings, whereas they require an intrinsic power budget to be allocated to the larger unity

gain frequency amplifiers. In this scenario, some studies have explored alternative circuital options, taking advantage of the low noise, low power, and large linearity performance of SF filters.

1.1. Source-Follower Filter State-of-the-Art vs. CMOS Technology

State-of-the-art SF filters adopt scarcely scaled-down technological nodes (0.13 μm [1] and 0.18 μm [2–5] CMOS at 1.2 V and 1.8 V supply voltage, respectively, for SP MOST). One of the main motivations is the intrinsic operating DC voltage difference between input/output (gate/source) nodes for biasing. Moreover, both 0.13 μm and 0.18 μm CMOS operate with a safe operating point voltage headroom (V_{DD}-V_{TH} = 1.3 V and 0.9 V, respectively), enabling a moderate inversion region for SF input MOSTs (for instance, M1 in Figure 1). This increases the characteristic transconductance (g_m), minimizes in-band noise power spectral density (PSD), and improves linearity performance when input tone frequency approaches filter pole frequency. In other words, SF filters well adapt to 0.13 μm [1] and 0.18 μm [2–5] CMOS nominal characteristics, resulting in very advanced and efficient circuital solutions.

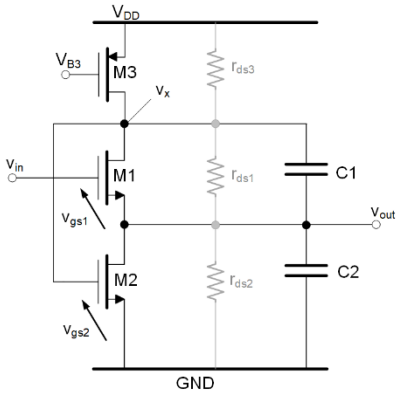


Figure 1. Flipped-source-follower biquadratic cell.

In [2] he single N-channel MOST SF has been improved by including a second gain stage (based on a p-channel MOST) in the direct path of the closed-loop scheme that allows synthesis of a specific complex pole pair and to separately optimize the two MOSTs (the input stage MOST for noise and linearity; the second stage MOST for loop-gain enhancement), increasing the circuit efficiency. If the additional gain stage is a P-channel device, and the input stage MOST is an N-channel type, mismatch between two different MOST carriers' mobility could be an issue for the closed-loop transfer function, where both MOSTs operate with their own transconductances. Moreover, an additional PMOS gain stage requires additional current consumption to be allocated directly to the stage (increasing power) or to be subtracted from the input stage (increasing noise).

In order to overcome these issues, M. De Matteis et al. [3] proposes (by Spice simulations) to adopt the flipped version of the SF circuit, where two cascode MOSTs concentrate the gain in the same stack, have the same channel carrier typology, and maintain the separation between noise/linearity (input MOST) and loop gain (the bottom MOST in the cascode). Unfortunately, this solution, even presenting an efficient design results (large in-band linearity with >20 dBm input IP3 and 5.8 nV/√Hz in-band noise PSD), scarcely fits with the reduction in both V_{DD}-V_{TH} (0.5 V in 28 nm CMOS against 1.3 V in 0.18 μm CMOS) voltage headroom for biasing and MOST intrinsic gain.

Xu Yang, et al. [4,5] present a similar biquadratic (biquad) cell concept in CMOS 0.18 μm technology nodes. Both devices achieve large in-band IIP3 and, importantly, operate with 1.35 V and 1.3 V supply voltages at 0.55 V nominal threshold voltages for SP MOST in CMOS 0.18 μm, approaching, without targeting, nanometer-range technology scenarios.

1.2. CMOS 28 nm Flipped-Source-Follower Filter

The filter presented here [15] advances the state of the art by:

- Improving matching and reducing power with respect to [2];
- Scaling-down FSF filters to 28 nm CMOS;
- Reducing the nominal supply voltage to 1 V;
- Extending the −3 dB bandwidth from 33 MHz [2] up to 100 MHz.

The filter is composed of the cascade of two biquads, synthesizing a 100 MHz pole frequency response and consuming 968 μW power from a single 1 V supply voltage. Measured input IP3 is 12.5 dBm and 2.5 dBm for 10 and 11 MHz and 50 and 51 MHz input tones, respectively. The final achieved figure-of-merit outperforms the state-of-the-art filters with 160 dBJ-1@10 and 11 MHz and 160.7 dBJ-1@50 and 51 MHz.

This paper is organized as follows. Section 2 presents the transistor-level scheme of the filter and most relevant design aspects in terms of operating point, closed-loop, and loop-gain transfer function, noise, and linearity. Section 3 shows the experimental validation of the filter prototype carried out by both time and frequency domain electrical characterizations. Finally, at the end of the paper, conclusions will be drawn.

2. Flipped-Source-Follower Filter Transistor-Level Design

The transistor-level scheme of the proposed biquadratic cell based on FSF analog stage is shown in Figure 1. The FSF filter is composed of an M1-M2 MOST biased by a current source (M3). C_1-C_2 capacitances with g_{m1}-g_{m2} (M1-M2 transconductances) synthesize a specific pair of complex conjugated poles. r_{ds1}, r_{ds2} and r_{ds3} are the output resistances of M1, M2 and M3 MOSTs, respectively.

The M1 gate-source voltage swing is strongly reduced by the M1-M2 loop-gain and all the nodes of the circuit (whose electrical voltages are v_{out} and v_x) have lower impedance to the ground compared to what was happening without the action of the loop-gain (low frequency output impedance to ground is approximately equal to $1/(g_{m1} \cdot g_{m2} \cdot r_{ds3})$ and M1 drain node impedance to ground is approximately equal to $1/g_{m2}$).

This implies that both M1 and M2 have very limited gate-source voltage (V_{GS}) swings. As a result, the biquad cell presented in Figure 1 synthesizes a specific complex pole pair, while ideally zeroing the gate-source voltage swing of all MOSTs, thus minimizing harmonic distortion (among other aspects directly proportional to the voltage swing at the MOST gate node). Moreover, at the first order, because M1 drain and source nodes have very small equivalent impedance to ground, any M2 noise current will flow by ground with negligible noise voltage swing.

2.1. Operating Point and Output Signal Swing

The input transistor (M1) operates with a finite DC voltage between gate and source nodes for biasing. A strong inversion region would limit the output swing, reducing the dynamic range (DR) for a given noise power.

On the other hand, a sub-threshold region leads to higher harmonic distortion power when the input tone frequency approaches the closed-loop pole frequency (where the filter has very small loop-gain and linearity is no longer preserved by the loop gain). Therefore, a larger V_{OV} would mitigate this increasing distortion at higher frequencies.

For these reasons, this design adopts a trade-off approach between DR maximization and harmonic distortion reduction, by setting the biasing overdrive voltage ($V_{OV} = V_{GS}$-V_{TH}) at 75 mV for both M1-M2 (i.e., the transition voltage point between weak and moderate inversion regions). This choice preserves DR while avoiding the deep sub-threshold region, where high-frequency distortion should dramatically increase.

Assuming that all MOSTs have the same V_{TH} and V_{OV}, then the input common-mode voltage ($V_{in,CM}$) of the biquad n-channel M1 MOST input stage and the input voltage swing ($V_{in,SW}$) are limited by the following relationship:

$$V_{TH} + 2 \cdot V_{OV} < V_{in,CM} + V_{in,SW} < V_{DD} \quad (1)$$

Hence, $V_{in,CM} + V_{in,SW}$ ranges from 0.65 V to 1 V (VDD), with $V_{TH} \approx 0.5$ V and $V_{OV} = 0.075$ V. This design adopts $V_{in,CM} = 0.825$ V, to maximize the filter input signal swing ($V_{in,SW} = 0.175\ V_{0\text{-}PEAK}$) that perfectly matches with the output swing limitations as follows. The M1 source common mode voltage ($V_{out,CM}$) is limited by Equation (2):

$$V_{OV} < V_{out,CM} + V_{out,SW} < V_{TH} \quad (2)$$

Thus, $V_{out,CM} = V_{in,CM} - (V_{TH} + V_{OV}) = 0.25$ V agrees with a ±0.175 $V_{0\text{-}PEAK}$ input/output swing.

The design approach operates both M1-M2 without considering body effect (which is non-null in M1). This leads to a slight mismatch between two transconductances, resulting in limited quality factor and pole frequency deviation that can be easily adjusted by recalculating C_1-C_2 values.

2.2. Biquad Closed-Loop Transfer Function

The biquad transfer function (assuming infinite MOST output resistances) is given by Equation (3):

$$T(s) = \frac{v_{out}}{v_{in}}(s) \cong \frac{1}{s^2 \cdot \frac{C_1 \cdot C_2}{g_{m1} \cdot g_{m2}} + s \cdot \frac{C_1}{g_{m1}} + 1} \quad (3)$$

It features 0 dB DC gain. Pole frequencies (ω_0) and quality factors (Q) are given by:

$$\omega_0 \cong \sqrt{\frac{g_{m1} \cdot g_{m2}}{C_1 \cdot C_2}} \quad \text{and} \quad Q \cong \sqrt{\frac{g_{m1}}{g_{m2}} \cdot \frac{C_2}{C_1}}\Bigg|_{g_{m1}=g_{m2}} = \sqrt{\frac{C_2}{C_1}} \quad (4)$$

2.3. Biquad Loop Gain

The proposed FSF filter uses C_1-C_2 capacitances for synthesizing complex conjugated poles. This changes the loop gain, compared with generic FSF buffers, in terms of lower unity gain frequency (which is now, in first approximation, equal to the filter closed-loop pole frequency). Equation (5) reports loop-gain transfer function including, in addition to g_{m1}-g_{m2} and C_1-C_2 pairs, all MOST output drain-source resistances:

$$G_{loop}(s) = -g_{m2} \cdot r_{ds3} \cdot \frac{1 + s \cdot \frac{C_1}{g_{m1}}}{s^2 \cdot \frac{C_1 \cdot C_2 \cdot r_{ds3}}{g_{m1}} + s \cdot \left(\frac{C_1}{g_{m1}} \cdot \left(1 + \frac{r_{ds3}}{r_{ds2}}\right) + \frac{C_2}{g_{m1}} \cdot \left(1 + \frac{r_{ds3}}{r_{ds1}}\right) \right) + 1} \quad (5)$$

The loop-gain magnitude and phase frequency response are plotted in Figure 2, with and without the effect of the M2 gate-source parasitic capacitance (C_{P2}) which does not significantly modify the phase margin at the unity gain frequency and whose impact is negligible comparing with C_1-C_2. FSF has lower loop-gain at higher frequency while approaching the pole frequency.

Figure 3 shows the Gauss plane root locus of the FSF biquad cell, where the loop-gain poles and zero with closed-loop poles are plotted, and as expected, the locus is attracted by the zero (whose frequency is $2 \cdot \pi \cdot g_{m1}/C_1 \approx 900$ MRad/s) and moved away from the poles ((−49.1 ± j·99) MRad/s which have an equivalent quality factor (Q_{Loop}) equal to 1.12).

The root locus (starting in the negative real part Gauss plane region) moves towards the left half Gauss plane, without any eventual stability issue.

Table 1 lists the values of the root locus main singularities, and Table 2 reports the design parameters of each cell.

The filter is composed of the cascade of two biquads, and this analysis is referred to the higher quality factor (Q = 1.3066).

Table 1. Root locus.

Singularity	Complex Notation	Frequency	Q
G_{loop} Poles (1)	[−49 ± j·99] MRad/s	2·π·17.58 MRad/s	1.12
G_{loop} Zero	−903.1 MRad/s	2·π·143 MRad/s	1.12
Filter Poles (1)	[−262 ± j·590] MRad/s	2·π·100 MRad/s	1.29

Table 2. Filter design parameters.

Cell A Parameter	Value	Cell B Parameter	Value
Q Factor	0.5412	Q Factor	1.306
g_{m1}-g_{m2}	1.8 mA/V	g_{m1}-g_{m2}	1.8 mA/V
C_{1a}	1.99 pF	C_{1b}	4.8 pF
C_{2a}	3.98 pF	C_{2b}	1.75 pF
Poles Frequency	100 MHz	Poles Frequency	100 MHz

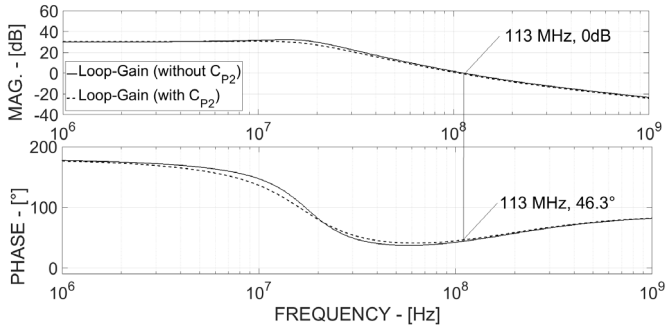


Figure 2. Flipped-source-follower loop-gain frequency response.

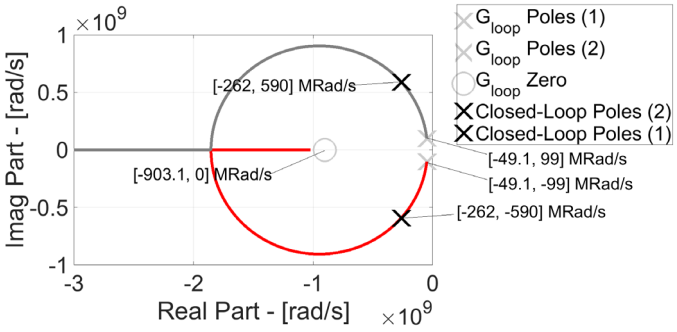


Figure 3. Flipped-source-follower root locus.

2.4. Biquad Linearity Performances

Inter-modulation (IM) distortions in FSF biquads are substantially set by M1 and M2. M3 operates as a current source and it does not introduce a relevant distortion contribution in its first approximation. The M1 IM distortion power ratio of the two components at $\omega_1 \pm \omega_2$ to the fundamental, called $IM_{3,M1}$ ($IM_{3,M2}$), is measured at the output of the FSF biquad and it is in first approximation depending on two key design parameters: the amount of M1 (M2) gate-source voltage swing (v_{gs1} and v_{gs2}) vs. the overdrive voltage and the loop gain [15,16]. Figure 4 shows v_{gs1}/v_{in} and v_{gs2}/v_{in} frequency responses extracted by the following transfer functions, referring to the scheme in Figure 1:

$$T_1(s) = \frac{v_{gs1}}{v_{in}}(s) = \cong \frac{1}{g_{m1} \cdot r_{ds3}} \cdot \frac{s^2 \cdot \frac{C_1 \cdot C_2 \cdot r_{ds1}}{g_{m2}} + s \cdot \frac{C_1}{g_{m1}} + 1}{s^2 \cdot \frac{C_1 \cdot C_2}{g_{m1} \cdot g_{m2}} + s \cdot \frac{C_1}{g_{m1}} + 1} \quad (6)$$

$$T_2(s) = \frac{v_{gs2}}{v_{in}}(s) = \cong -\frac{1}{g_{m2} \cdot r_{ds2}} \cdot \frac{1 + s \cdot C_2 \cdot r_{ds1}}{s^2 \cdot \frac{C_1 \cdot C_2}{g_{m1} \cdot g_{m2}} + s \cdot \frac{C_1}{g_{m1}} + 1} \quad (7)$$

Notice that:

- v_{gs1}/v_{in} magnitude frequency response has a −27 dB dc gain, two zeros, and two poles, inducing high-frequency 0 dB gain;
- v_{gs2}/v_{in} is −30 dB at low frequency, has one zero and two poles, and this implies −20 dB/decade high frequency drop.

It follows that the FSF biquad has low distortion power at low frequency (where the signal is lower, and the loop-gain is higher) and IM distortion increases at high frequency while approaching the closed-loop pole frequency.

Assuming to operate with both M1 and M2 MOSTs at $V_{OV1} = V_{OV2} = 75$ mV, $IM_{3,M1}$ and $IM_{3,M2}$ are given by:

$$IM_{3,M1} \cong \frac{3}{4} \cdot \left(\frac{v_{gs1}}{V_{OV1}}\right)^2 \cdot \frac{1}{G_{loop}} \quad (8)$$

$$IM_{3,M2} \cong \frac{3}{4} \cdot \left(\frac{v_{gs2}}{V_{OV1}}\right)^2 \cdot \frac{1}{G_{loop}} \quad (9)$$

where G_{loop} is the loop-gain of the biquad, whose transfer function is reported in Equation (5). As a result, Figure 5 shows $IM_{3,M1}$ and $IM_{3,M2}$ vs. frequency (with $v_{in1} = v_{in2} = 10$ $mV_{0\text{-PEAK}}$ amplitude, i.e., −30 dBm power-per-tone). The total IM_3 resulting from both M1-M2 distortion contributions is also plotted. IM_3 is dominated by the M1 MOST up to approximately 10 MHz, whereas from 10 MHz up to 100 MHz, the distortion contribution due to M2 MOST becomes more important.

Figures 4 and 5 curves were obtained by simulating a MATLAB small-signal model of the biquad B, whose main design parameters are listed in Table 2. IM_{3TOT} is −118 dB at low frequency, and it rises to −28 dB at 100 MHz; therefore, the resulting simulated input IP3 for the FSF biquad will range from 29 dBm at low frequency down to −2 dBm at 100 MHz, which is in line with the expected measurement results for single cell linearity.

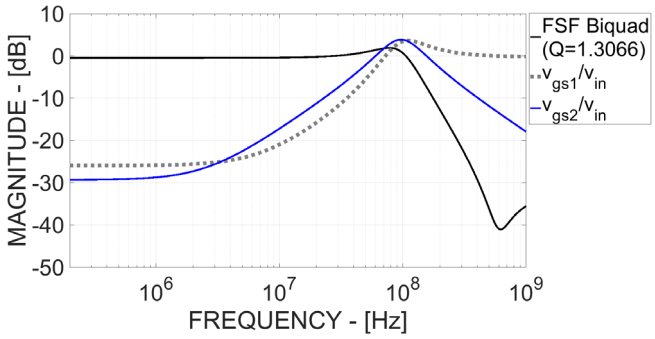


Figure 4. M1-M2 gate-source voltage vs. v_{in} frequency response.

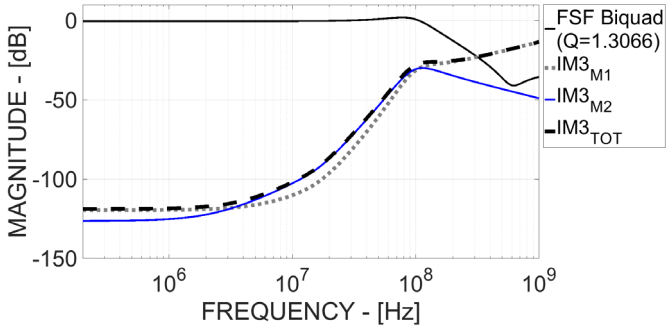


Figure 5. M1-M2 IM3 vs. $v_{in1} = v_{in1} = 10$ mV$_{0\text{-PEAK}}$.

2.5. Biquad Noise Performances

There are three noise sources that contribute to the final input referred noise (IRN) power spectral density:

$$IRN^2 \cong \frac{v_{n1}^2}{\Delta f} + \left(\frac{v_{n2}^2}{\Delta f}\right) \cdot \left(\frac{1}{g_{m1} \cdot r_{ds1}}\right)^2 + \left(\frac{v_{n3}^2}{\Delta f}\right) \cdot \left(\frac{g_{m3}}{g_{m1}}\right)^2 \cong \frac{16}{3} \cdot k \cdot T \cdot \frac{1}{g_{m1}} \cdot \left(1 + \frac{g_{m3}}{g_{m1}}\right) \quad (10)$$

Here, $\frac{v_{n1}^2}{\Delta f}$, $\frac{v_{n2}^2}{\Delta f}$ and $\frac{v_{n3}^2}{\Delta f}$ are M1, M2 and M3 MOST thermal noise voltage sources and they are in first approximation given by the following equation:

$$\left.\frac{v_{ni}^2}{\Delta f}\right|_{i=1,2,3} \cong \left.\frac{16}{3} \cdot k \cdot T \cdot \frac{1}{g_{mi}}\right|_{i=1,2,3} \quad (11)$$

For these MOSTs operating at the transition point between weak and moderate inversion regions, the characteristic transconductance can be in first approximation equal to $I_1/(n_N \cdot V_{Thermal})$ for n-channel MOST (or $I_1/(n_P \cdot V_{Thermal})$ for p-channel MOST devices). I_1 is the M1-M2-M3 common DC current, $V_{thermal}$ is 25 mV at room temperature, and n_N-n_P are the sub-threshold slope factors [17], which in first approximation are dependent on the MOST depletion layer and oxide capacitances).

Hence, Equation (10) can be simplified as follows:

$$IRN^2 \cong= \frac{16}{3} \cdot k \cdot T \cdot \frac{1}{g_{m1}} \cdot \left(1 + \frac{n_N}{n_P}\right) \quad (12)$$

Assuming $n_N \approx n_P$, the target of 7 nV/√Hz noise PSD for a fourth-order low pass filter (equivalent to 5 nV/√Hz noise PSD per-biquad), is achieved with $g_{m1} = 1.8$ mA/V at 242 µA bias current for each single branch cell.

3. Experimental Measurements Results

The transistor-level pseudo-differential scheme of the proposed filter is shown in Figure 6. The device has been integrated in 28 nm CMOS technology and fully characterized in terms of operating point, frequency, and time domain performances. The chip and layout photo are shown in Figure 7. The whole FSF filter occupies 0.026 mm^2.

The fourth-order filter cascades two biquad cells (Biquad A at Q = 0.5412 and Biquad B at Q = 1.3066).

The lower quality factor cell is placed at the beginning of the cascade, performing some filtering of the in-band and out-of-band power with the main aim of improving linearity performance (at the cost of a slight noise increase). Specific output buffers based on a PMOS source follower have been used to drive the output load (mainly capacitive and in the order of some pF).

The bias reference current is used to align the filter frequency response in front of CMOS process technological variations.

Total power consumption (excluding both bias circuit and output buffers) is 0.968 mW. The measured power consumption per biquad is 0.4356 mW (0.2178 mW per branch) for biquad A and 0.532.4 mW for biquad B (0.266.2 mW per branch).

Biquad B uses a slightly higher current because it should synthesize the higher quality factor, and intrinsically require more bandwidth.

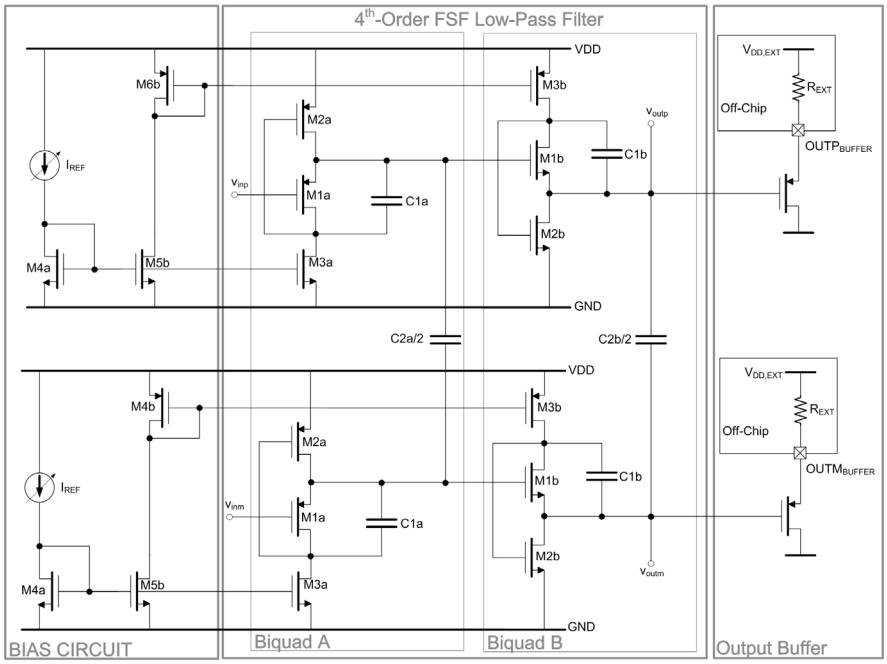


Figure 6. FSF transistor-level scheme.

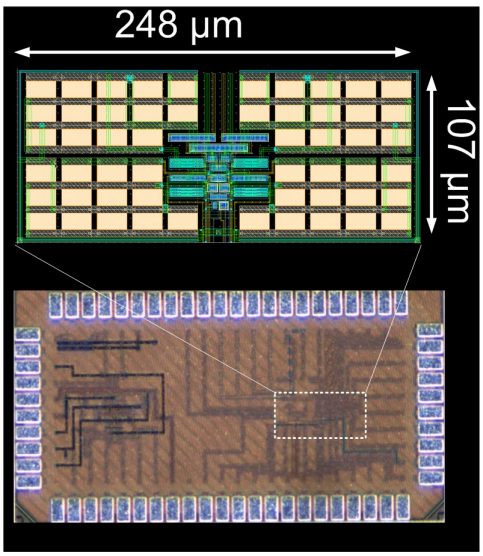
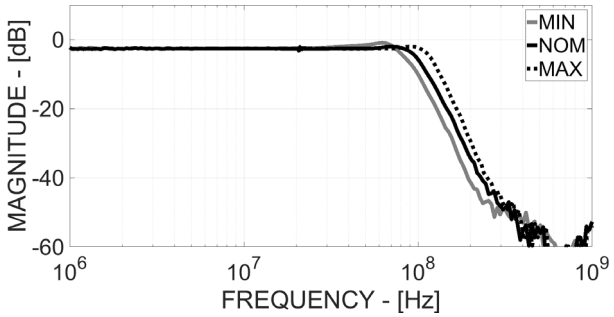


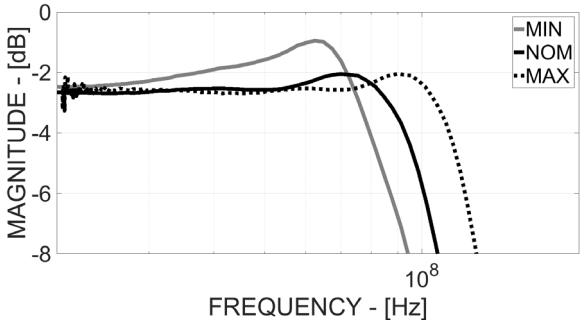
Figure 7. Chip Photo.

3.1. Frequency Response

Figure 8 shows whole pass-band (and pass-band right edge) filter frequency responses in nominal conditions (nominal I_{REF} of 10 µA) and with maximum and minimum currents (where I_{REF} is 12 µA and 8 µA, respectively). The filter DC gain is −2.5 dB. This drop is mainly due to the output buffer that has been biased to maximize bandwidth at the cost of a small gain reduction.



(**a**) Whole bandwidth frequency response.



(**b**) Bandwidth edge frequency response

Figure 8. Frequency responses.

The measured −3 dB frequency was 100 MHz at nominal I_{REF}, whereas it ranged from 85 MHz to 120 MHz for max. and min. I_{REF}. The maximum in-band ripple was +1.5 dB for max IREF frequency response, and it was lower than 0.5 dB for the minimum and nominal I_{REF}.

3.2. Linearity Performance

The filter linearity has been characterized by single and double tone tests. The output spectrum of a 0.33 $V_{0\text{-}PEAK}$ output signal at 20 MHz input frequency is shown in Figure 9. The third-order harmonic distortion is dominant, and it is equal to −49.5 dB, resulting in a Total-Harmonic-Distortion (THD) of −40 dBc.

The total output noise power is 98 μV_{RMS}. In this way, the final FSF filter DR for −40 dBc@THD is 67.6 dB, which is, in some cases, better than the state-of-the-art analog filters in the literature, as illustrated in Table 3 [2,4,5,10–14,17–20].

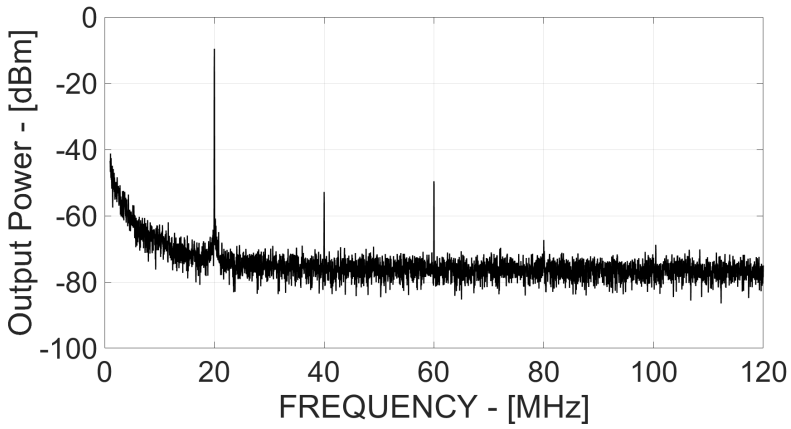


Figure 9. Output spectrum at 20 MHz input signal.

Table 3. Comparison with state-of-the-art filters.

Param.	This Work	[2]	[4]	[5]	[10]	[11]	[12]	[13]	[14]	[17]	[18]	[19]	[20]
Order	4th	4th	4th	4th	5th	5th	5th	5th	6th	6th	2nd	4th	4th
Technology [nm]	28	180	180	180	130	180	130	120	90	180	130	65	45
Supply [V]	1	1.8	1.35	1.3	1.2	1.8	1.2	1	1	1.8	1.2	1.8	
Power [mW]	0.96	1.38	0.62	0.65	7.5	5.6	11.2	6.1	4.3	4.7	20.	19	5.1
DC gain [dB]	−3.2	0	0	0	0	0	2	0	−2.7	0	-	0	
BW [MHz]	100	33	31	20	20	20	19.7	5	13.5	500	200	16	12.6
IRN [nV/√Hz]	8	7.8	22	15.3	52	-	30	139	75	66.2	21.8	44.6	
Noise [μV_{RMS}]	98	45	122	68.4	285	1040	80	312	270	240	495	189.6	31
THD [dB]	−40	−40	-	-	−40	-	−9	−40	−40	-	−40	-	
V_{OUT} [$V_{0\text{-}PEAK}$]	0.33	0.225	-	-	0.223	-	0.375	0.355	0.475	-	0.375	-	
SNR [dB]	67.6	70	-	-	-	-	70.4	-	61.8	-	54	-	
IIP [dBm]	4–13.5	18	23	17	31.3	27.5	20.35	20	22.1	11.5	14	22.1	26.8
1dBCP [dBm]	2.6	8	-	7.3	-	-	2.9	3.6	7.6	-	-	8	
FoM [dBJ^{-1}]	160 (161)	156	159.2	159	142	146.9	143	146.5	145	144	146	148	157

Importantly, this FSF filter maintains the SNR performance compared with state-of-the-art analog devices, even when using the most scaled-down technology.

The 1 dB compression point (1dB-CP) of 2.6 dBm (0.426 $V_{0\text{-}PEAK}$ output voltage) has been measured, and the corresponding input/output characteristics are shown in Figure 10.

Figures 11 and 12 show the two-tone output spectra for 10 and 11 MHz and 50 and 55 MHz input tones frequency.

The third-order intermodulation product is −46 dB and −40 dB, respectively (with a two output iso-power tones of −14 dBm and −20 dBm).

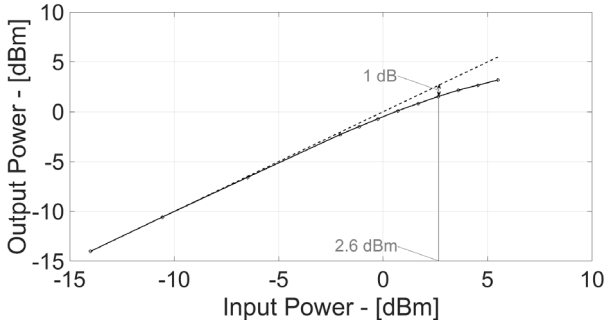


Figure 10. 1 dB compression point at 20 MHz input signal.

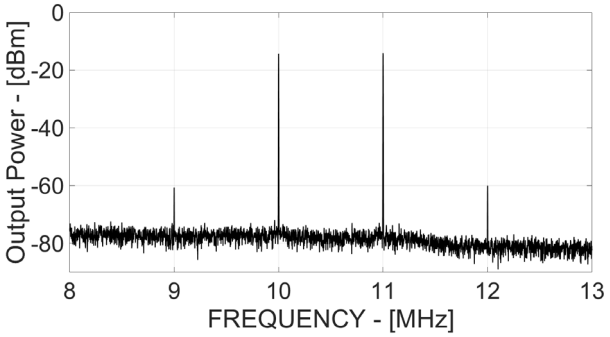


Figure 11. Output spectrum with 10 and 11 MHz Input Signal.

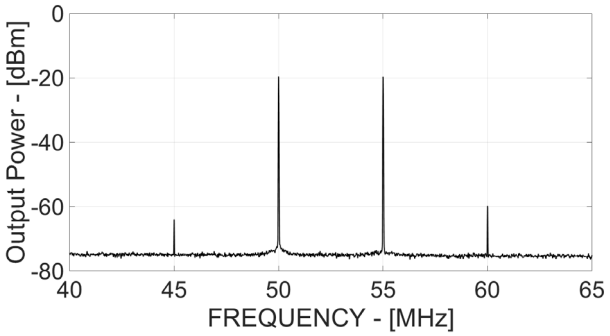


Figure 12. Output spectrum with 50 and 55 MHz input signal.

This gives an input IP3 of 13.2 dBm and 4 dBm at 10 and 11 MHz and 50 and 55 MHz input tones frequency, respectively, as shown in Figures 13 and 14.

Finally, this filter has been compared with the state-of-the-art filters by adopting the following figure-of-merit (FoM [2]):

$$FoM = 10 \cdot log_{10} \frac{IMFDR_3 \cdot f_{-3dB} \cdot N}{PW} \cdot \frac{f_{IM3,LOW}}{f_{POLES}} \quad (13)$$

where PW is the total power consumption, f_{-3dB} is the cut-off frequency, N is the number of poles, and $IMFDR3$ is the spurious-free IM3. Such FoM takes into account the distance of the inter-modulation products from the pole frequencies by including the ratio between the lower frequency third-order inter-modulation tone ($f_{IM3,LOW}$) and the pole frequency (f_{POLE}S), as discussed in [2].

The filter achieves the significant 160 and 161 dBJ^{-1} FoM (for 10 and 11 MHz and 50 and 55 MHz, respectively, as shown in Figure 15), outperforming analog filter implementations in scaled nodes (<130 nm), enabling 28 nm CMOS analog filters for future telecommunications wireless transceivers.

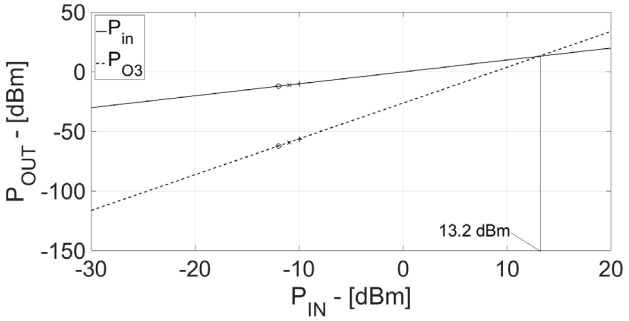


Figure 13. Input IP3 at 10 and 11 MHz input signal.

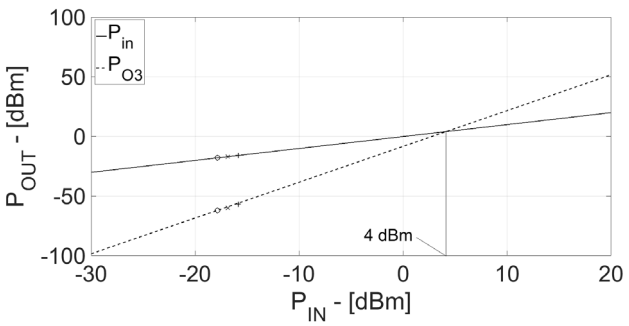


Figure 14. Input IP3 at 50 and 55 MHz input signal.

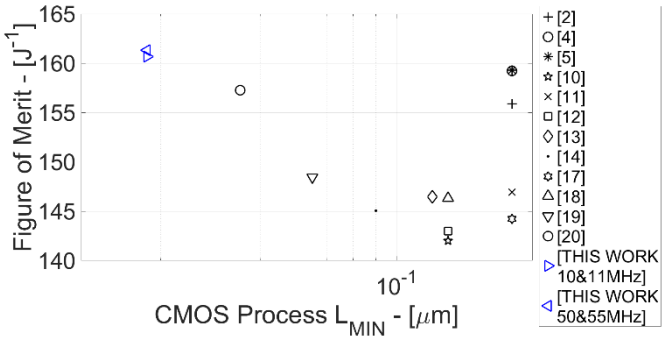


Figure 15. Figure-of-merit vs. CMOS L_{MIN}.

4. Conclusions

In this paper, both complete design and electrical/experimental characterization of a fourth-order flipped-source-follower filter have been presented. The device synthesizes a fourth-order low-pass Butterworth transfer function at 100 MHz −3 dB frequency using a single cascode stack, optimizing a noise/power trade-off and improving matching comparing with source-follower state-of-the-art analog filters. Moreover, this paper proposes the most scaled-down CMOS implementation of FSF filters operating with the lower supply voltage (1 V). The device achieved one of the better FoM (and the most scaled CMOS process) compared with the state-of-the-art filters (160 dBJ^{-1}).

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