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The Design Methodology of Fully Digital Pulse Width Modulation

Fadi R. Shahroury

Department of Electrical Engineering, Princess Sumaya University for Technology, Amman 11941, Jordan; fadi@psut.edu.jo

Abstract: This paper describes the design methodology and calibration technique for a low-power digital pulse width modulation demodulator to enhance its robustness against the process, voltage, and temperature variations in different process corners, in addition to intra-die variability, which makes it a very good choice for implantable monitoring sensors. Furthermore, the core of the proposed demodulator is fully digital. Thus, along with the proposed design methodology, the proposed demodulator can be simply redesigned in advanced subnanometer CMOS technologies without much difficulty as compared to analog demodulators. The proposed demodulator consists of an envelope detector, a digitizer, a ring oscillator, and a data detector with digital calibration. All the proposed circuits are designed and simulated in the standard 1P9M TSMC's 40 nm CMOS technology. Simulation results have shown that the circuit is capable of demodulating and recovering data from an input signal with a carrier frequency of 13.56 MHz and a data rate of 143 kB/s with an average power consumption of 5.62 µW.

Keywords: implantable devices; pulse width modulation (PWM); 13.56 MHz; glucose monitoring

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1. Introduction

Diabetes is a lifelong metabolic disorder that weakens the human body's ability to process blood sugar. Building up sugars in the blood can lead to serious complications such as stroke, blindness, heart diseases, kidney failure, and lower limb amputation. Despite diabetes being an incurable condition, careful and ongoing monitoring of diabetes along with appropriate diet and medication can help patients to stay healthy. The diabetes incidence rate is increasing every year, and according to the World Health Organization (WHO) report (2021), there are approximately 422 million confirmed cases worldwide, mostly in low- and middle-income countries [1,2]. It is expected that over 693 million people will be exposed to this lifetime disease by 2045 if proper actions are not taken [3,4].

The most effective drug for controlling the blood glucose level of diabetics is insulin, and this drug needs to be delivered to the blood. Traditional methods for delivering insulin to the human blood usually involve some form of invasive injection or oral therapy and these are regarded as painful or unpleasant by most patients [5,6]. To overcome this problem and enhance adherence to insulin regimens, transdermal drug delivery (TDD) has been widely used. TDD stands out as a more favorable option, due to its non-invasive and painless approach. It is accomplished by increasing the permeability of the skin to insulin, through which insulin can be applied and then absorbed, eventually entering the blood. This method offers an important advantage due to the ease of accessibility to the skin and has attracted the attention of researchers and diabetics [7,8].

The skin consists of two main layers: the epidermis and the dermis. The epidermis is divided into two sub-layers which are the stratum corneum and the living epidermis. The outer layer of the skin, the stratum corneum, causes the low permeability of the skin to TDD [9]. Many methods have been used to overcome the low permeability of the skin such as mechanical methods [10] (microneedles, abrasion, perforation, and skin stretching) and electrical-assisted methods [11] (iontophoresis, electroporation, and radiofrequency) [12].

However, other promising physical methods such as ultrasound [13] can be used to increase the permeability of the skin in a phenomenon referred to as sonophoresis [14].

The effectiveness of the ultrasound technique depends on many controlled parameters, such as the intensity, the net exposure time, and the on-off ratio of the in vivo delivery of insulin, but also depends on a number of uncontrolled parameters such as the hair concentration on the skin, the thickness of the stratum corneum, and humidity [15]. These parameters can cause varying levels of insulin absorption through the skin, and the amount of insulin that reaches the blood would be hard to control. In order to overcome this problem, real-time monitoring of the insulin level in the blood can provide a feedback mechanism for accurately controlling the amount of insulin that is injected into the blood. Moreover, if the blood glucose concentration can also be monitored in real-time, it can be used to trigger the injection of insulin automatically. This would allow for the realization of a self-controlled ultrasound system that delivers insulin to the blood automatically according to instant glucose and insulin levels within the blood, without the involvement of the patient. This self-controlled technique deploys implantable glucose and insulin biosensors as the main building blocks of the entire system.

Implantable biosensor devices are of great importance for monitoring internal body parameters such as electrocardiogram data [16], pressure levels [17], gastrointestinal parameter values (pH, temperature, pressure) [18], and blood glucose [19], to name a few. In these systems, implantable sensor units transmit data to an external reader device and then to a control unit (computer) or a central monitoring unit for data analysis [20].

Figure 1 illustrates a possible implementation for a self-controlled ultrasound insulin delivery system. In the red-dashed box, the portable external reader device transmits a modulating signal through inductive coupling coil L1. The implantable monitoring sensor (IMS) receives the modulating signal through the internal coil (L2). The IMS includes a demodulator, internal clock generator, power management circuitry, biosensor, digital control circuitry, and backscattering modulator.

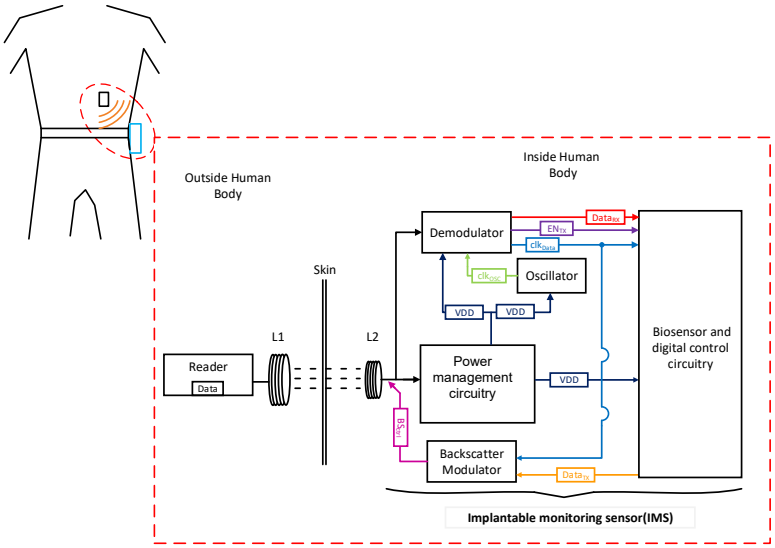

Figure 1. The block diagram of self-controlled ultrasound insulin delivery system.

In IMS, the PWM modulation scheme has been intensively used, primarily because of the low power consumption and the simplicity of its demodulator circuitry [21]. However, designing a demodulator for PWM in advanced CMOS technologies, such as 40 nm, is a challenging issue. This is mainly due to the high sensitivity of advanced CMOS technologies for the process, supply voltage, and temperature variation (PVT), besides intra-die variability [22,23]. On the other hand, the size of the IMS is dominated by on-chip capacitors. A high on-chip capacitance density (metal-oxide-metal capacitor) makes advanced CMOS technologies attractive for IMS [24,25].

This article is a continuation of the author's work published in [26], where the passive transponder front-end for IMS was proposed. However, the design methodology of the digital PWM demodulator (DPWMD) was not discussed despite its importance. Therefore, this article discusses the design methodology of a low-power DPWMD to enhance its robustness against PVT variations in different process corners. Additionally, a calibration technique is utilized to minimize the impact of PVT variations and intra-die variability. The proposed DPWMD consists of an envelope detector, a digitizer, a ring oscillator, and a data detector with digital calibration. The proposed DPWMD is designed and simulated using 40 nm 1P9M TSMC's CMOS technology. Simulation results have shown that the circuit is capable of demodulating and recovering data from an input signal with a carrier frequency of 13.56 MHz and a data rate of 143 kB/s with an average power consumption of 5.62 µW.

This paper is organized as follows. Section 2 presents the proposed DPWMD, and Section 3 describes the overall design methodology for the proposed demodulator. Results and analysis are discussed in Section 4, followed by the conclusion and remarks in Section 5.

2. Proposed DPWMD

Figure 2 shows the timing diagram of the proposed DPWMD. The top trace shows the typical modeling waveforms of the proposed PWM, each gap representing a clock pulse transition. The duration of the gap represents either a logic "one" or "zero" transition depending on the duration of the gap width. The demodulator interprets long/short durations as logic "one"/"zero". To solve PVT variations and intra-die variability issues, a calibration mode is introduced. This mode is activated at the beginning of the transmission by sending three successive gaps followed by the calibration gap. The second trace from the top illustrates the extracted data clock (*clk*), the third trace from the top depicts the extracted data (*Data*), and the bottom trace shows the ring oscillator (clk_{osc}) that is used to measure the gap duration.

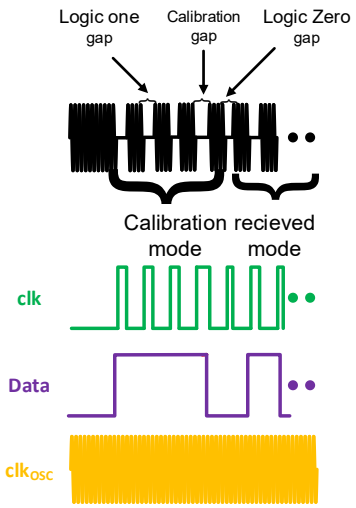

Figure 2. Waveform timing description of the proposed PWM.

The basic block diagram of the proposed DPWMD is illustrated in Figure 3. The PWM demodulation is done by an envelope detector, a digitizer, a ring oscillator, and a data detector with digital calibration. The implementation details and design considerations are presented in the following sections.

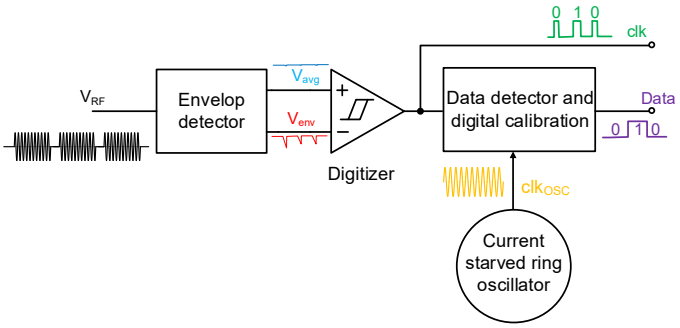

Figure 3. Implemented DPWMD architecture.

2.1. Envelope Detector

The functionality of the envelope detector circuitry is to generate two output signals: the V_{env} and its average V_{avg} from the received modulating signal [27], as shown in Figure 4. The three diode-connected devices M1–M3 are used to detect the presence of the gaps in the received modulating signal, and C1–C3 are storage capacitors. During the gap duration, M4 and M5 provide a path to discharge C1 and C2. In addition, to enhance noise immunity, V_{avg} is shifted below V_{env} through connecting the drains of M2 and M3.

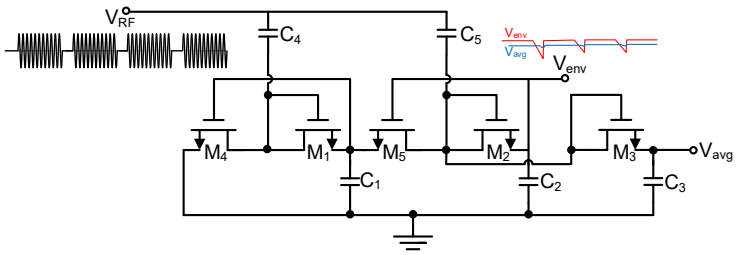

Figure 4. Schematic of envelope detector.

2.2. Digitizer

The digitizer is principally a comparator or more precisely a Schmitt trigger [28]. The digitizer has two switching points: upper and lower trip points UTP and LTP, respectively. When V_{env} is lower than V_{avg} by the amount of UTP, the output voltage pulse is high. This output voltage continues to be high until V_{env} rises again above V_{avg} by the amount of LTP. The digitizer generates pulses with variable durations. The presence of the pulse corresponds to a transition in the transmitted data. Thus, the output of the digitizer can be considered as a data clock (*clk*). Furthermore, the duration of the pulse can be used to identify whether logic "one" or "zero" has been transmitted. The schematic of the proposed digitizer is depicted in Figure 5.

2.3. Ring Oscillator

The designed ring oscillator is based on the current-starved inverter structure. As shown in Figure 6, it consists of three starved inverters, G1, G2, and G3, connected in the ring structure followed by a simple inverter, G4 and G5, to sharpen the edges of the output signal (clk_{OSC}). This circuit provides an on-chip clock signal to measure the duration of the gaps and to distinguish between long and short gaps. However, it is obvious that the frequency of the oscillator is highly effected by PVT variations and intra-die variability issues. Thus, a calibration technique is introduced to solve this issue.

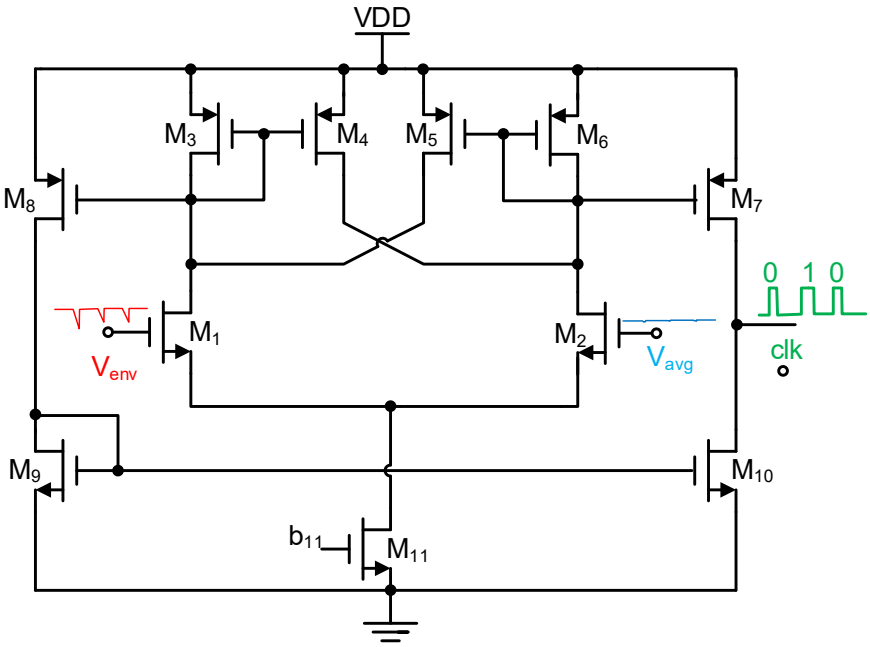

Figure 5. Schematic of digitizer.

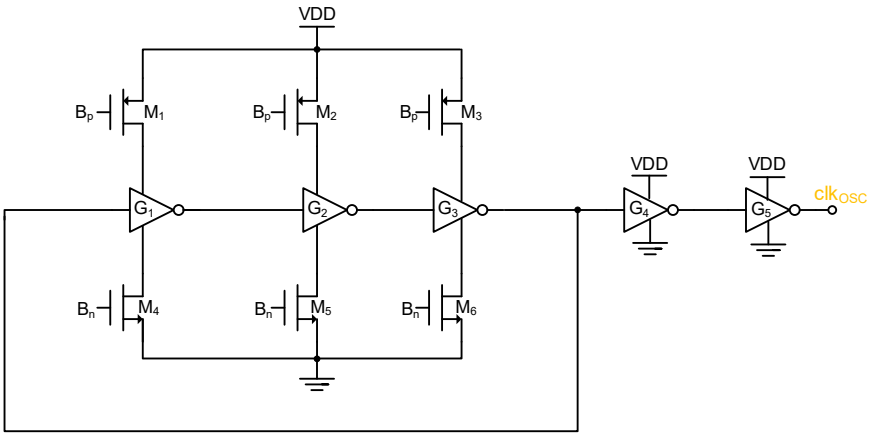

Figure 6. Schematic of the ring oscillator based on current-starved inverter structure.

2.4. Data Detector with Digital Calibration

The main function of this block is to distinguish between long and short-duration digitizer output pulses (*clk*) by using the clk_{OSC}. To minimize the error due to the PVT variations and the intra-die variability, the binary decision threshold principle has been employed. If the duration of the *clk* pulse is greater than or equal to T_{cal}, then the *clk* pulse is interpreted as a long gap (logic one). Otherwise, the *clk* pulse is interpreted as a short gap (logic zero). This simple methodology minimizes the probability of making an incorrect decision in determining the pulse duration, even with the presence of the PVT variations and the intra-die variability.

Figure 7 shows the data detector with digital calibration. The gap discrimination is done by a digital counter, a threshold register, a comparator, and a calibration circuitry. The digital counter is clocked by the clk_{OSC} signal and enabled by the *clk* signal. Thus, it counts the duration of the *clk* pulse in terms of the clk_{OSC} pulses. At the end of the *clk* duration, the content of the digital counter is N_c. The threshold register stores a binary number (N_{th}) corresponding to T_{cal}. The comparator provides an output that assumes one of two distinct values based on N_c and N_{th}: high voltage (logic one) when $N_c \geq N_{th}$ (long pulse) and low voltage (logic zero) when $N_c < N_{th}$ (short pulse). Finally, the calibration circuitry is used to detect the calibration mode pattern which consists of three successive long-duration pulses.

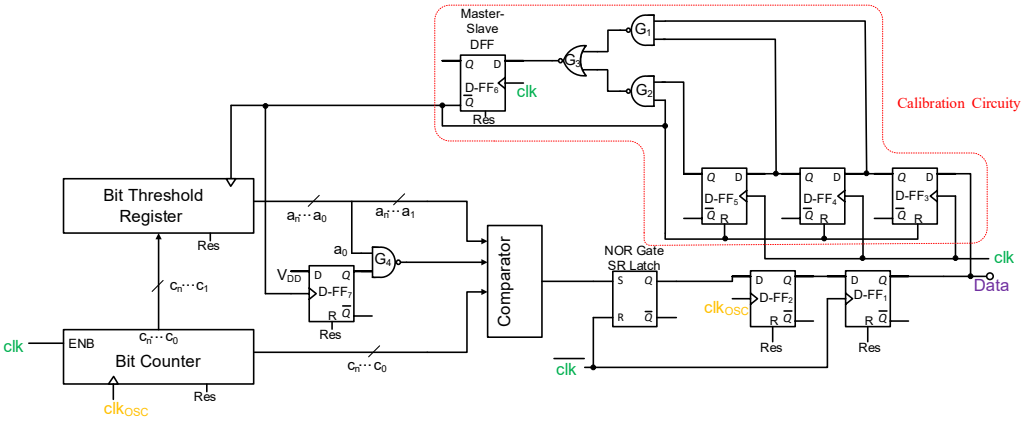

Figure 7. Schematic of data detector with digital calibration.

When the calibration circuitry detects the calibration pattern, the threshold register stores the half value of the digital counter which corresponds to the duration of T_{cal}. This can be simply done by transferring the content of the digital counter after dropped the least significant bit (LSB) to the threshold register.

3. Design Issues and System Parameters

This section introduces all the parameters that need to be considered to design the proposed DPWMD, such as the time duration of the gap representing logic zero (T_0), the time duration of the gap representing logic one (T_1), the time duration of the calibration gap (T_{cal}), the size of the digital counter (DC_{size}), and the size of the threshold register (ThR_{size}).

As mentioned previously, the time duration of a gap T_g is determined by the digital counter for N clock cycles of the clk_{OSC} signal. N is an integer number, and it is given for a positive-edge-triggered counter as

$$N = \lfloor T_g f_{clk_{OSC}} \rfloor , \tag{1}$$

where $\lfloor . \rfloor$ is denoted for the floor function. It is obvious that $f_{clk_{OSC}}$ is highly affected by PVT variations and intra-die variability. Therefore, for a fixed gap duration, N is not defined as a single value, but it is defined as an element in the set of candidate values.

As illustrated in Figure 8, there are three candidate sets of integers: logic zero set $\mathbb{N}_0 = [N_{0,min}, N_{0,max}]$ is interpreted as a logic zero, logic one set $\mathbb{N}_1 = [N_{0,min}, N_{0,max}]$ is interpreted as a logic one, and threshold set $\mathbb{N}_{th} = [N_{th,min}, N_{th,max}]$ which used to discriminate between set $\mathbb{N}_0$ and $\mathbb{N}_1$. The boundary elements of $\mathbb{N}_0$ ($N_{0,min}$ and $N_{0,max}$) can be described by

$$N_{0,min} = \lfloor T_0 f_{min} \rfloor , \tag{2}$$

$$N_{0,max} = \lfloor T_0 f_{max} \rfloor . \tag{3}$$

where f_{max} and f_{min} are the maximum and minimum frequencies of clk_{OSC} due to PVT variations, respectively. In the same way, the boundary elements of $\mathbb{N}_1$ ($N_{1,min}$ and $N_{1,max}$) can be found by substituting T_1 instead of T_0 in Equations (2) and (3), respectively. The boundary elements of $\mathbb{N}_{th}$ ($N_{th,min}$ and $N_{th,max}$) are given as

$$N_{th,min} = \left\lfloor \frac{\lfloor T_{cal} f_{min} \rfloor}{2} \right\rfloor , \tag{4}$$

$$N_{th,max} = \left\lfloor \frac{\lfloor T_{cal} f_{max} \rfloor}{2} \right\rfloor . \tag{5}$$

For proper operation, two conditions must be satisfied: first $N_{th,min} > N_{0,max}$ and second $N_{1,min} > N_{th,max}$. Thus, T_{cal} must be

$$\frac{T_1}{\alpha} > \frac{T_{cal}}{2} > T_0\alpha \, . \tag{6}$$

where $\alpha = \frac{f_{max}}{f_{min}}$. The above equation implies that $T_1 > T_0\alpha^2$. To simply achieve the requirement in Equation (6), T_{cal} is given as

$$T_{cal} = \frac{T_1}{\alpha_c} + T_0\alpha_c \, . \tag{7}$$

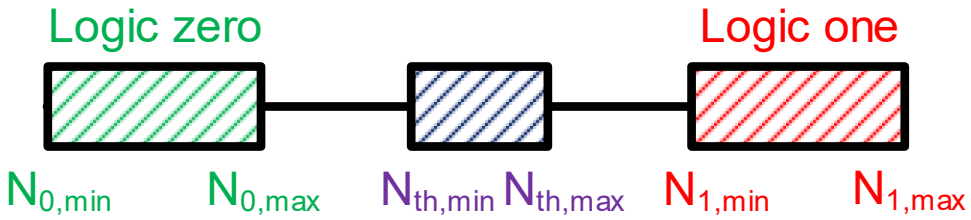

Figure 8. Logic zero set ($\mathbb{N}_0$), logic one set ($\mathbb{N}_1$), and threshold set ($\mathbb{N}_{th}$).

The design methodology of the proposed DPWMD is illustrated in the flowchart shown in Figure 9. In this methodology, the calculation of the parameters is done for the worst-case condition. The first step starts with simulating the ring oscillator for PVT variations in different process corners. Once the simulation results are done, α_{max} and f_l can be determined as defined in the flowchart. In the next step, α_c is selected to be greater than about α_{max}. At the same step, the lowest digital counter reading (DC_{min}) (that propositional to T_0 under low clock frequency condition (f_l)) is defined. It is worth noting that the value of T_{cal} should be less than the bit interval (in our case, $1/(143\text{ kB/s}) \approx 7\ \mu\text{s}$). In addition, to simplify the design of the power management circuitry, T_1 should be at least less than 20% of the bit interval to preserve the continuity of the carrier signal [27].

Once the values of T_o, T_1, and T_{cal} are calculated, $N_{0,max}$, $N_{1,min}$, $N_{th,min}$, and $N_{th,max}$ can be found as defined in Equations (1)–(5). If $N_{0,max}$, $N_{1,min}$, $N_{th,min}$, and $N_{th,max}$ are overlapped, then the assumed values of α_c, DC_{min}, or both of them should be changed. In addition, the previously mentioned steps must be repeated. If there are no overlaps in $N_{0,max}$, $N_{1,min}$, $N_{th,min}$, and $N_{th,max}$, then $N_{1,h}$ can be found as defined in the flowchart. In the last step, the size of the counter and the threshold register are determined as defined in the flowchart, where $\lceil . \rceil$ is denoted for the ceiling function.

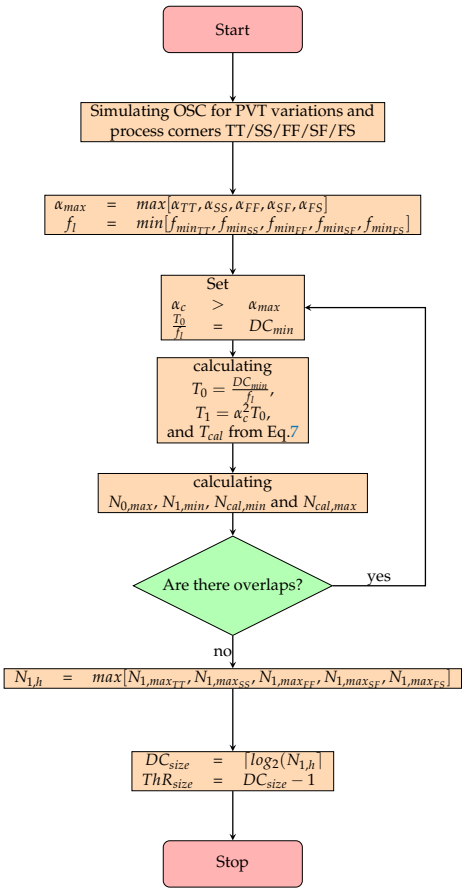

Figure 9. Design procedure for the proposed digital PWM demodulator.

4. Simulation Results and Discussion

The proposed DPWMD is designed and simulated in 1P9M TSMC's 40 nm CMOS process technology. The demodulator is simulated with a carrier frequency of 13.56 MHz, a data rate of 143 kB/s, and a nominal supply voltage of 0.9 V.

As mentioned earlier, the proposed DPWMD utilizes the ring oscillator's frequency to measure the duration of the gaps to discriminate between long and short gaps. Thus, for proper operation, the worst-case condition due to PTV variation of the ring oscillator should be identified. However, in IMS, temperature variations are not an issue since the human body temperature is self-regulated [29]. Therefore, the oscillator frequency variations due to supply voltage changes ($\pm$100 mV from the nominal value of 0.9 V) at TT, SS, FF, SF, and FS process corners are simulated, as shown in Figure 10.

To tolerate the frequency variations, the design methodology described in the last section is followed. From the illustrated simulation results, $\alpha_{max} = 1.46$, and $f_l = 16$ MHz, so the values of α_c and DC_{min} have been selected to be 1.6 and 6, respectively. For the selected values, $T_0 = 0.4$ µs, $T_1 = 1$ µs, and $T_{cal} = 1.3$ µs.

The calculated $\mathbb{N}_0$, $\mathbb{N}_1$, and $\mathbb{N}_{th}$ sets at each process corner are listed in Table 1. As noted, there are no overlaps between sets for the selected values. In addition, the value of $N_{1,h} = max[24, 24, 32, 23, 35] = 35$. Therefore, the size of the counter and threshold registers have been chosen to be 6 bits and 5 bits, respectively.

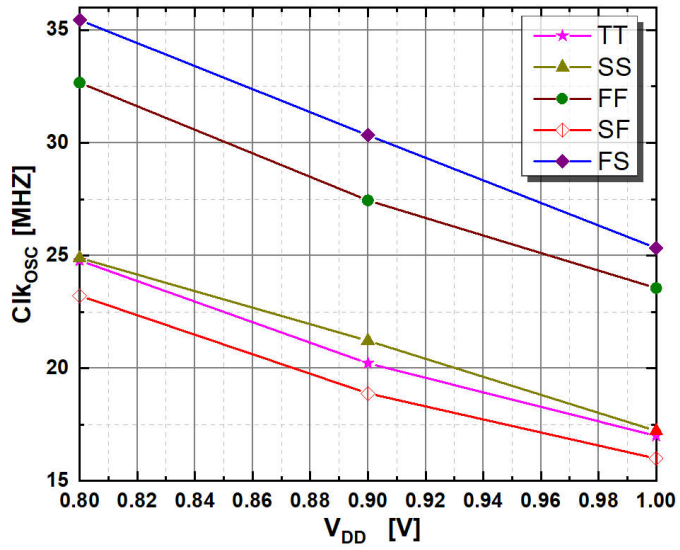

Figure 10. Simulation results of the ring oscillator frequency due to supply voltage variation at each process corner.

Table 1. The calculated $\mathbb{N}_0$, $\mathbb{N}_1$, and $\mathbb{N}_{th}$ sets at each process corner.

	$N_{0,min}$	$N_{0,max}$	$N_{th,min}$	$N_{th,max}$	$N_{1,min}$	$N_{1,max}$
TT	6	9	11	16	17	24
SS	6	9	11	16	17	24
FF	9	13	15	21	23	32
SF	6	9	10	15	16	23
FS	10	14	16	23	25	35

The transient simulation results of the proposed DPWMD are shown in Figure 11. It can be noticed that the proposed DPWMD extracted the data clock (*clk*) and *Data signal* from the RF carrier signal. The proposed demodulator can function accurately under a supply voltage variation of ±100 mV from the nominal value of 0.9 V. The demodulated signal starts with three successive bits to enable the calibration mode, followed by a calibration pulse. After the calibration pulse period is measured using the internal signal, the proposed demodulation can successfully distinguish between long and short gaps, even with supply voltage variations.

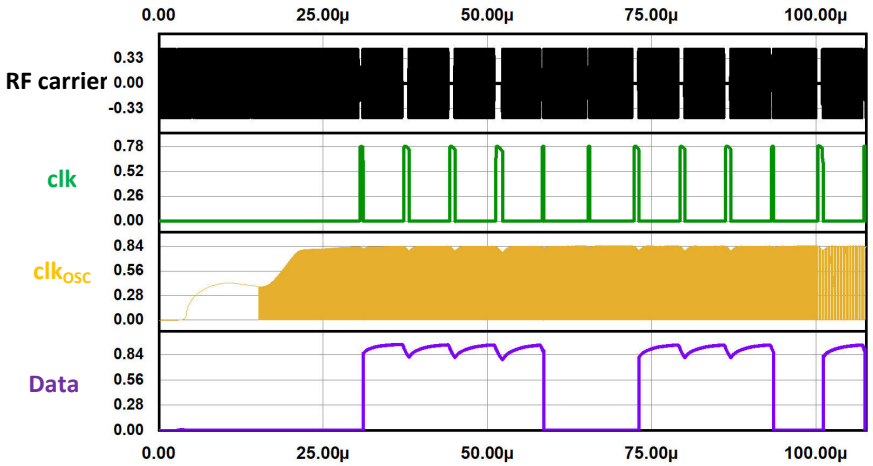

Figure 11. The transient simulation results of proposed demodulator circuit.

The proposed design has a total average power consumption of 5.62 µW. The average power consumption of the demodulator is 3.32 µW, while the envelope detector, digitizer, and ring oscillator consume 2.3 µW.

Table 2 shows a list of useful and necessary features of the proposed demodulator. A brief comparison is drawn among the different published articles and this work in supporting these features. It is clear from the table summary that the proposed demodulator of this work has a high energy efficiency with an FoM of 39.3 pJ/bit.

Table 2. Performance parameters comparison with the literature.

	[30]	[31]	[32]	[33]	This Work
Process node (nm)	350	180	180	350	40
Carrier (MHz)	13.56	13.56	13.56	13.56	13.56
Modulation scheme	ASK	PPM	ASK	ASK	PWM
Supply voltage (V)	3	1.8	1.8	3∼3.6	0.9
Data rate (Mbps)	0.7	0.00813	6.78	0.42375	0.143
Power (uW)	76.5	27.8	396	450	5.62
FoM [a] (pJ/bit)	109.3	3419	58.4	1062	39.3

[a] FoM = Power/Data Rate.

5. Conclusions

This paper describes the design methodology and calibration technique for a low-power digital pulse width modulation demodulator to enhance its robustness against the process, voltage, and temperature variations in different process corners, in addition to intra-die variability, which makes it a very good choice for implantable monitoring sensors. The proposed demodulator consists of an envelope detector, a digitizer, a ring oscillator, and a data detector with digital calibration. The transient simulation results showed that the proposed demodulator can function accurately under a supply voltage variation of ±100 V from the nominal value of 0.9 V. Furthermore, the core of the proposed demodulator is fully digital. Thus, along with the proposed design methodology, the proposed demodulator can be simply redesigned in advanced subnanometer CMOS technologies without much difficulty as compared to analog demodulators.

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Conflicts of Interest: The author declares no conflict of interest.

Abbreviations

The following abbreviations are used in this manuscript:

CMOS	Complementary Metal–Oxide–Semiconductor
WHO	World Health Organization
PWM	Pulse Width Modulation
ASK	Amplitude Shift Keying
PPM	Pulse Position Modulation
PVT	Process, Voltage, and Temperature Variations
TTD	Transdermal Drug Delivery
IMS	Implantable Monitoring Sensor
DPWMD	Digital PWM Demodulator
LSB	Least Significant Bit

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