

Article

An Improved CMOS Design of Op-Amp Comparator with Gain Boosting Technique for Data Converter Circuits

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Abstract: A modified architecture of a comparator to achieve high slew rate and boosted gain with an improvement in gain design error is introduced and investigated in this manuscript. It employs the conventional architecture of common-mode current feedback with the modified gain booster topology to increase gain, slew rate, and reduced gain error from the conventional structure. Observation from the simulation results concludes that the modified structure using 24 transistors shows power dissipation of 362.29 μ W in 90 nm CMOS technology by deploying a supply voltage of 0.7 V, which is a 70% reduction as compared to the usual common mode feedback (CMFD) structure. The symmetric slew rate of 839.99 V/ μ s for both charging and discharging is obtained, which is 173% more than the standard CMFD structure. A reduction of 0.61% in gain error is achieved through this architecture. A SPICE simulation tool based on 90 nm CMOS technology is employed for executing the Monte Carlo simulations. A brief comparison with earlier CMFD structures shows improved performance parameters in terms of power consumption and slew rate with the reduction in gain error.

Keywords: cascode; current mirrors; power consumption (PC); common mode feedback (CMFD); gain boosting (GB); complementary mosfet technology (CMOS)

1. Introduction

One of the most significant and critical elements of analog integrated circuits are comparators [1,2]. Comparators play a pivotal role in regulating the decisive parameters of many imperative analog and digital circuits [3]. Data converters are one such kind of circuit as their speed of conversion, resolution, and power consumption, along with other prominent parameters, depends directly on it [4–6]. The CMOS fabrication technologies have entered the submicron domain, and transistor sizing is scaling down to nano-dimension levels. This, in turn, restrains the maximum power supply voltage in ICs eventually allowing an audit of the fidelity of these MOS transistors [6–8]. This effect is positive for digital ICs, but has an adverse impact on analog ICs. The primary consequences of this scaling are reduced output conductance and small output voltage swing and, hence, led to decreased DC gains [9]. Thus, the op-amp comparators designed under such CMOS technologies with restrained supply voltage will not be able to comply with the designer requisites and, thus, adversely affect the performance parameters of abstract circuits that employ these comparators as their core element [10]. Data converters, such as ADC and DAC conversion speed and accuracy, sturdily depend upon the comparator's capability to detect the smallest voltage levels [11,12]. The op-amp comparators with a

high slew rate and high gain with high accuracy are to be designed in order to attain these excellent parameters in data converters [13,14].

A modified architecture is proposed in this paper, which suggests useful data information in understanding the performance of op-amp comparators. Better optimization for providing an accurate differential mode gain and high slew rate is achieved through this design [14]. Thus, to meet the requirement of gain in the op-amp comparator modified architecture with gain a boosting block is used. Common mode feedback (current feedback) is used in the circuit of the op-amp comparator to maintain the output node at constant DC [15]. Current biasing of the modified design is done by using current mirrors [16]. The common mode feedback with modified architecture and gain boosting block provides a very high gain with an improved gain error by more than 95% [17]. The use of the cascode current mirror structure in the current feedback amplifier, in addition to the high gain, also provides a very high slew rate [18].

This manuscript is further assembled as follows: Section 2 dispenses a quick overview of the modified circuit description in the form of a circuit. Section 3 provides details about the simulation results and explanations of the analysis of the modified architecture. Section 4 contains comparisons of the modified architecture with existing op-amp comparators, like DCFIA, SCFIA [19], and CMFD [20–23], which utilize common mode current feedback through tables and graphs. The paper concludes with Section 5.

2. Circuit Description

Figure 1 depicts the block architecture for common-mode feedback structure [20]. It incorporates three major blocks. First, there is a fully differential pair amplifier that works in balanced mode. Next, there is a sensing circuit stage which senses common mode output signal. In the final stage, there is a comparator which compares this output common mode signal with a reference voltage and feeds the rectified signal back to the fully differential pair that, in turn, adjusts according to this signal [21]. The reference voltage ideally equals 0 V. Thus, a rectified signal is formed and applied to the fully differential pair, such that, finally, the alteration signal becomes near to zero. The rectified signal is a subtracted value taken by subtracting the reference voltage and the common-mode signal [22,24].

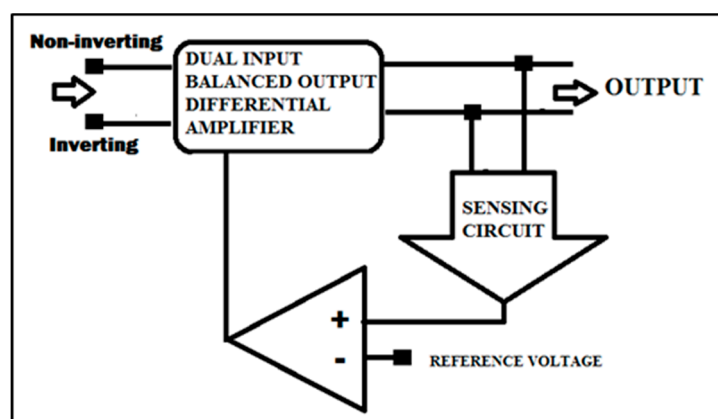


Figure 1. Block structure of current mode feedback op-amp.

Figure 2 shows the entire architecture of the modified op-amp comparator (GB-CMFD) with gain boosting and common mode current feedback [23–25]. Inputs are given to the dual input fully differential pair that comprises of M1 and M2 MOSFETS. The output of this differential pair is taken from the output node which incorporates folded cascode current mirrors as source and sink. M4, M5, M6, and M7 form a current source while, on the other hand, M8, M9, M10, and M11 forms a current sink [26]. The sensing circuit comprises Ms1 and Ms2, which sense the common mode signal from the output node. Next, this signal is compared with the reference voltage through a comparator circuit through M3 and M12.

Further, the correction signal is fed to the fully differential pair through M3 and, thus, it adjusts its operating current according to the correction signal and reduces the common mode gain. A gain booster block which includes MG1, MG2, MG3, and MG4 is also added along with this circuit. This block is responsible for the gain boosting.

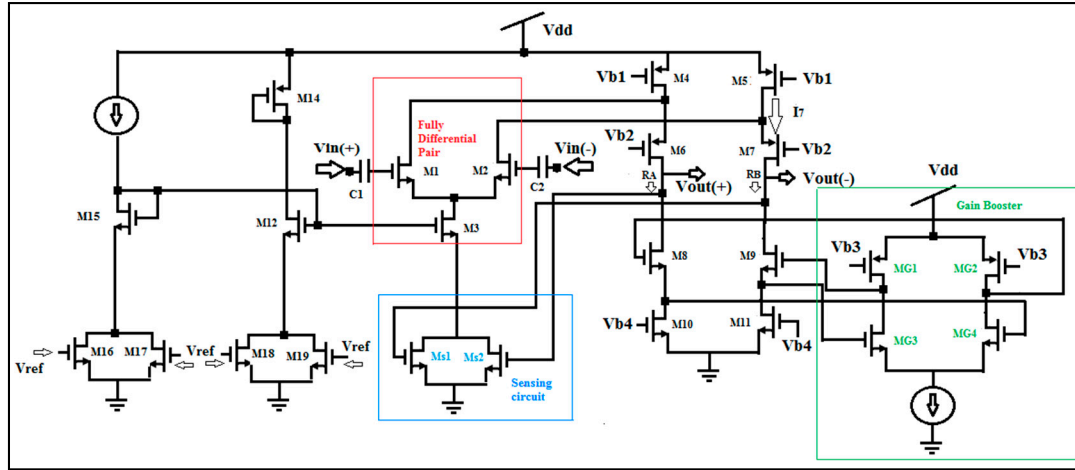


Figure 2. Modified GB-CMFD comparator circuit.

The difference signal taken from the differential pair M1 and M2 is amplified further by the next stage, which comprises of eight MOS devices. R_A and R_B are the output resistances at output nodes $v_{out}(+)$ and $v_{out}(-)$, respectively. These output resistances are responsible for the high output gain of the op-amp comparator circuit as the gain of any amplifier is estimated by the product of its transconductance and output resistance. M8, M9, M10, and M11 MOS devices are arranged and biased in such a manner as to provide high resistance to the output nodes.

In the final segment of the operational amplifier comparator, the gain booster block interacts with the M8 and M9 MOS devices. The output from the drain terminal of M8 and M9 NMOS devices is fed into the gate terminal of MG4 and MG3 MOSFET devices, respectively, which are working in a common source amplifier configuration. The MOS devices MG2 and MG1 are biased with a voltage v_{b3} and connected to the drain terminal of MG4 and MG3 devices to increase the resistance at the output terminal. Thus, the output of the op-amp comparator gets enhanced by the gain of the gain booster block and is again fed back to the gate terminal of M8 and M9 devices and, thus, the overall output gain of operational amplifier comparator gets boosted.

Major differences in this modified schematic with respect to the general CMFD topology [23–25] are the less complicated structure by utilizing fewer MOS devices, which ultimately reduces power consumption of this modified structure. For gain boosting this structure employs only one gain boosting block in the pull-down section. As there are fewer MOS devices in the pull-up section, it results in the fast charging of the output node, which eventually leads to a high slew rate.

Mathematical Analysis

Gain for the differential pair is given as:

$$\text{Gain} = \text{Effective } g_m \cdot \text{Effective } R_{out} \quad (1)$$

where, g_m is the effective trans-conductance and R_{out} is the effective output resistance [1,13]. Looking at the output node V_{out} the resistance R_B can be calculated as given in Equation (1):

$$R_B = \frac{(r_{ds7} + g_{m9} \cdot r_{ds9} \cdot r_{ds11})}{g_{m7} \cdot r_{ds7}}$$

$$R_B = \frac{(r_{o7} + g_{m9} \cdot r_{o9} \cdot r_{o11})}{g_{m7} r_{o7}} \quad (2)$$

Additionally, the current I_7 that flows through this output node can be calculated as:

$$I_7 = \left\{ \frac{g_{m2}(r_{o2} \parallel r_{o5})}{2 \left[\left(\frac{g_{m9} \cdot r_{o9} \cdot r_{o11}}{g_{m7} r_{o7}} \right) + (r_{o2} \parallel r_{o5}) \right]} \right\} \cdot V_{in}(-)$$

$$I_7 = \left\{ \frac{g_{m2} \cdot V_{in}(-)}{2 \left\{ 1 + \left[\left(\frac{g_{m9} \cdot r_{o9} \cdot r_{o11}}{g_{m7} r_{o7}} \right) \cdot (g_{ds2} + g_{ds5}) \right] \right\}} \right\} \quad (3)$$

From Equations (1) and (3) the output voltage gain comes out to be:

$$\frac{V_{out}}{V_{in}} = \left\{ \frac{g_{m1}}{2} + \left\{ \frac{g_{m2} \cdot V_{in}(-)}{2 \left\{ 1 + \left[\left(\frac{g_{m9} \cdot r_{o9} \cdot r_{o11}}{g_{m7} r_{o7}} \right) \cdot (g_{ds2} + g_{ds5}) \right] \right\}} \right\} \right\} \cdot R_{out} \quad (4)$$

where R_{out} is given as:

$$R_{out} = [g_{m9} \cdot r_{o9} \cdot r_{o11}] \parallel [g_{m7} r_{o7}(r_{o2} \parallel r_{o5})]$$

Rearranging and solving the Equation (4) by assuming trans-conductance and output resistance of all mirrors as g_m and r_o :

$$\frac{V_{out}}{V_{in}} = \left\{ \frac{g_{m1}^2 \cdot r_o^2}{4} \right\} \quad (5)$$

Now, solving for the gain boosting circuit, R_{out} can be calculated as:

$$R_{out} = [A \cdot g_{m9} \cdot r_{o9} \cdot r_{o11}] \parallel [g_{m7} r_{o7}(r_{o2} \parallel r_{o5})]$$

Again, solving for gain:

$$\frac{V_{out}}{V_{in}} = \left\{ \frac{A \cdot g_{m1}^2 \cdot r_o^2}{4} \right\} \quad (6)$$

Comparing Equations (5) and (6) it can be easily concluded that with the modified architecture the gain improves in comparison to the general common feedback structure [23–25].

3. Results

In this segment, all the required simulations, such as transient, AC analysis, along with parameter variations of the modified circuit using a closed loop configuration is demonstrated. Monte Carlo simulations have been performed by using SPICE in 90 nm CMOS technology. At least 20 iterations are performed by utilizing the Monte Carlo simulation methods for concluding the final results.

An op-amp with a feedback circuit is designed to have a gain of 20. The design schematic blocks of that are shown in Figure 3 [15,27].

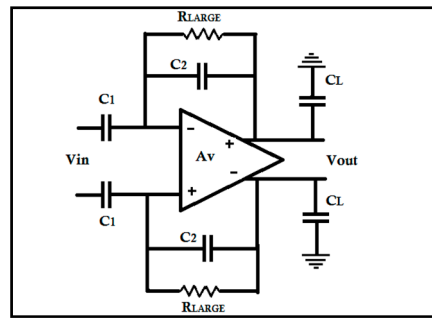


Figure 3. An operational amplifier with feedback.

Figure 4 represents the modified circuit of the op-amp comparator employing common mode current feedback with folded cascoded current mirrors along with gain-boosting circuit. The channel length of 90 nm and the channel width of 1 μm is used as the dimension of MOS devices in the proposed op-amp comparator modified architecture.

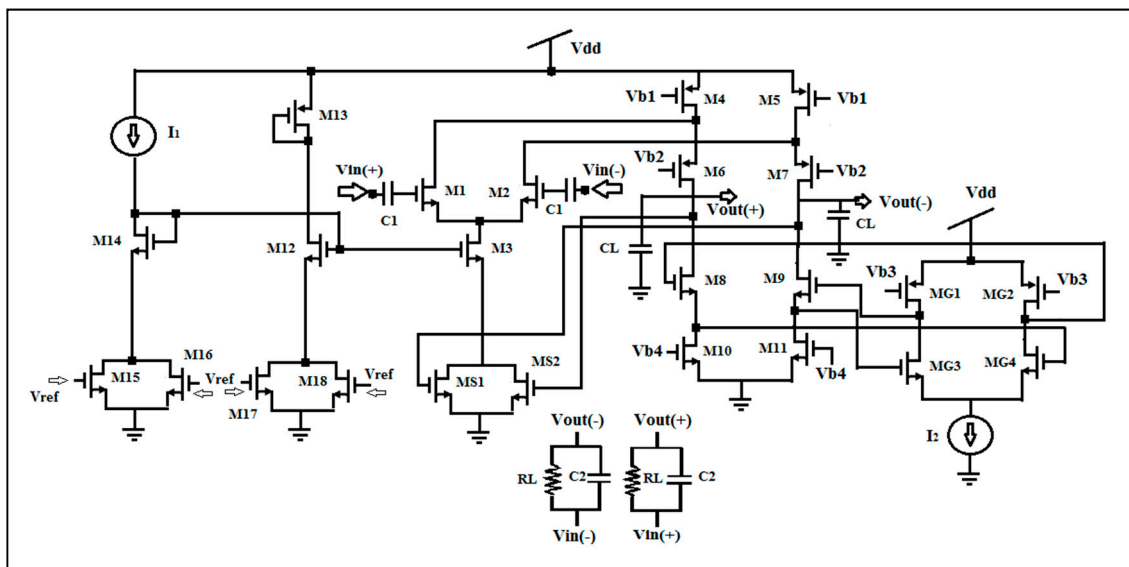


Figure 4. Comparator with modified gain boosting current feedback.

Table 1 shows the power consumption, maximum current drawn, and the rise time and fall time of the modified op-amp (GB-CMFD) comparator. Simulation is done on a supply voltage of 0.7 V at 25 $^{\circ}\text{C}$.

Table 1. Power consumption, current drawn, and rise and fall times of the modified GB-CMFD.

Supply Voltage = 0.7 V			Temp = 25 $^{\circ}\text{C}$	
Width (μm)	Power Consumption (μW)	Current Drawn (μA)	Rise Time (ps)	Fall Time (ps)
1.0	362	517	7	7
1.5	390	558	7	7
2.0	416	595	7	7
2.5	436	623	7	7
3.0	454	649	7	7
3.5	472	674	7	7
4.0	489	699	7	7
4.5	506	724	7	7
5.0	524	748	7	7

Variations in the parameters when the channel width is varied from 1 μm to 5 μm are also included in Table 1. This circuit draws a maximum current of 517 μA by consuming the power of 362 μW at 1 μm channel width. The values of power consumption and current drawn are increased by 44% when the channel width is increased to 5 μm . Figure 5a,b shows these variations graphically.

Table 1 also gives the details regarding the rising and falling duration for the output pulse and its variation with channel width. Rise and fall times of 7 ps are observed for both rising and falling edges. The variations in these values are negligible with the variation in channel width.

Figure 6 gives details regarding the output waveforms that are recorded with respect to the input waves for the modified structure (CMFD-GB). The input voltage at the negative terminal is kept constant at 350 millivolts and then a varying voltage is applied at the positive terminal. The output waveform at the non-inverting terminal, which is recorded, is shown in Figure 6

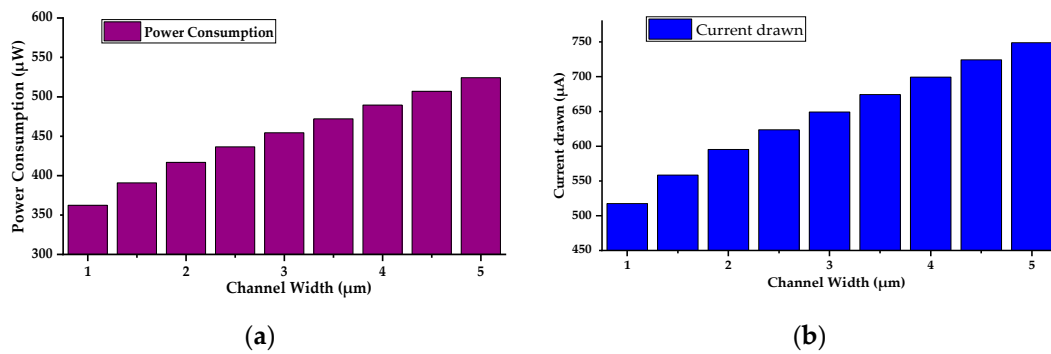


Figure 5. (a) Power consumption vs. channel width; and (b) current drawn vs. channel width.

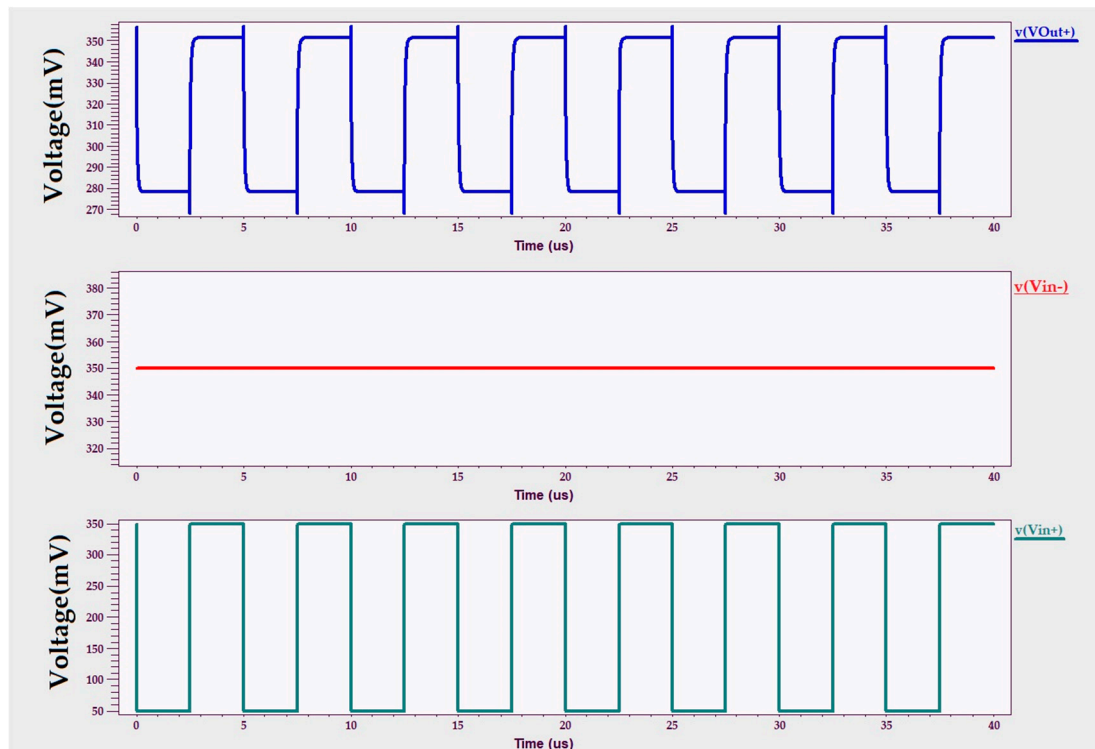


Figure 6. Output waveforms of CMFD-gain boosting comparator (transient analysis).

Table 2 shows power consumption, observed closed loop gain, open loop gain, gain error, and slew rate of the modified GB-CMFD comparator. Simulation is done at a supply voltage of 0.7 V by varying the temperature from $-5\text{ }^{\circ}\text{C}$ to $55\text{ }^{\circ}\text{C}$.

Table 2. Power consumption, gain error, slew rate, and closed and open loop gain of the modified GB-CMFD at different temperatures.

Temp (°C)	Power Consumption (μ W)	Observed Closed Loop Gain (dB)	Open Loop Gain	Gain Error %	Slew Rate (Rise Time) (V/ μ s)	Slew Rate (Fall Time) (V/ μ s)
−5	365	13	953	0.69	839	839
0	364	13	953	0.69	839	839
5	364	13	953	0.69	839	839
15	363	13	1075	0.61	839	839
25	362	13	1075	0.61	839	839
35	361	13	1229	0.53	839	839
45	361	13	1229	0.53	839	839
55	362	13	1229	0.53	839	839

In Table 2 the variations in the power consumption are detailed. The modified circuit consumes 362 μ W at 25 °C. This value increases marginally but remains close to 362 μ W when the temperature is raised to 55 °C. On the other hand, when the temperature was reduced to −5 °C the power consumption increased further and attained the value of 365 μ W at −5 °C. Figure 7a shows the variations of power consumption with temperature.

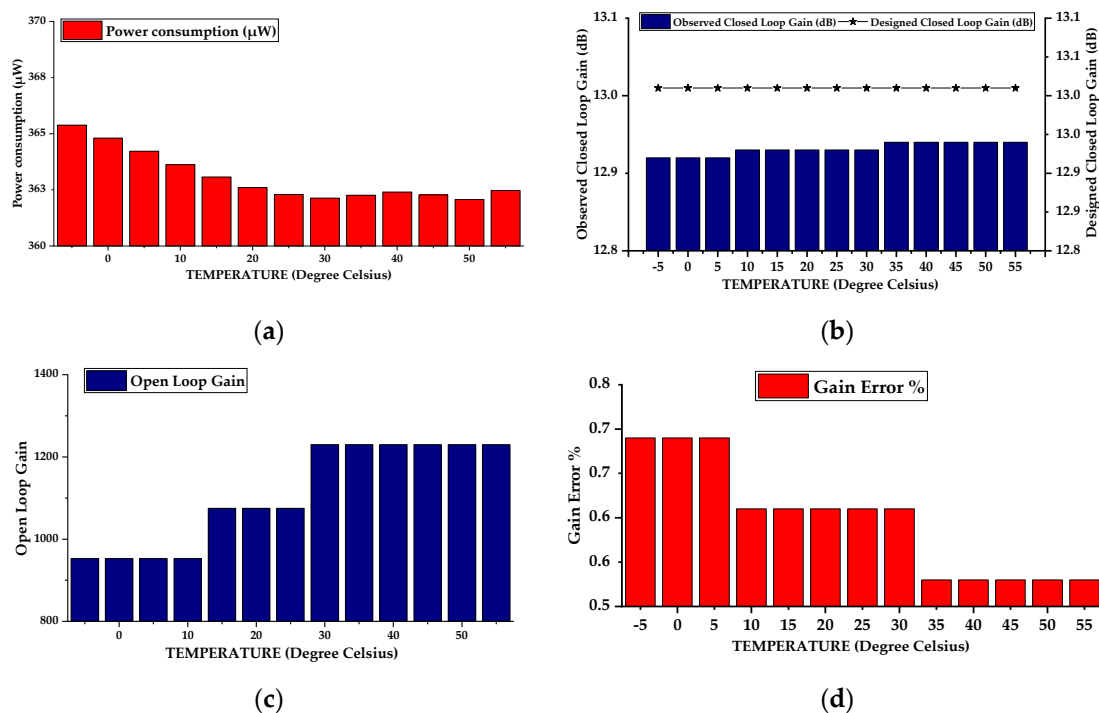
**Figure 7.** (a) Power consumption vs. temperature; (b) observed closed loop gain vs. temperature; (c) open loop gain vs. temperature; and (d) gain error vs. temperature.

Figure 7b,c exhibit the observed closed loop gain and open loop gain variations with temperature. An observed closed loop gain of 12.93 decibels at 25 °C is recorded, which is very close to the designed closed loop gain of 13.01 decibels. Diminutive level variations are recorded when the temperature varied from −5 to 55 °C. Open loop gain is then detailed with its variations with temperature. The open loop gain of 1075 is observed for the GB-CMFD structure at 25 °C, which is quite large as compared to standard comparator structures. The open loop gain of 1075 is recorded for the modified architecture at 25 °C, which increases to 1229 when the temperature is raised to 55 °C. However, the open loop gain reduced to 953 when the temperature is reduced to −5 °C. Overall, the percentage variations of the open loop gain are 11% to 14% with the variations in temperature.

The gain error variations with temperature are shown in Table 2. Though the circuit is designed in a closed loop configuration for the power gain of 20, which equals 13.01 dB, the values that are obtained from the magnitude plot are marginally different at different temperatures. The gain error is almost constant for the temperature range of -5 to 25 °C and has an error of 0.1% from the expected value, which is relatively acceptable. Figure 7d shows the variations of gain error with temperature.

Figure 8 represents the frequency response of the closed loop CMFD-GB structure. The variations in the closed loop gain with respect to temperature can be easily observed from this response.

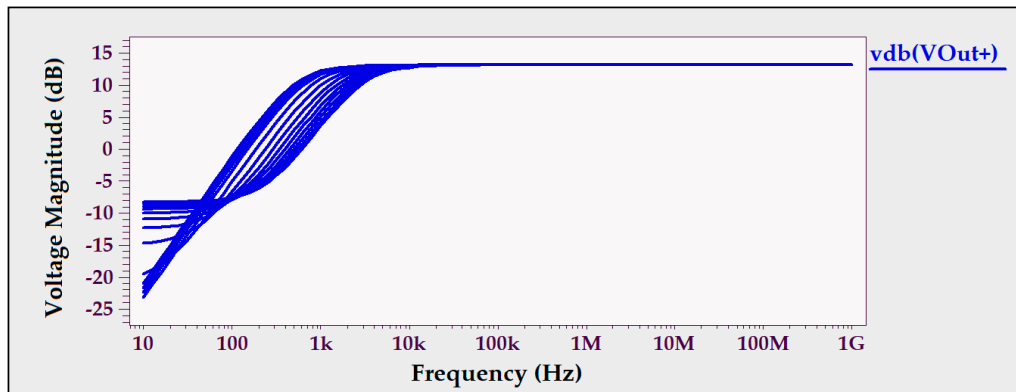


Figure 8. Variations in closed loop gain with temperature (AC analysis).

In the end Table 2 gives the details regarding the slew rate of the modified gain boosting CMFD comparator and its variations with temperature. Slew rate is the measure of the rate at which the output voltage rises with respect to time [28]. Thus, if a comparator has a high slew rate, it will lead to the high speed of comparison [29].

$$SLEW\ RATE = \frac{VOLTAGE\ LEVEL\ (V)}{RISE\ TIME\ (\mu s)\ or\ FALL\ TIME\ (\mu s)}$$

Thus, from the above relation, if a circuit has a very small value of rising time and fall time then it will eventually have a very high slew rate.

From Table 1 the rise time and fall time for this modified GB-CMFD circuit are seven picoseconds and the maximum minus minimum voltage range that is observed after the simulation is 0.006 V for both the rising and falling edge. Thus, using these values, a slew rate of $839\ V/\mu s$ is obtained for the circuit, which is quite a high value as compared to the other comparators. Figure 9a,b shows the variations of the slew rate for charging and discharging edge with temperature.

It can be seen that this variation is very minute and, thus, this circuit has a high slew rate which is almost stable with temperature variations.

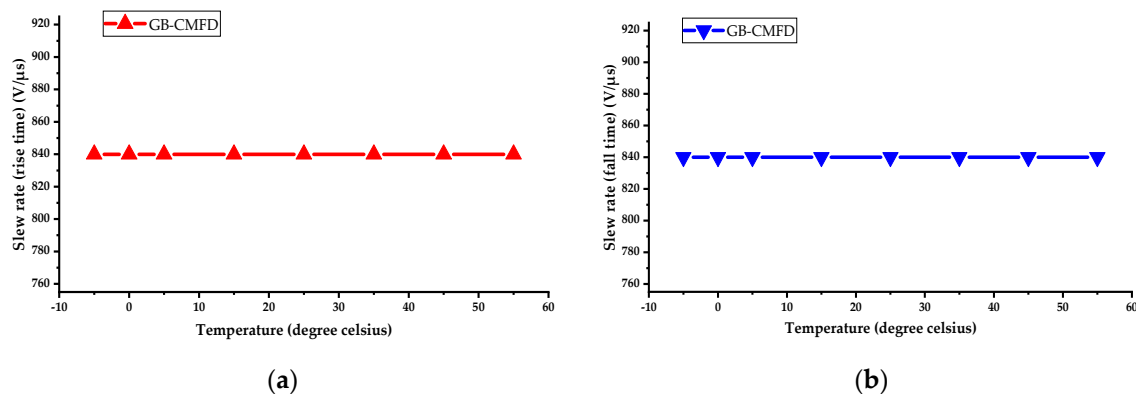


Figure 9. (a) Slew rate (rising edge) vs. temperature; and (b) slew rate (falling edge) vs. temperature.

Table 3 summarizes the performance of the modified gain boosting CMFD comparator. CMOS technology is used to design this circuit with the channel length of 90 nm and channel width of 1 μm . A supply voltage of 0.7 V is deployed for the simulations. Twenty-four MOS transistors are used for designing the circuit, along with four capacitors and two resistors. The value of power consumption at 25 $^{\circ}\text{C}$ is 362 μW while drawing a current of 517 μA , both having a variation of approximately 2%. A total of 12.93 decibels of closed loop gain is observed at 25 $^{\circ}\text{C}$, which is quite close to the calculated gain of 13.01 decibels.

The open loop gain of 1075 is attained by this structure at 25 $^{\circ}\text{C}$, which is large, compared to normal comparator structures. A gain error of 0.6% is obtained after simulation of this circuit at 25 $^{\circ}\text{C}$, which is relatively acceptable. A very high slew rate is achieved by this modified design that is 839 V/ μs that will eventually lead to a very high speed of comparison and, thus, this comparator can be utilized in designing high-speed analog circuits, such as ADCs and DACs [30–32].

Table 3. Comparison of results at 25 $^{\circ}\text{C}$.

Temperature	25 $^{\circ}\text{C}$
Technology	CMOS
No. Of Mosfets	24
Channel Length	90 nm
Channel Width	1 μm
Supply voltage	0.7 V
Power consumption	362 μW
Current drawn	517 μA
Observed closed loop gain	13 decibels
Gain error %	0.6
Open loop gain	1075
Slew rate	839 V/ μs

Table 4 summarizes the percentage variation of these parameters with temperature. Power consumption varies substantially with the decrease in temperature. A total of 0.07% of marginal variations are recorded for observed closed loop gain, which almost equals zero and is acceptable. Open loop gain variations are then shown in the table, which varies from 12% at -5°C and 14% at 55 $^{\circ}\text{C}$. Significant variations in the gain error are recorded when the temperature scales down to -5°C on the other hand, when the temperature increased to 55 $^{\circ}\text{C}$ the variations are minimal. Almost null variations are observed for the slew rate.

Table 4. Percentage variation with temperature.

Temperature	-5°C to $+55^{\circ}\text{C}$
Power consumption	$\cong 0\%$
Observed closed loop gain	$\cong 0\%$
Open loop gain	12% to 14%
Gain error	12% to 0.07%
Slew rate	$\cong 0\%$

4. Comparison

To evaluate the proposed modified architecture of the op-amp comparator (GB-CMFD) three more structures of the op-amp comparator are utilized for analyses and comparison. These three structures are DCFIA, SCFIA [19], and CMFD [23,24]. The structural design of these three architectures are depicted in Appendix A (Figures A1–A3). DCFIA and SCFIA are the amplifiers which employ common mode current feedback from drain and source terminals [10]. CMFD is a common mode current feedback with conventional cascode amplifier [23,24].

These three structures are again simulated in 90 nm CMOS technology. Results that are obtained after Monte Carlo simulation are shown in Table 5.

Table 5. Comparison of simulations results at 25 °C.

	DCFIA [19]	SCFIA [19]	CMFD [23,24]	GB-CMFD (Proposed Modified Architecture)
Technology	CMOS	CMOS	CMOS	CMOS
No. Of Mosfets	19	21	20	24
Channel Length	90 nm	90 nm	90 nm	90 nm
Channel Width	1 μm	1 μm	1 μm	1 μm
Supply voltage	0.8 V	0.8 V	1.8 V	0.7 V
Power consumption	10 μW	119 μW	1179 μW	362 μW
Observed closed loop gain(dB)	13.2	13.5	13.1	13
Gain error %	1	3	0.8	0.6
Open loop gain	467	177	801	1075
Slew rate	1 V/ μs	1 V/ μs	307 V/ μs	839 V/ μs

Figure 10 shows the variations in the power consumptions for all four comparators structures when the temperature is varied from -5 to $+55$ °C. The proposed modified architecture, despite using 24 MOS transistors, consumes power at a moderate level, which is approximately in the range of 360 μW . It also shows marginal variations with temperature variations.

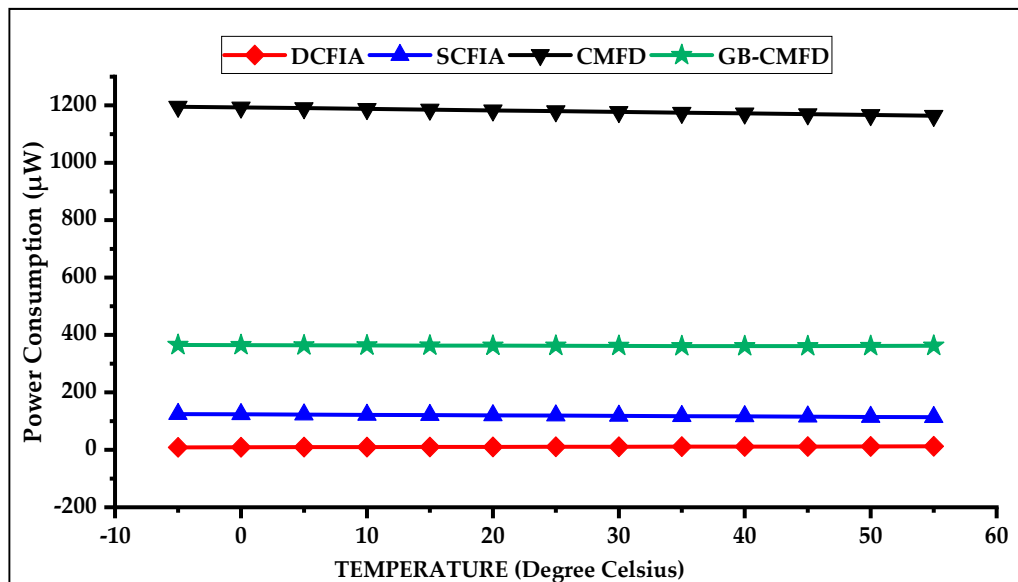
**Figure 10.** Power consumption vs. temperature.

Figure 11 shows the comparison of the gain error value for all four structures. It can be observed from the curves that GB-CMFD has the least value of the percentage gain error. Maximum variations in the gain error is shown by DCFIA and CMFD structures which increased substantially when temperature varies from -5 to $+55$ °C. SCFIA show the least variation with temperature but has more gain error value than GB-CMFD.

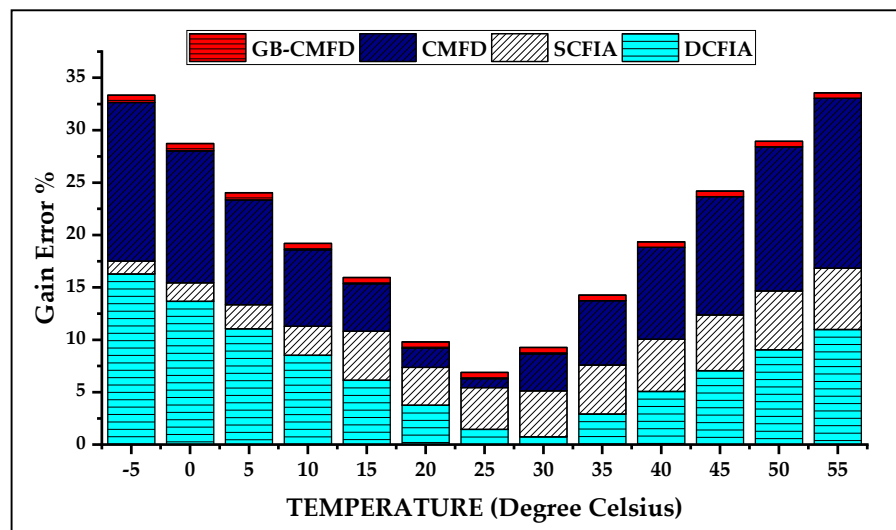


Figure 11. Gain error (%) vs. temperature.

Figure 12 illustrates the variations of observed closed loop gain for all four comparator structures. All four structures are employed in the circuit shown in Figure 3, which is designed for a closed loop gain of 13.01 decibel. The values of actual closed-loop gain that are observed at different temperatures in the simulations are then plotted in Figure 12. The magnitude of the observed closed loop gain for GB-CMFD is almost constant and very close to the designed closed loop value. The magnitude of observed closed loop gain for DCFIA decreases with the increase in temperature opposite to that of the observed CMFD closed loop gain value, which increases with the increase in temperature. The observed SCFIA closed loop gain values are small as compared to DCFIA and CMFD, but substantially large as compared to GB-CMFD.

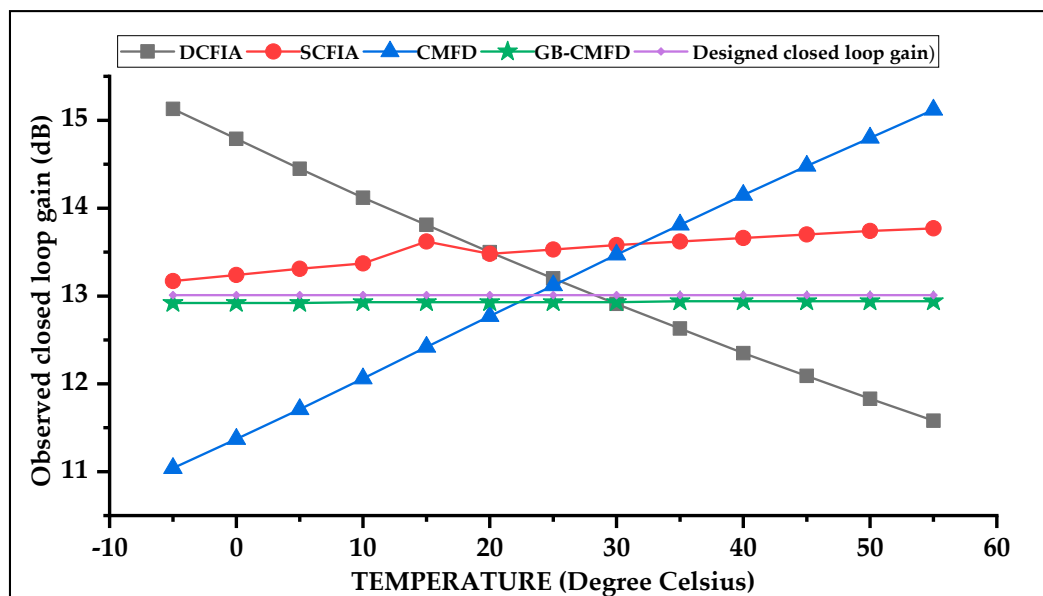


Figure 12. Observed closed loop gain vs. temperature.

Figure 13 depicts the variations in open loop gain with temperature. The GB-CMFD structure again shows the maximum magnitude of the open loop gain at different temperatures in comparison to other structures.

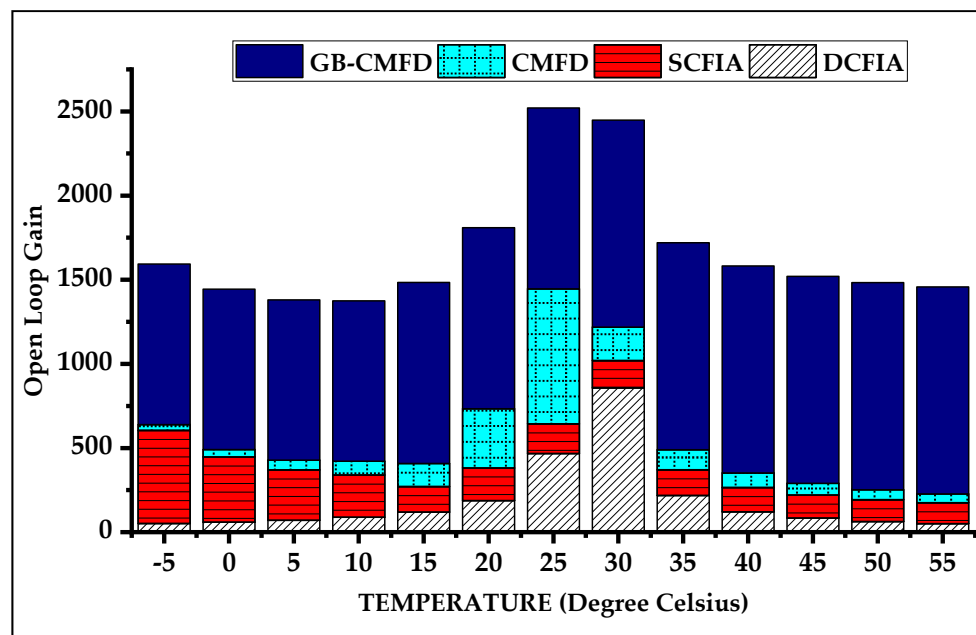


Figure 13. Open loop gain vs. temperature.

Table 6 summarizes these parametric variations of all four structures at different temperatures. The modified op-amp comparator (GB-CMFD) shows the least variation in comparison to others in all six parameters which are taken into consideration for comparison.

Table 6. Percentage variations in parameters when the temperature changes from -5 to 55 °C.

Parameters	DCFIA [19]	SCFIA [19]	CMFD [23,24]	GB-CMFD (Proposed Modified Architecture)
Power consumption	23 to 16	4 to 5	$\cong 3$	$\cong 0$
Observed closed loop gain	15 to 12	3 to 2	16 to 15	$\cong 0$
Open loop gain	88 to 89	212 to 30	96 to 94	11 to 14
Gain error	16 to 11	1 to 6	15 to 16	12 to 0.07
Slew rate (charging)	$\cong 0$	$\cong 0$	1 to 6	$\cong 0$
Slew rate (discharging)	$\cong 1$	$\cong 1$	29 to 27	$\cong 0$

Table 7 gives details regarding the comparison on the basis of power consumption of this comparator with other pertinent associated studies.

Table 7. Comparison with other associated studies.

	Technology CMOS	Supply Voltage	Slew Rate	Channel Length	Power Consumption
[29]	350 nm	2.5 V	161 V/ μ s	350 nm	456 μ W
[32]	350 nm	2.5 V	176 V/ μ s	350 nm	195 μ W
[33]	130 nm	1.0 V	—	130 nm	100 μ W
[34]	180 nm	1.1 V	—	180 nm	1300 μ W
[35]	180 nm	—	—	180 nm	$\cong 750$ μ W
[36]	65 nm	1.2 V	—	65 nm	2800 μ W
[37]	65 nm	1.2 V	—	65 nm	370 μ W
[37]	180 nm	0.7 V to 1.1 V	—	180 nm	420 μ W
GB-CMFD (Proposed-architecture)	90 nm	0.7 V	839 V/ μ s	90 nm	362 μ W

5. Conclusions

A modified architecture of an op-amp comparator to achieve a high slew rate and boosted gain with an improvement in gain design error is proposed and investigated in this manuscript. Deploying the gain booster block and common-mode current feedback structure, the modified architecture of the op-amp comparator (CMFD-GB) achieves an improvement in the overall gain and slew rate with the reduction in gain error and power consumption. An overall gain of 1075 is attained by implementing an additional gain booster block at the end segment of the op-amp comparator that is approximately a 34% improvement as compared to the general common-mode current feedback structure. The rise and fall time also get reduced due to this boosted gain which, in turn, leads to the very high slew rate for this modified op-amp comparator structure. A slew rate of $839 \text{ V}/\mu\text{s}$ is observed for this modified op-amp comparator structure, which is quite high and which makes this comparator a prominent contender for high-speed data converters circuits. Closed loop analysis of the modified op-amp comparator structure is done by utilizing this structure for designing a closed feedback amplifier with a gain of 13.01 dB. Results from the simulations depict that the observed and design gain is almost equal for the CMFD-GB comparator with the value of 12.93 decibels. Comparing it to the general CMFD structure, this is an approximately 27% reduction. Considerable reduction in power consumption is also attained through this modified op-amp comparator structure. In spite of using more MOS devices, the power consumption observed for this modified architecture is $362.29 \mu\text{W}$, which almost equals a 70% reduction as compared to general CMFD structure. The modified architecture of the op-amp comparator along with high slew rate also shows symmetry for charging and discharging output edges which makes it perfect for the designing of accurate and linear data converter circuits. Temperature sensitivity of these parameters is also observed for the modified comparator architecture by simulating this circuit at different temperatures. The results show an optimum variation of these critical parameters with varying temperature for the modified op-amp comparator architecture (CMFD-GB) as compared to three other architectures. Boosted gain and a large slew rate with optimum power consumption of this modified op-amp comparator structure (CMFD-GB) increases its applicability in high-speed analog and digital circuits, which are designed in ultra deep submicron technologies where high-speed and low-power consumption are the essential design constraints.

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Abbreviations

GB	Gain boosting
CM	Common mode
CMFD	Common mode feedback
PC	Power consumption
DCFIA	Drain current feedback instrumentation amplifier
SCFIA	Source current feedback instrumentation amplifier

Appendix A

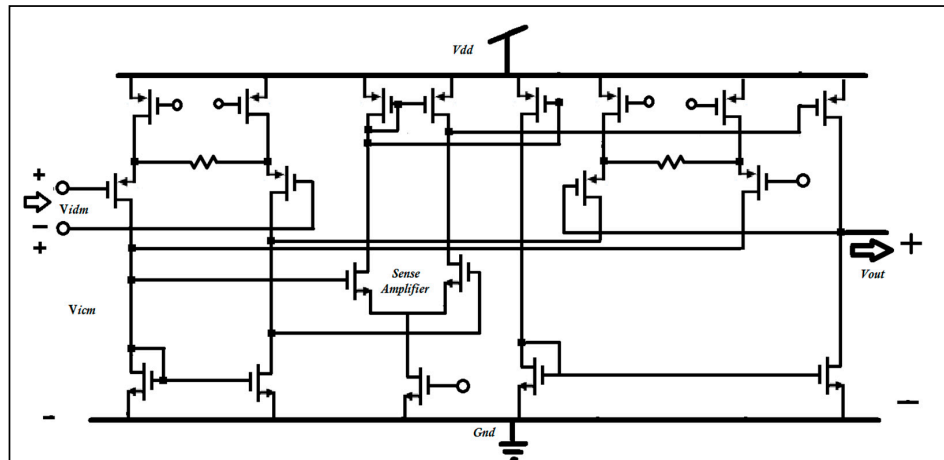


Figure A1. Drain current feedback instrumentation amplifier (DCFIA) schematic.

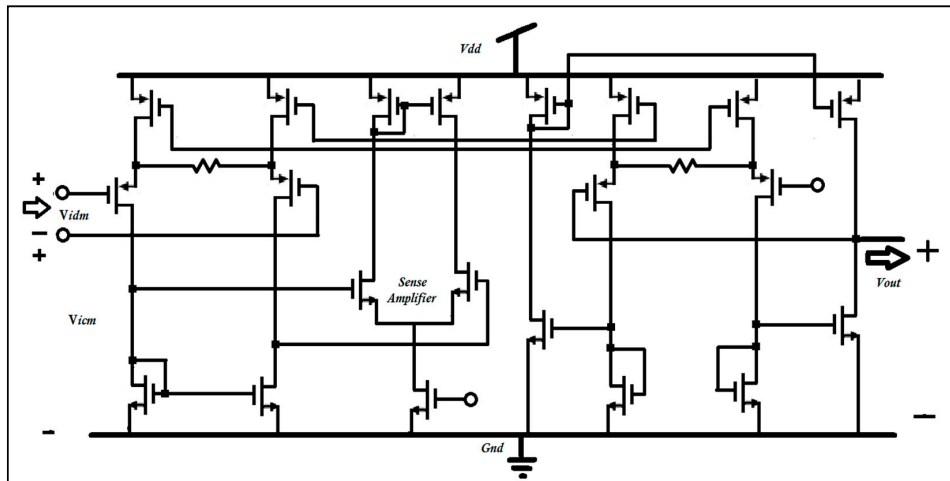


Figure A2. Source current feedback instrumentation amplifier (SCFIA) schematic.

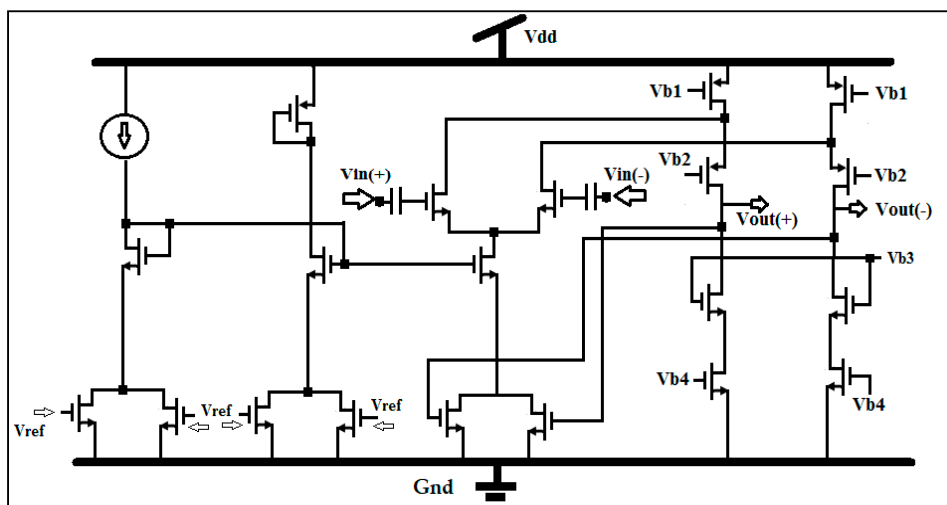


Figure A3. Common mode current feedback schematic.

References

1. Jendernalik, W. An Ultra-Low-Energy Analog Comparator for A/D Converters in CMOS Image Sensors. *Circuits Syst. Signal Process.* **2017**, *36*, 4829–4843. [[CrossRef](#)]
2. Ay, S.U. Energy Efficient Supply Boosted Comparator Design. *J. Low Power Electron. Appl.* **2011**, *1*, 247–260. [[CrossRef](#)]
3. Savani, V.; Devashrayee, N.M. Design and Analysis of Low-Power High-Speed Shared Charge Reset Technique Based Dynamic Latch Comparator. *Microelectron. J.* **2018**, *74*, 116–126. [[CrossRef](#)]
4. Xin, X.; Cai, J.; Xie, R.; Wang, P. Ultra-Low Power Comparator with Dynamic Offset Cancellation for SAR ADC. *Electron. Lett.* **2017**, *53*, 1572–1574. [[CrossRef](#)]
5. Bindra, H.S.; Lokin, C.E.; Schinkel, D.; Annema, A.J.; Nauta, B. A 1.2-V Dynamic Bias Latch-Type Comparator in 65-Nm CMOS With 0.4-MV Input Noise. *IEEE J. Solid-State Circuits* **2018**, *53*, 1902–1912. [[CrossRef](#)]
6. Richelli, A.; Colalongo, L.; Kovacs-Vajna, Z.; Calvetti, G.; Ferrari, D.; Finanzini, M.; Pinetti, S.; Prevosti, E.; Savoldelli, J.; Scarlassara, S. A Survey of Low Voltage and Low Power Amplifier Topologies. *J. Low Power Electron. Appl.* **2018**, *8*, 1–20. [[CrossRef](#)]
7. Savani, V.; Devashrayee, N.M. Analysis and Design of Low-Voltage Low-Power High-Speed Double Tail Current Dynamic Latch Comparator. *Analog Integr. Circuits Signal Process.* **2017**, *93*, 287–298. [[CrossRef](#)]
8. Khatak, A.; Dhull, S.; Taleja, M.K. A Study on Advanced High Speed and Ultra Low Power ADC Architectures. *Indian J. Sci. Technol.* **2017**. [[CrossRef](#)]
9. Taghizadeh, A.; Koozehkanani, Z.D.; Sobhi, J. A New High-Speed Low-Power and Low-Offset Dynamic Comparator with a Current-Mode Offset Compensation Technique. *AEU—Int. J. Electron. Commun.* **2017**, *81*, 163–170. [[CrossRef](#)]
10. Bano, S.; Narejo, G.B.; Ali Shah, S.M.U. Power Efficient Fully Differential Bulk Driven OTA for Portable Biomedical Application. *Electronics* **2018**, *7*, 41. [[CrossRef](#)]
11. Khatak, A.; Kumar, M.; Dhull, S. Analysis of CMOS Comparator in 90nm Technology with Different Power Reduction Techniques. *Int. J. Electr. Comput. Eng.* **2018**, *8*. [[CrossRef](#)]
12. Zahrai, S.A.; Onabajo, M. Review of Analog-To-Digital Conversion Characteristics and Design Considerations for the Creation of Power-Efficient Hybrid Data Converters. *J. Low Power Electron. Appl.* **2018**, *8*, 12. [[CrossRef](#)]
13. Dubey, A.K.; Nagaria, R.K. Optimization for Offset and Kickback-Noise in Novel CMOS Double-Tail Dynamic Comparator: A Low-Power, High-Speed Design Approach Using Bulk-Driven Load. *Microelectron. J.* **2018**, *78*, 1–10. [[CrossRef](#)]
14. Khorami, A.; Sharifkhani, M. A Low-Power High-Speed Comparator for Precise Applications. *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.* **2018**, 1–12. [[CrossRef](#)]
15. Kumaravel, S.; Venkataramani, B. An Improved Recycling Folded Cascode OTA with Positive Feedback. *WSEAS Trans. Circuits Syst.* **2014**, *13*, 85–93.
16. Ragheb, A.N.; Kim, H.W. Ultra-Low Power OTA Based on Bias Recycling and Subthreshold Operation with Phase Margin Enhancement. *Microelectron. J.* **2017**, *60*, 94–101. [[CrossRef](#)]
17. Maloberti, F.; Pea-Perez, A.; Gonzalez-Diaz, V.R. Opamp Gain Compensation Technique for Continuous-Time $\Sigma\Delta$ Modulators. *Electron. Lett.* **2014**, *50*, 355–356.
18. Khorami, A.; Sharifkhani, M. Excess Power Elimination in High-Resolution Dynamic Comparators. *Microelectron. J.* **2017**, *64*, 45–52. [[CrossRef](#)]
19. Worapishet, A.; Demosthenous, A. Generalized Analysis of Random Common-Mode Rejection Performance of CMOS Current Feedback Instrumentation Amplifiers. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2015**, *62*, 2137–2146. [[CrossRef](#)]
20. Lee, J.Y.; Hwang, S.N. A High-Gain Boost Converter Using Voltage-Stacking Cell. *Trans. Korean Inst. Electr. Eng.* **2008**, *57*, 982–984.
21. Ng, K.A.; Xu, Y.P. A Low-Power, High CMRR Neural Amplifier System Employing CMOS Inverter-Based OTAs With CMFB Through Supply Rails. *IEEE J. Solid-State Circuits* **2016**, *51*, 724–737.
22. Mahdavi, S.; Noruzpur, F.; Ghadimi, E.; Khanshan, T.M. A New Fast Rail-to-Rail Continuous-Time Common-Mode Feedback Circuit. In Proceedings of the 2017 MIXDES—24th International Conference Mixed Design of Integrated Circuits and Systems, Bydgoszcz, Poland, 22–24 June 2017; pp. 387–391.

23. Haga, Y.; Zare-Hoseini, H.; Berkovi, L.; Kale, I. Design of a 0.8 Volt Fully Differential CMOS OTA Using the Bulk-Driven Technique. In Proceedings of the 2005 IEEE International Symposium on Circuits and Systems, Kobe, Japan, 23–26 May 2005; pp. 220–223.
24. Duque-Carrillo, J.F. Control of the Common-Mode Component in CMOS Continuous-Time Fully Differential Signal Processing. *Analog Integr. Circuits Signal Process.* **1993**, *4*, 131–140. [[CrossRef](#)]
25. Bult, K.; Geelen, G.J.G.M. The CMOS Gain-Boosting Technique. *Analog Integr. Circuits Signal Process.* **1991**, *1*, 119–135. [[CrossRef](#)]
26. Hassanpourghadi, M.; Zamani, M.; Sharifkhani, M. A Low-Power Low-Offset Dynamic Comparator for Analog to Digital Converters. *Microelectron. J.* **2014**, *45*, 256–262. [[CrossRef](#)]
27. Zhao, X.; Zhang, Q.; Wang, Y.; Deng, M. Transconductance and Slew Rate Improvement Technique for Current Recycling Folded Cascode Amplifier. *AEU—Int. J. Electron. Commun.* **2016**, *70*, 326–330. [[CrossRef](#)]
28. Aggarwal, B.; Gupta, M.; Gupta, A.K. A Comparative Study of Various Current Mirror Configurations: Topologies and Characteristics. *Microelectron. J.* **2016**, *53*, 134–155. [[CrossRef](#)]
29. Danesh, S.; Hurwitz, J.; Findlater, K.; Renshaw, D.; Henderson, R. A Reconfigurable 1 GSps to 250 MSps, 7-Bit to 9-Bit Highly Time-Interleaved Counter ADC with Low Power Comparator Design. *IEEE J. Solid-State Circuits* **2013**, *48*, 733–748. [[CrossRef](#)]
30. Miki, T.; Morie, T.; Matsukawa, K.; Bando, Y.; Okumoto, T.; Obata, K.; Sakiyama, S.; Dosho, S. A 4.2 MW 50 MS/s 13 Bit CMOS SAR ADC With SNR and SFDR Enhancement Techniques. *IEEE J. Solid-State Circuits* **2015**, *50*, 1372–1381. [[CrossRef](#)]
31. Maji, K.B.; Kar, R.; Mandal, D.; Ghoshal, S.P. An Evolutionary Approach Based Design Automation of Low Power CMOS Two-Stage Comparator and Folded Cascode OTA. *AEU—Int. J. Electron. Commun.* **2016**, *70*, 398–408. [[CrossRef](#)]
32. Gupta, R.; Gupta, R.; Sharma, S. Design of High Speed and Low Power 4-Bit Comparator Using FGMOS. *AEU—Int. J. Electron. Commun.* **2017**, *76*, 125–131. [[CrossRef](#)]
33. Khorami, A.; Sharifkhani, M. High-Speed Low-Power Comparator for Analog to Digital Converters. *AEU—Int. J. Electron. Commun.* **2016**, *70*, 886–894. [[CrossRef](#)]
34. De La Fuente-Cortes, G.; Espinosa Flores-Verdad, G.; Gonzalez-Diaz, V.R.; Diaz-Mendez, A. A New CMOS Comparator Robust to Process and Temperature Variations for SAR ADC Converters. *Analog Integr. Circuits Signal Process.* **2017**, *90*, 301–308. [[CrossRef](#)]
35. Goll, B.; Zimmermann, H. A Comparator with Reduced Delay Time in 65-Nm CMOS for Supply Voltages down to 0.65 V. *IEEE Trans. Circuits Syst. II Express Briefs* **2009**, *56*, 810–814. [[CrossRef](#)]
36. Chua, C.; Kumar, R.B.N.; Sireesha, B. Design and Analysis of Low-Power and Area Efficient N-Bit Parallel Binary Comparator. *Analog Integr. Circuits Signal Process.* **2017**, *92*, 225–231. [[CrossRef](#)]
37. Rahmani, S.; Ghaznavi-Ghouschi, M.B. Design and Analysis of a High Speed Double-Tail Comparator with Isomorphic Latch-Preamplifier Pairs and Tail Bootstrapping. *Analog Integr. Circuits Signal Process.* **2017**, *93*, 507–521. [[CrossRef](#)]

