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An 8–12.5-GHz LC PLL with Dual VCO and Noise-Reduced LDO Regulator for Multilane Multiprotocol SerDes in 28-nm CMOS Technology

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Abstract: This study presents an inductance capacitance (LC) phase-locked loop (PLL) with a dual voltage-controlled oscillator (VCO) and a noise-reduced low-dropout (LDO) regulator, which was used in four-lane multiprotocol serial link applications. The dual VCO architecture can increase the total frequency-tuning range to ensure that the LC PLL achieves multiprotocol serial link coverage from 8 to 12.5 Gbps. Two switch capacitor array-based LC VCOs have a large frequency-tuning range and small VCO gain. The noise-reduced LDO regulator provides a very low-noise power supply to the VCO. The active area occupied by the proposed LC PLL in UMC 28-nm 1P10M complementary metal–oxide–semiconductor (CMOS) technology is 0.25 mm^2. The phase noise of the VCO at 1 MHz is −108.1 dBc/Hz. The power consumption of the LC PLL with a 1.8-V supply is 16.5 mW.

Keywords: Multiprotocol SERDES; LC PLL; noise-reduced LDO regulator; dual VCO

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1. Introduction

A clock synthesizer is a fundamental module in an integrated Serializer/Deserializer (SerDes) system, and the phase-locked loop (PLL) is the most widely used clock synthesizer on a chip. With the ever-increasing data rate and diverse communication protocols, the demand for faster SerDes systems has considerably increased in recent years. Recent studies show that the data rate of the SerDes system is beyond 60 Gbps [1,2]. Although faster links beyond 60 Gbps are beginning to replace the 10–25-Gbps ports, 10–25 Gbps is still the mainstream data rate in the industry. Because of the increase in the data rate of the SerDes system, the PLL design has encountered more challenges, such as a high-frequency design and a wide frequency-tuning range with a low-jitter design [3–7]. Ring PLL and LC PLL are the two most widely used integrated on-chip PLLs. As Cameron et al. have shown [5], ring PLL is an appropriate choice for low-frequency applications because it can easily realize a wide frequency-tuning range and occupies a small active area. However, it is difficult for a ring voltage-controlled oscillator (VCO) to generate a high-frequency clock; an LC PLL can generate a high-frequency clock with good noise performance but has a narrow frequency-tuning range and occupies a large active area [8]. To increase the frequency-tuning range of the LC VCO, a capacitor array and two LC VCOs [9,10] are used in the present study.

In this study, we propose an inductance capacitance (LC) PLL with two VCOs and a noise-reduced low-dropout (LDO) regulator in a four-channel SerDes system. The LC VCO uses a five-bit capacitor array to increase the frequency-tuning range and decrease the VCO gain. The output noise level from the LC VCO should be small in case the PLL obtains a smaller jitter spec. The noise-reduced LDO regulator will provide very low-noise output as a power supply to the VCO to reduce the VCO noise resulting from coupling with the power supply.

An increasing number of applications require a low-noise LDO to suppress the output voltage ripple and noise [11,12]. The traditional LDO structure has some limitations in low-noise design. Sometimes it is necessary to design a low-noise error amplifier and bandgap [13–15] or to add a filter network to the bandgap and LDO output signal [16–18]. In this study, we designed an LDO structure with a diode array and a control algorithm feedback circuit. The diode has lower noise than traditional complementary metal–oxide–semiconductor (CMOS) devices; hence, the LDO noise can be reduced to a very small level. Another advantage of this study is that the area and power consumption of the proposed LDO can be more easily reduced compared with a traditional LDO because it has a simple analog part and a complex digital part. This study did not need to design a high-performance analog circuit, such as a low-noise bandgap and low-noise error amplifier. The digital circuit can easily reduce the area and power consumption when the CMOS logic process progresses.

The remainder of this paper is structured as follows. Section 2 describes the LC PLL design, including the LC VCO structure and noise-reduced LDO regulator structure with noise analysis. Post-simulation and measurement results are presented in Section 3 and are followed by a conclusion in Section 4.

2. LC PLL Design

2.1. LC PLL Structure

The SerDes transmitter (TX) structures are shown in Figure 1. They include a first-in first-out (FIFO) memory, which is used to synchronize different input data. The encoder can encode the data into the SerDes standard. The serializer can convert data of the parallel format into data of the serial format. The equalizer is used to improve the high-frequency component in the serial data to compensate the high-frequency energy loss in the transmission channel. The driver can improve the driving ability of serial data. The serializer needs a high-frequency and low-jitter clock input, which is usually provided by a PLL. The receiver can change the input differential clock signal Ref CLK+ and Ref CLK− into a single-ended clock signal reference clock (CKREF) and provide this CKREF to the PLL as an input reference clock signal.

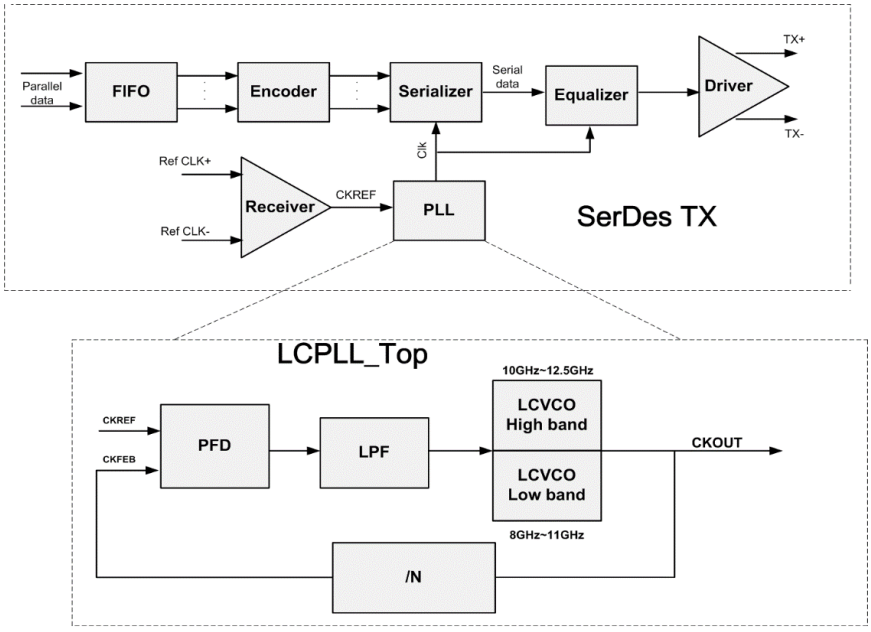

Figure 1. Block diagram of the Serdes transmitter (TX) and the inductance capacitance (LC) phase-locked loop (PLL) structure. FIFO: first-in first-out; PFD: phase and frequency detector; LPF: low pass filter.

The LC PLL structure is also shown in Figure 1. It includes a phase and frequency detector (PFD), which is used to detect the phase and frequency difference between the CKREF and feedback clock (CKFEB) signals. The PFD output is mostly a narrow pulse signal. The low pass filter (LPF) can convert the PFD output signal into a smooth analog voltage; the LC VCO output frequency is controlled by the LPF output voltage. For example, if the frequency of CKREF is higher than that of CKFEB, the LPF output voltage level and the LC VCO output frequency rise until the frequency of CKFEB is close enough to that of CKREF. When the PLL enters the steady state, the frequency of CKOUT is equal to N*CKREF; therefore, PLL is also used as a frequency multiplier to generate a high-frequency and low-jitter clock signal. The tuning range of the LC VCO is smaller than that of other VCO structures. Therefore, in this study, we designed two LC VCOs covering the range of 8–12.5 GHz and the input CKREF that covers 100 MHz, which can meet most clock applications.

The main module of the LC PLL shown in Figure 1 is the LC VCO, which is also the main source of noise in the LC PLL. The noise of the LC VCO can be divided into two parts: one is the device noise of the LC VCO itself and the other is the coupling noise from the power source. Thus, the noise reduction of the LC VCO often focuses on two parts: reducing the device noise and the power coupling noise. This study mainly focuses on reducing the power coupling noise. The proposed design uses LDO as a power supply to the LC VCO, which can effectively reduce the power coupling noise. However, the device noise of LDO itself is simultaneously introduced into the VCO output frequency. To meet the noise requirements of the LC PLL and LC VCO, the proposed design also adopts an LDO structure that can effectively reduce the LDO device noise.

2.2. LC VCO Structure and Noise Analysis

For a PLL system, the phase noise of the VCO is the key factor determining the clock jitter of the entire PLL. Figure 2 shows the LC VCO circuit structure and passive inductance layout designed by the metal layer. The LC VCO mainly comprises an on-chip inductance L, a voltage-controlled capacitance array Cv and C_0–C_n, and an LDO. The layout should be highly symmetrical to reduce the parasitic effect. Both the voltage-controlled capacitance and on-chip inductance are not the main sources of noise. The voltage-controlled capacitance array determines the tuning range of the LC VCO output frequency. The LDO isolates most of the noise from the 1.8-V power supply VDD and provides a 1.1-V low-noise power supply to the VCO. This reduces the phase noise of the VCO output frequency. In the circuit, as shown in Figure 2, we only use two cross-coupled N-metal-oxide-semiconductors (NMOSs), M1 and M2, to provide current to the LC oscillator, rather than the current source circuit, because the LDO not only suppresses the power noise but also limits the total current provided to the LC oscillator to achieve stable oscillation. Such an LC VCO design simplifies the active devices in the circuit and can also achieve better phase noise.

The phase noise of the LC VCO is the most important parameter for measuring VCO performance. There are several models and theories for analyzing phase noise, among which the Leeson model formula is widely used [19,20]:

$$L\{\Delta\omega\} = 10\log\left\{\frac{2FkT}{P_{sig}}\left[1+\left(\frac{\omega_0}{2Q\Delta\omega}\right)^2\right]\left(1+\frac{\Delta\omega_{1/f^3}}{|\Delta\omega|}\right)\right\} \quad (1)$$

where ω_0 is the VCO oscillation frequency, $\Delta\omega$ is the frequency offset, P_{sig} is the signal power, k is the Boltzmann constant, T is the temperature in Kelvin, and F is the noise factor, which is an empirical parameter usually obtained through an experimental fitting. $\Delta\omega_{1/f^3}$ is the turn-around frequency of $1/(\Delta\omega)^2$ and $1/|\Delta\omega|^3$, and in this Leeson model, it is equal to the $1/f$ inflection point of the device noise. Q is the quality factor of the LC oscillator. Sometimes, measurement data did not match this Leeson formula very well, because Leeson formula is a fitting formula, but it also can give some important guidance

to low noise VCO design. As shown in Formula (1), increasing the signal power P_{sig} and the Q value, as well as decreasing the boundary frequency $\Delta\omega_{1/f^3}$ and noise factor F, can effectively reduce the VCO output frequency phase noise. The mechanism of noise factor F is very complex, mainly due to the variable capacitance and differential pair.

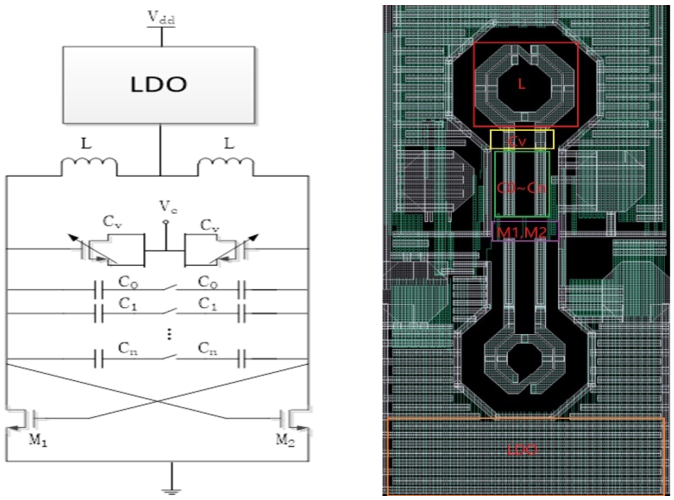

Figure 2. LC voltage-controlled oscillator (VCO) structure and passive inductance layout. LDO: low dropout regulator.

In the proposed design, the LDO is used to isolate power supply noise; thus, the total noise output by the LC VCO includes the noise of the LDO and LC VCO devices. Because there is no correlation between the LC VCO and LDO device noises, the total phase noise of the LC VCO can be expressed as Formula (2):

$$L_{(TOTAL)} = \sqrt{L_{(VCO)}{}^2 + L_{(LDO)}{}^2}, \quad (2)$$

where $L_{(TOTAL)}$ is the total output phase noise of the LC VCO at a frequency offset f_m and $L_{(VCO)}$ is the device noise of the LC VCO itself at a frequency offset f_m; $L_{(LDO)}$ is the LDO output noise at a frequency offset f_m. In this study, we measured the VCO phase noise at f_m = 1 MHz. When we consider the influence of the VCO power supply on the VCO output frequency phase noise because the VCO power supply is provided by the LDO output voltage in this design, the LDO output noise can equivalently be expressed as Formula (3) [21]:

$$L_{(LDO)} = 20\log_{10}\left(\frac{P \times S_{f_m}}{\sqrt{2} \times f_m}\right), \quad (3)$$

where f_m is the offset frequency (Hz) corresponding to the measurement of noise spectral density, S_{f_m} is the noise spectral density ($V/\sqrt{Hz}$) of the LDO output, and P is the voltage push coefficient (MHz/V) of the VCO, which is used to represent the disturbance caused by the power supply voltage fluctuation to the VCO output signal frequency.

The LDO output voltage in this design is 1.1 V. Accordingly, we use an ideal power supply for the LC VCO and set the supply voltage to 1.1 ± 0.05 V; under this condition, the simulated voltage push coefficient P of the LC VCO is approximately 490 MHz/V, implying that when the supply voltage changes to 0.05 V, the LC VCO output frequency changes by approximately (490 MHz/V) × 0.05 V = 24.5 MHz. The LC VCO phase noise $L_{(VCO)}$ simulation result is −108.7 dBc/Hz at 1MHz with the ideal power supply at 1.1 V. The SerDes system requires that the LC VCO total phase noise $L_{(TOTAL)}$ SPEC be less than −105 dBc/Hz at 1MHz. According to formulas (2) and (3), at f_m = 1 MHz, the calculation result of LDO noise spectral density S_{f_m} should be less than 12 $nV/\sqrt{Hz}$ to meet the $L_{(TOTAL)}$ SPEC. The noise characteristics of a traditional LDO and this design LDO are analyzed below.

2.3. Noise-Reduced LDO Design

The main noise in a traditional LC PLL comes from the LC VCO. In SerDes applications, to avoid the interference of the TX, Receiver (RX), and other digital modules, an LDO is placed on the LC VCO to isolate the noise interference from the power supply. However, the LDO also brings its noise, which is modulated by the VCO circuit to the VCO output frequency and becomes VCO phase noise. Thus, reducing LDO noise has become a key point of low-noise LC VCO design.

The traditional LDO structure is shown in Figure 3. According to the circuit principle, the output voltage V_{OUT} of the traditional LDO can be calculated as follows:

$$V_{OUT} = V_{REF}\left(1 + \frac{R_1}{R_2}\right). \tag{4}$$

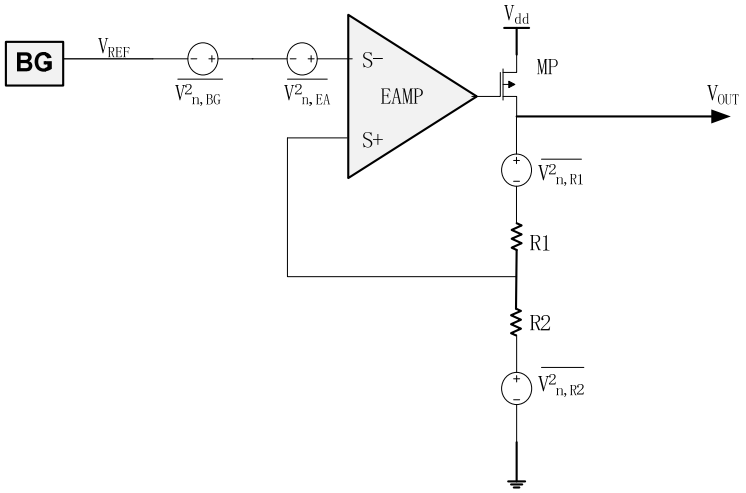

Figure 3. Conventional low-dropout (LDO) regulator structure. BG: bandgap reference.

The output noise of the traditional LDO comprises three parts: the output noise of bandgap reference (BG) $\overline{V_{n,\,BG}^2}$, equivalent input noise of the error amplifier (EAMP) $\overline{V_{n,\,EA}^2}$, and thermal noise of the resistance feedback network $\overline{V_{n,\,R1}^2}$ and $\overline{V_{n,\,R2}^2}$. These noises are uncorrelated and can be accumulated. Thus, the equivalent output noise of the traditional LDO (with a frequency range of f_1 –f_2) is [22]:

$$\overline{V_{n,\,OUT}^2} = \int_{f_1}^{f_2} [\left(\overline{V_{n,\,BG}^2} + \overline{V_{n,\,EA}^2}\right)\left(1 + \frac{R_1}{R_2}\right)^2 + \overline{V_{n,\,R1}^2} + \overline{V_{n,\,R2}^2}\left(\frac{R_1}{R_2}\right)^2]df. \tag{5}$$

According to the above calculation, the noise performance requirement of the SerDes system in this LDO design is less than 12 nV/$\sqrt{\text{Hz}}$ at 1 MHz. But the simulation result of the output noise performance of the traditional LDO structure is 13.2 nV/$\sqrt{\text{Hz}}$ at 1 MHz, which cannot meet the requirements of less than 12 nV/$\sqrt{\text{Hz}}$ at 1 MHz. However, it is difficult to reduce the noise caused by BG and EAMP, which usually requires an RC filter with a low inflection point to remove the device noise, but this will result in an extremely large area.

In the design of an LDO, digital feedback control and programmable technology are often introduced to optimize the performance of the LDO. Huang and Liao [23] used programmable feedback resistance to considerably expand the output voltage range of the LDO. Yuan et al. [24] used a digital feedback control technology to reduce the ripple and dropout voltage of LDO output. The LDO in the present study used the digital control algorithm finite state machine (FSM) to reduce LDO device noise.

The LDO structure in this study is shown in Figure 4. Compared with the traditional structure, it comprises a current source array I1–In, a diode array D1–Dn, a comparator (Comp), a BG that is not in the loop, and an FSM.

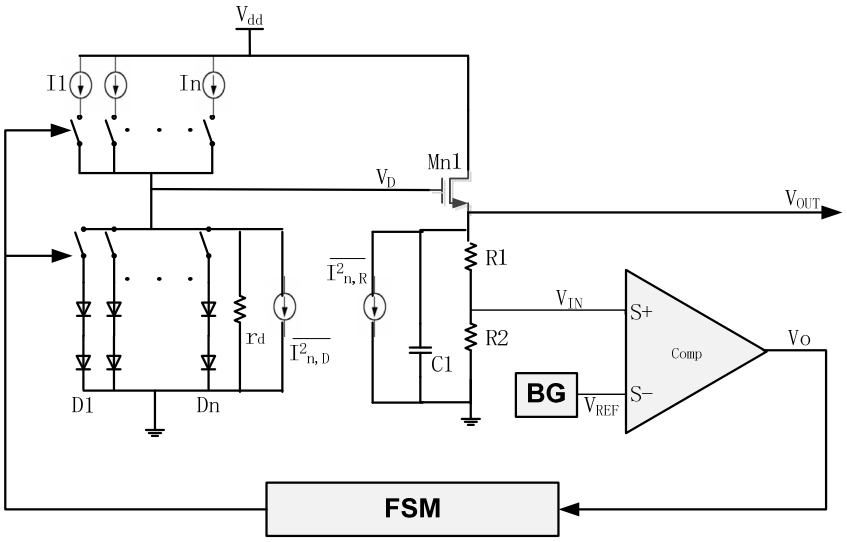

Figure 4. Structure of the noise-reduced LDO regulator. FSM: finite state machine.

Current source I1–In generates controllable current according to different switch control signals, which is input into the diode array D1–Dn, and a voltage V_D is generated at the gate of Mn1, which is a source follower. The voltage drops from V_D to V_{OUT}. Then, $V_{IN} = (V_{OUT} \times R2)/(R1 + R2)$ is compared with V_{REF}, which is generated by a BG, and the comparison result Vo is input into the control algorithm FSM. If Vo is 1, it indicates that the output voltage (V_{OUT}) is greater than the expected voltage (VREF) $\times$ (R1 + R2)/R2 and the output of the control algorithm FSM reduces the current source array, thus reducing V_{OUT}. If Vo is 0, it indicates that V_{OUT} is less than the expected voltage VREF $\times$ (R1+R2)/R2, and the output of the control algorithm FSM increases the current source array, thus increasing V_{OUT}. The output of the control algorithm FSM can control both the current source array and the diode array, and the principle of controlling the current source array and the diode array is similar. Moreover, it is possible to control both the current source and diode array simultaneously, with one array as rough tuning and the other as fine tuning; the tuning precision determines the voltage precision of the final LDO output. When the mean value of Vo in a continuous time is close to 0.5, the loop is considered to have entered a stable state. At this point, the loop is cut off and the output value of the FSM and V_{OUT} is fixed. In this way, BG noise will not enter the loop after the control algorithm loop is disconnected, thus eliminating the influence of BG noise on LDO output V_{OUT}. In addition, because of the diode being a device that is below the gate surface, the diode noise is smaller than that of the conventional CMOS device; thus, the noise generated by the analog circuit in the entire loop is smaller than that of the bandgap voltage source BG and EAMP in the conventional architecture.

The output noise of the noise-reduced LDO regulator in this design can be expressed as follows:

$$\overline{V_{n,\,OUT}^2} = \overline{V_{n,\,D}^2} + R^2\overline{I_{n,\,R}^2}, \tag{6}$$

$$\overline{V_{n,\,D}^2} = r_d{}^2\overline{I_{n,\,D}^2} = 2r_d{}^2qI_Df_m. \tag{7}$$

When the algorithm control loop is disconnected, R = R1 + R2, r_d is the equivalent dynamic resistance of the diode array and I_D is the static current of the diode array. Compared with the traditional structure LDO, the noise from BG and EAMP is suppressed and the diode itself has low noise; therefore, the noise performance improves significantly.

The simulation results of the noise-reduced LDO regulator output of this design are also shown in Figure 5. The noise is 3.06 nV/$\sqrt{\text{Hz}}$ at 1 MHz, which fully meets the requirement of 12 nV/$\sqrt{\text{Hz}}$ at 1 MHz.

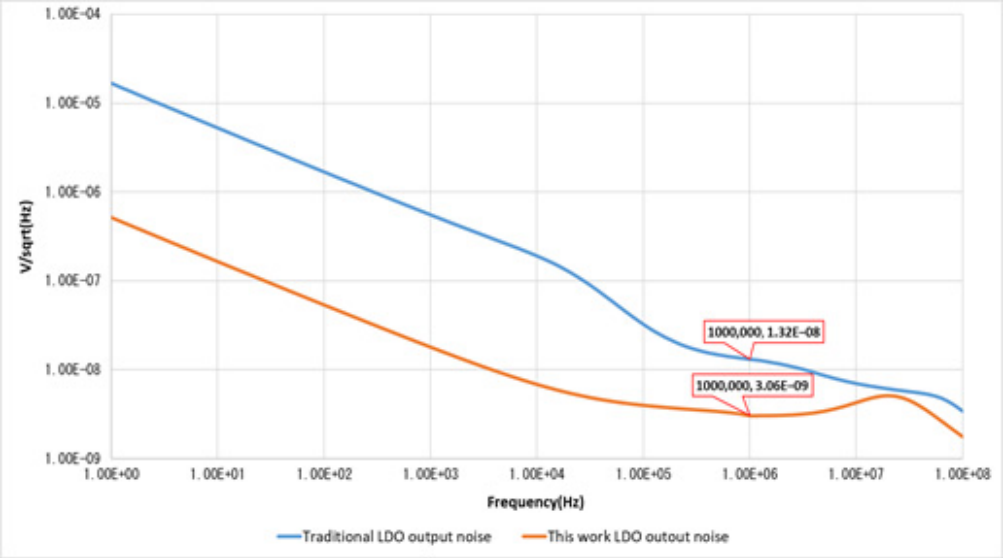

Figure 5. Comparison of output noise simulation results of the conventional LDO and the proposed LDO.

In this study, we used Cadence (Cadence Systems, Inc., San Jose, CA, USA) Spectre as the circuit simulation tool; the AC noise analysis function in the Cadence Spectre tool was chosen to evaluate the LDO output noise spectral density. This design is based on the UMC 28-nm 1P10M CMOS technology; the device noise parameters are included in the model file of the UMC 28-nm 1P10M CMOS technology, which loads in the Cadence Spectre tool during the simulation.

3. Post-Simulation and Measurement Results

3.1. Low-Noise LC PLL Layout

Figure 6 shows the four-channel SerDes system layout using the LC PLL of the proposed design. The red rectangular region is the LC PLL. The blue rectangular region is the power management (PM) circuit. The four purple rectangular regions are the four channels of the SerDes TX and RX. The LC PLL is based on the UMC 28-nm 1P10M CMOS technology, and the LC PLL area is 0.25 mm^2.

3.2. VCO Noise

Figure 7 shows the post-simulation result of the total output phase noise of the LC VCO designed in this study. It should be noted that to correspond to the test circuit, during the simulation, the output frequency of the VCO should be 3.125 GHz after passing through a divide-by-four circuit (the frequency is reduced four times). The phase noise simulation result includes the influence of the VCO's device and LDO output noises.

The post-simulation result in Figure 7 shows that when the LC VCO output frequency is divided by 12.5–3.125 GHz, the phase noise is −120.46 dBc/Hz at a frequency offset f_m = 1 MHz. The simulation tool is also a Cadence Spectre; the PSS and P noise function in the Spectre tool were chosen for the oscillation signal analysis.

Figure 8 shows the LC VCO output phase noise test results in the open-loop condition. The LC VCO output frequency is passed through the divide-by-four test circuit, and the noise spectrum of LC VCO is free run at 3.18 GHz, measured using E5052B, which is a signal source phase noise analyzer manufactured by Agilent (Agilent Technologies Inc., Santa Clara, CA, USA).

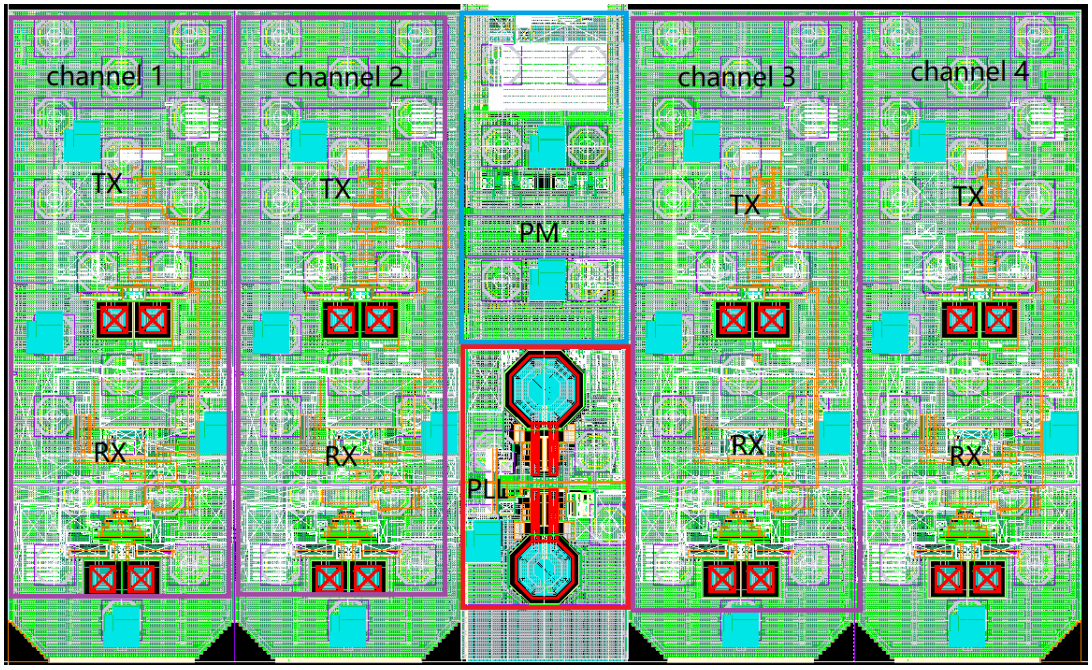

Figure 6. Layout of SerDes and PLL. RX: Receiver; PM: power management.

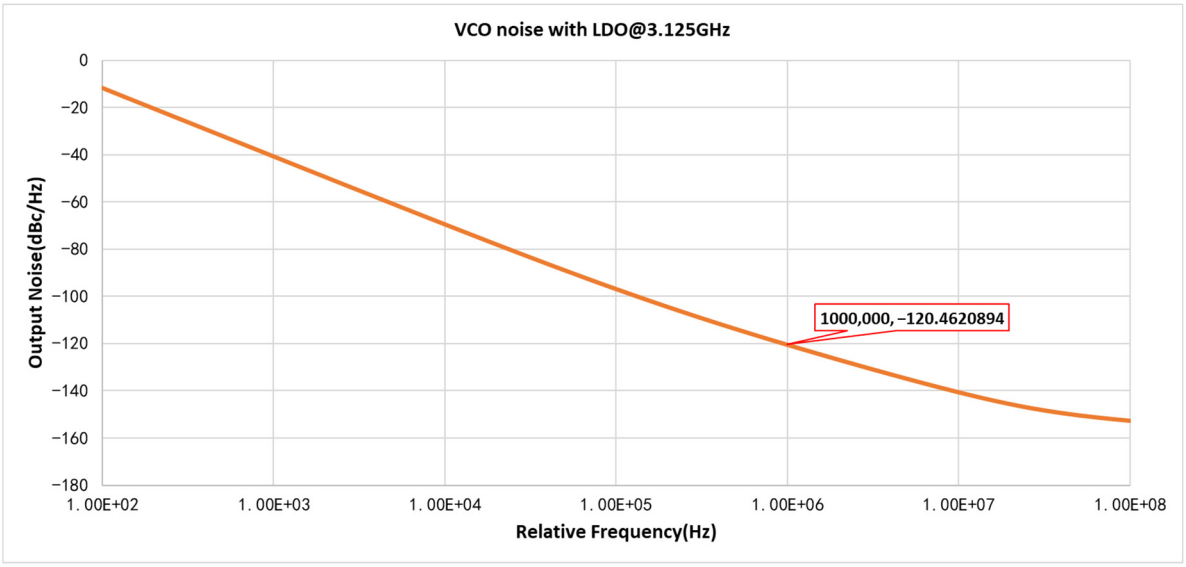

Figure 7. LC VCO output phase noise post-simulation results.

The post-simulation and test results in Figures 7 and 8 are very close, −120.46 and −120.08 dBc/Hz, respectively, at a 1-MHz frequency offset. Because the output frequency of the VCO at this time is reduced by four times after a divide-by-four circuit, it can be calculated according to the fact that the phase noise around 12.5 GHz will worsen by approximately 12 dBc/Hz compared with the above results around 3.125 GHz. In particular, when the output frequency is 12.5 GHz and the frequency offset is 1 MHz, the phase noise is approximately −108.46 and −108.08 dBc/Hz, respectively. This test result meets the requirement that the phase noise of LC VCO output should be less than −105 dBc/Hz at 1 MHz when the output frequency is 12.5 GHz. The abovementioned test and post-simulation conditions are obtained with a 1.8 V power supply at 27 °C, with a TT device. TT means that the process corner is a typical NMOS device and a typical P-channel metal oxide semiconductor (PMOS) device.

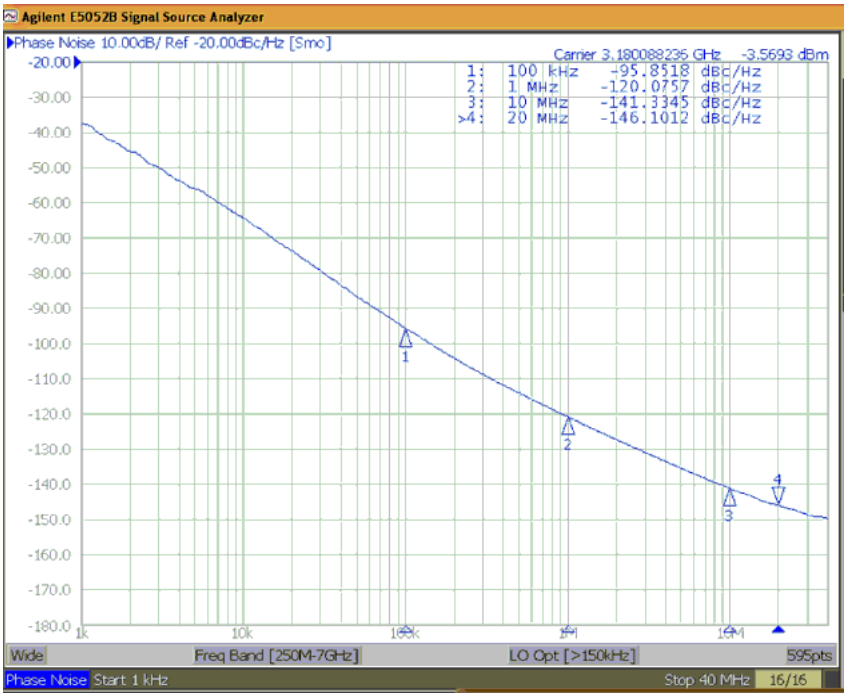

Figure 8. Test results of VCO output.

3.3. LC PLL Noise

The LC PLL and LC VCO test system block diagram is shown in Figure 9, and the noise spectrum test results of the LC PLL output at 12.5 GHz are shown in Figure 10.

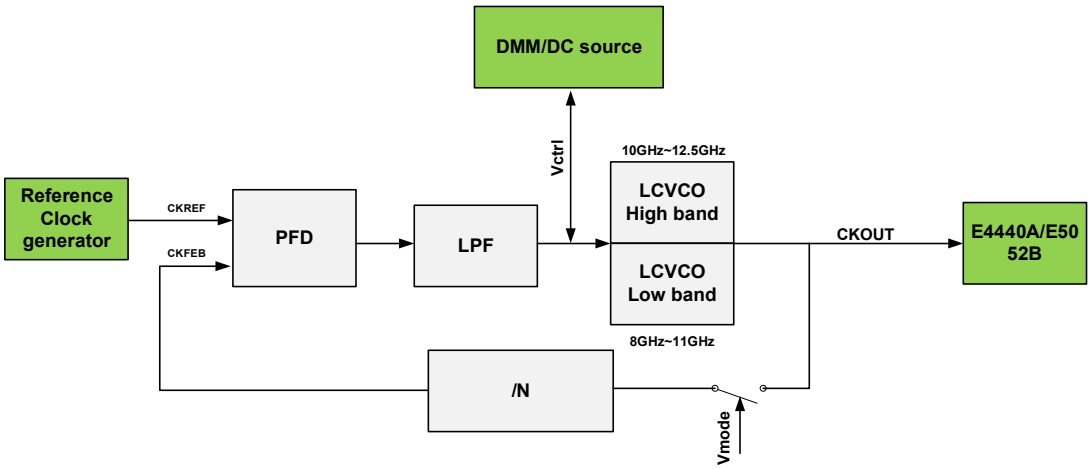

Figure 9. Block diagram of the LC PLL and LC VCO test system.

The PLL test system shown in Figure 9 can test both the LC VCO and LC PLL output noise performance. To test the LC PLL, V_{mode} was set to make the loop close and a Digital Multimeter (DMM) was used to monitor the Vctrl voltage from the LPF output. If Vctrl becomes stable, it means the LC PLL has also entered a stable state; in that case, E4440A is used to test the LC PLL output frequency jitter. E4440A is a spectrum analyzer manufactured by Agilent Technologies Inc. To test the LC VCO, V_{mode} was set to make the loop open, and a DC source was used to supply an external Vctrl to the LC VCO. Then, the E5052B was used to test the LC VCO output frequency phase noise.

When the PLL output is 12.5 GHz, the period is 80 ps and the maximum random jitter tolerance is approximately 8 ps, which should satisfy the seven-sigma standard; thus, the

maximum jitter spec for PLL is 8 ps/14 = 0.571 ps. Test results show that the PLL jitter in this study is 0.535 ps.

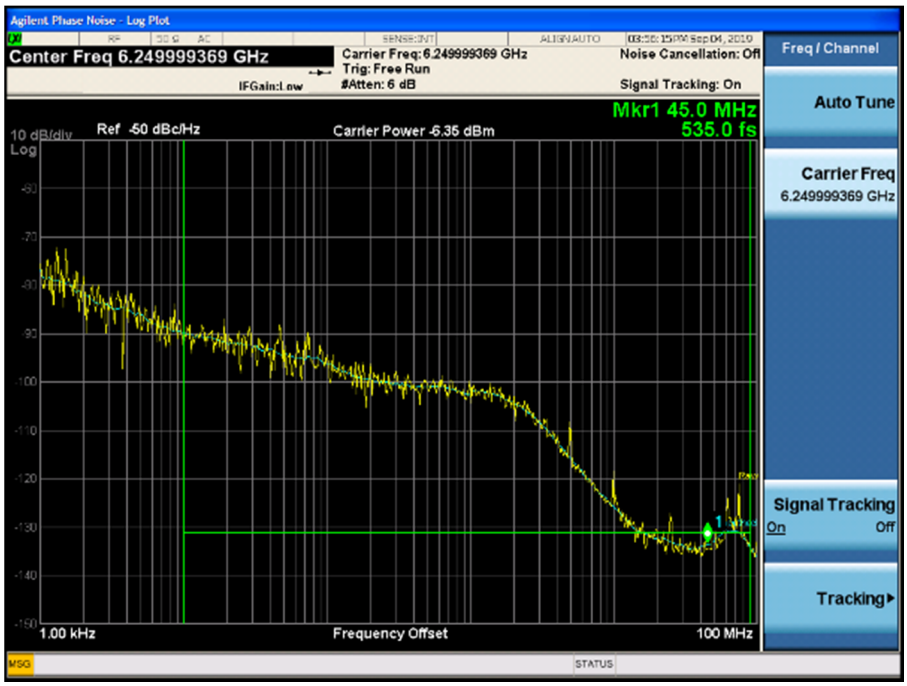

Figure 10. LC PLL output noise test results.

In this design, the noise jitter spec of the LC PLL is 0.571 ps (integral range of 1 KHz–20 MHz), and the test result shown in Figure 10 is 0.535 ps (integral range of 1 KHz–90 MHz). The test result meets the spec requirements.

3.4. Calculation of the LC VCO Figure of Merit (FOM) Value

The designed LC VCO works at 1.1 V with an average operating current of 3 mA and power consumption of 3.3 mW. The calculation formula of FOM [25] value is as follows:

$$\mathrm{FOM} = -\mathrm{L}(\Delta f) + 20\log\left(\frac{f_0}{\Delta f}\right) - 10\log(P), \tag{8}$$

where $\mathrm{L}(\Delta f)$ is the phase noise of the LC VCO; Δf is the frequency offset, which is 1 MHz here; f_0 is the central frequency of LC VCO output; P is the power consumption of the LC VCO. Based on the above data, the calculated FOM value of the LC VCO in this design is 185 dB. The results of the comparison between the calculated FOM value in this work and the FOM value of VCOs in some references are given in Table 1; our FOM value is better than those of some references [25,26], and our f_0 is much higher than that of [27]; thus, the present study achieves a better trade-off between the f_0 and FOM value.

Table 1. Comparison results of VCO's Figure of Merit (FOM).

Reference	f_0 (GHz)	Δf (Hz)	P (mW)	L (Δf) dBc/Hz	FOM (dB)
[25]	8	1M	19.1	−105	170
[26]	5	1M	8.76	−105	170
[27]	2.92	1M	3.73	−126.5	190
This work	12.72	1M	3.3	−108.1	185

3.5. Performance Summary

The main specs of the VCO and PLL are summarized in Table 2. The simulation results show that the output noise of the LDO in this study is only 3.06 nV/$\sqrt{\text{Hz}}$ at 1 MHz (Figure 5). Through the above noise optimization, the total output phase noise test result of the LC VCO is 108.1 dBc/Hz at 1 MHz, the FOM value is 185, and the output noise jitter test result of the LC PLL is 0.535 ps (integral range of 1 KHz–90 MHz), all meeting the spec requirements of the SerDes system. The LC PLL is designed based on the UMC 28-nm CMOS 1P10M technology, and the area is approximately 0.25 mm^2. The supply voltage is 1.8 V and the LDO output voltage is 1.1 V. The PLL power consumption is 16.5 mW.

Table 2. Performance summary of LC PLL and LC VCO.

Technology	UMC 28 nm CMOS
PLL Power supply (V)	1.8
LDO output for VCO (V)	1.1
PLL Power (mW)	16.5
VCO power (mW)	3.3
Tuning range (GHz)	8~12.5
PLL jitter (pS)	0.535
VCO phase noise (dBc/Hz)	−108.1@1MHz
VCO FOM (dB)	185

4. Conclusions

The LC PLL designed in this study was applied to a multilane multiprotocol SerDes system. We designed a dual LC VCO containing a voltage-controlled capacitor array, which can improve the coverage of the LC VCO output frequency; a further improvement was achieved by designing a new low-noise LDO regulator structure (Figure 4). It mainly includes a low-noise diode array and a control algorithm circuit. This low-noise LDO is used as a 1.1-V low-noise power supply for the LC VCO to isolate the noise from the 1.8-V power supply. The diode device noise is much smaller than the CMOS device and this LDO output noise does not contain the BG and EAMP noise; therefore, the total noise of this LDO output is very low. After optimizing the LDO noise performance, the VCO and PLL output noise can meet the spec requirements of the SerDes system.

The designed low-noise LDO can easily reduce the area and power consumption when transferred to 14- or even 7-nm technology. Because a critical analog circuit, which includes low-noise BG and low-noise EAMP, is not necessary for this LDO structure, it can also be used in a high-performance SerDes system based on the 14- or 7-nm technology in the future.

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