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A Fully Integrated 64-Channel Recording System for Extracellular Raw Neural Signals

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Abstract: This paper presents a fully integrated 64-channel neural recording system for local field potential and action potential. It mainly includes 64 low-noise amplifiers, 64 programmable amplifiers and filters, 9 switched-capacitor (SC) amplifiers, and a 10-bit successive approximation register analogue-to-digital converter (SAR ADC). Two innovations have been proposed. First, a two-stage amplifier with high-gain, rail-to-rail input and output, and dynamic current enhancement improves the speed of SC amplifiers. The second is a clock logic that can be used to align the switching clock of 64 channels with the sampling clock of ADC. Implemented in an SMIC 0.18 μm Complementary Metal Oxide Semiconductor (CMOS) process, the 64-channel system chip has a die area of 4×4 mm^2 and is packaged in a QFN−88 of 10×10 mm^2. Supplied by 1.8 V, the total power is about 8.28 mW. For each channel, rail-to-rail electrode DC offset can be rejected, the referred-to-input noise within 1 Hz–10 kHz is about 5.5 μV_{rms}, the common-mode rejection ratio at 50 Hz is about 69 dB, and the output total harmonic distortion is 0.53%. Measurement results also show that multiple neural signals are able to be simultaneously recorded.

Keywords: 64-channel; neural recording system; low noise amplifiers; SAR ADC; clock logic

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1. Introduction

Over the past fifteen years, working towards the in-depth understanding of human neural networking, scientists and engineers have greatly developed integrated neural interface systems [1–28]. From central [19] to peripheral [28] nervous system, hundred billions of neurons communicate with each other through electrical firing events and chemical neurotransmitters [29], and the neural interface system helps to track and record them, thereby gradually completing the neural image of the inside of the brain. Health information can be collected for the treatment of chronic neurological disorders, such as epilepsy and Alzheimer's disease [8]. Precision neuroprosthesis can be controlled by amplifying the neural signals and decoding them [2]. To date, the systems have featured more functions, such as electrical, chemical, or optical modulation [29], impedance measurement, wireless power transfer, and data communication [16]. However, the neural recording function is still one of the most critical parts, and the increasing number of simultaneous recording channels brings a trade-off between noise, power, and area.

Compared with traditional bench-top or bulky instrumentation in which a few outside acquisition channels connect electrodes with a bundle of wires, implantable recording

systems on chips together with microelectrode array (MEA) are able to capture much more neural signals with less disturbance [4]. The MEA has hundreds to thousands of electrodes with a scale approximate to neuron size, including the common silicon-based Utah array [2,4,5,8,13], Michigan probe [7,11,19,21–23], or switch matrix [17] for in vivo or in vitro experimentation. With easily reconfigurable properties, MEA is able to select the most interesting sites to be recorded or switch the electrode between recording and stimulation [13]. Today's fabrication has successfully integrated MEA and CMOS-based circuits [11,20–22], so the interference noise and signal attenuation ratio can be reduced due to the long electrode wiring and large parasitics being avoided.

Depending on different MEA types, electrode pitch ranges from tens to hundreds of microns [4,13,17,19], which allows for high-density neural recording. The element neural signal is action potential (AP), also called spike, which is detected by the electrode a few tens of microns away from the neuron [2]. AP's amplitude can be as small as 20 μV [5,8] and is usually less than 1 mV [2,7,8]. The AP's main spectrum starts from about 300 Hz [2,7] and cuts off between 5 kHz and 10 kHz [1–8]. Another cell-level neural signal, called local field potential (LFP), represents the aggregation of electrical activity from the surrounding neurons, which are within the volume of several hundreds of microns from the electrode [8,11]. LFP's amplitude ranges from several hundreds of microvolts up to 5 mV [5], and it varies slowly, with a bandwidth between 1 Hz and 300 Hz [6–11]. Some studies [12,13,16] have also placed electrode grids on the surface of the cerebral cortex to record electrocorticography (ECoG), which is less invasive but still has a moderate amplitude between 10 μV and 500 μV. ECoG's bandwidth ranges from 1 Hz to 500 Hz.

The design of neural electrodes compromises between material, impedance, miniaturization, and lifetime. The cell–electrode interface's impedance should be low enough to mitigate the signal attenuation and its thermal noise. In [9], 20×20 μm^2 Au microelectrodes have been measured, which can be modeled as frequency-dependent resistors in parallel with the capacitor. From 10 Hz to 10 kHz, the impedance decreases from 20 MΩ to 1 MΩ with a mismatch of about 10% and generates integrated noise around 14 μV_{rms}. Moreover, the sum of many smaller spikes acts as background noise, which increases the total electrode's output noise to about 20 μV_{rms} [3]. For most neural signals smaller than 1 mV, the SNR is about 31 dB, so an analogue-to-digital converter (ADC) of above 6-bit resolution [3] would be suitable for the recording system. The DC offset between two electrodes should be of concern as well, which is typically tens of millivolts [8,10,16], but is sometimes as large as 1–2 V [1,3,13]. To avoid saturation due to such a large offset, the recording system usually has the input stage of high-pass filtering, which may be dc-coupled with a feedback low-pass filter [9,12,15,16,20] or ac-coupled with an input capacitor [1–8,17–19,21–28]. Without additional power, the ac-coupled method is passive and easier to achieve.

Working towards high-channel-count design, the recording system has developed some low-power techniques. The current-reuse technique [24] is a common analogue design to achieve low power and low noise, but at the cost of voltage headroom. Reference [30] reviews the recent developments in low-noise biomedical amplifier design based on CMOS technology, including lateral bipolar devices. In addition to biomedical amplifier design methods, signal folding with two threshold-detecting comparators [10] can keep the amplified signal varying in the fixed linear range, so it decreases supply voltage and the demand for ADC resolution. In [25], for time-multiplexing systems, with the help of prior knowledge of an amplifier's bandwidth and noise, the power-area hungry antialiasing filter in every channel can be removed, and the aliased noise is cancelled after ADC by the generated image in the frequency domain. To reduce data throughput and save digital dynamic power, $\triangle$ [4] or $\triangle - \triangle\Sigma$ [23,26] compression algorithms have been applied to one channel signal and channel-to-channel signals because plenty of LFPs in the vicinity have spatio-temporal correlation. APs can also be compressed by spike detection [18,23] due to its temporal sparsity. Before compression, the system needs different filters to select

the corresponding neural signal. However, recording raw information is still popular to keep neural signals' integrity [17–22].

The rest of this paper is organized as follows. Section 2 discusses the overall architecture of a fully integrated 64-channel recording system for extracellular raw neural signals. Sections 3–5 present in detail signal conditioning circuitry, ADC, and timing sequence alignment for time division multiplexing. Section 6 shows the chip floor plan and measurement setup. Section 7 presents the measurement results and performance comparisons. Finally, Section 8 concludes the paper.

2. System Overall Architecture

The presented 64-channel neural recording system is shown in Figure 1. This chip includes a four-stage signal conditioning circuitry, a successive-approximation register (SAR) ADC, bandgap reference and bias circuitry, a digital logic unit for clock and control, and a unidirectional serial peripheral interface (SPI), resulting in a total of 88 input and output pins.

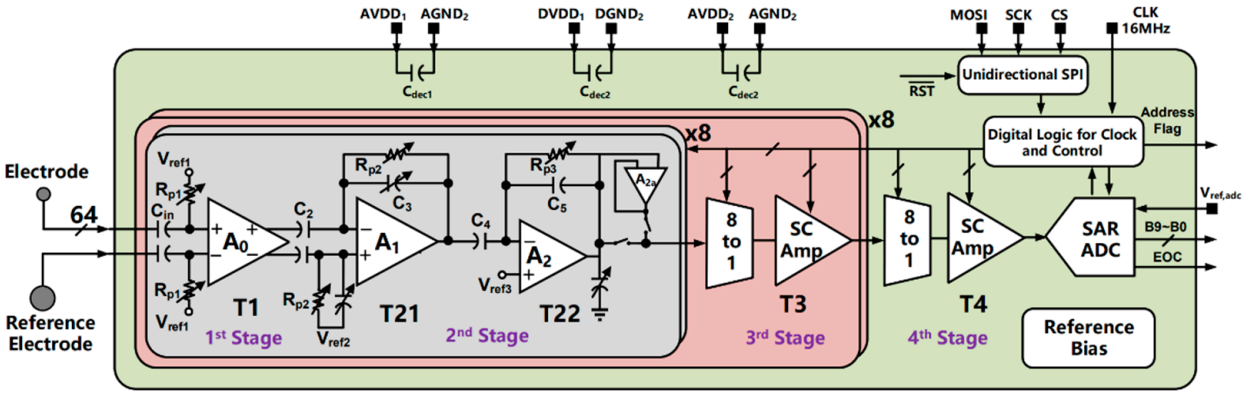


Figure 1. Overall architecture of 64-channel neural recording system.

In the signal conditioning circuitry, from 64 electrodes and the reference electrode, 64 differential signals are separately amplified and filtered by 64 continuous-time first-stage (T1) and second-stage (T2) amplifiers. Through an 8-to-1 analog multiplexer in a repeated cycle, every 8-channel's outputs from T2 are sampled and amplified by a switched-capacitor (SC) amplifier sequentially, which acts as the third stage (T3). Then, the outputs of eight independent T3s are sampled and further amplified by fourth-stage (T4) SC amplifier, which is also the driver of the following SAR ADC. The system gain plans to be programmable from 8 to 4096 by the ratio of a metal–insulator–metal (MiM) capacitor, and T2 is a differential to single-ended antialiasing stage to save capacitance area.

Following the fourth stage, a 10-bit SAR ADC is used, which in parallel outputs 10-bit comparison results and 1-bit end of conversion (EOC). The quantified range of ADC is determined by the off-chip reference voltage from 0 V to 1.8 V. For neural signals mainly within 10 kHz, the sampling frequency of each channel must be at least 20 kHz, so the switching frequencies of T3 and T4 are larger than 160 kHz and 1.28 MHz, respectively. Therefore, the synchronous SAR ADC requires an input clock greater than 12.8 MHz, which is provided by the clock logic unit driven by external clock of 16 MHz. Digital logic units also output the 1-bit address Flag to classify the ADC output channel by channel.

Using four 8-bit registers, a unidirectional SPI, which only transfers data from outside to inside the chip, is able to control system gain and bandwidth and select and reset the recording channel and ADC. The SPI can be self-reset after power on and needs three pins of the serial clock SCK, master output slave input MOSI, and chip select CS.

The bandgap reference generates a temperature-insensitive voltage, which provides bias to T1–T4 and ADC's comparator. The proportional to absolute temperature (PTAT) current source provides constant transconductance bias to the subthreshold circuit.

The AVDD1 and AGND1 are assigned to power supply and ground for T1–T4 and bandgap reference, AVDD2 and AGND2 for ADC, DVDD1 and DGND1 for SPI, and digital logic. AVDD1 and AVDD2 are 1.8 V, and DVDD1 can be 1.5 V–1.8 V. Sufficient decoupling capacitors have been added between the power supply and the ground to reduce the voltage ripple induced by bonding wire.

3. Signal Conditioning Circuitry

3.1. Low-Noise Open Loop Amplifier

In Figure 2, T1 is designed as a passive high-pass filter (HPF) followed by an open-loop amplifier A_0. The electrode dc offset over 1 V is able to be blocked by C_{in} about 5 pF, and A_0's input is biased by V_{ref1} by about 0.6 V through pseudo-resistor R_{p1}, which is formed by two in-series thick PMOS transistors connecting the source and body together. When S_1 is closed and S_2 is open, PMOS transistors are biased in the deep subthreshold region, so high-pass corner f_{HP1} is able to be very low, about 5 mHz, and therefore T1 amplifies the neural signal normally. When S_2 is closed and S_1 is open, f_{HP1} is increased to about 18 kHz, and T1 recovers quickly in the presence of artificial interference, which may cause several hundred millivolts of fluctuation at the input of the T1. The RL12 are 1.3 MΩ; otherwise, in order to ensure accurate matching between RL12, we connect several resistors in series with RL12, each of which has a resistance of about 25 kΩ and is controlled by a switch.

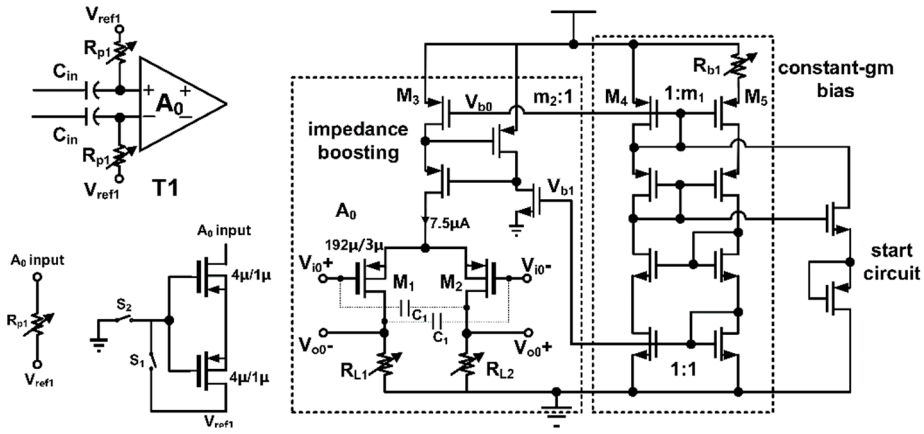


Figure 2. The schematic of T1.

The recording system's referred-to-input (RTI) noise is mainly determined by T1, including thermal and 1/f noise, so using as few components contributing to noise as possible can achieve low noise. With a limited gain of about 8, A_0 is a differential common-source amplifier, which works in open-loop and has enough linearity for a weak neural signal. The input transistor $M_{1,2}$ is thick PMOS and the load $R_{L1,2}$ is poly-resistor. The size of $M_{1,2}$ is large to reduce 1/f noise, and the positive feedback cross-coupled capacitor C_1 can compensate parasitic capacitance at A_0's input to minimize input signal attenuation. The RTI noise of T1 comes from R_{p1}, $M_{1,2}$, and $R_{L1,\,2}$, and its power spectral density (PSD) is derived as:

$$\overline{V_{n,T1}^2} = 4kTR_{p1} \cdot \left(\frac{f_{HP1}}{f}\right)^2 + \frac{2K_p}{C_{ox}WL}\frac{1}{f} + \frac{8kT\gamma_p}{g_{m1}} + \frac{8kT}{g_{m1}{}^2R_{L1}} \quad (1)$$

in which the first term can be ignored from 1 Hz to 10 kHz because of very low f_{HP1}.

To keep A_0's gain variation low from different processes and temperature (PT), a constant-gm bias scheme [17] is adopted. All transistors are biased in the subthreshold region and a PTAT current is generated for the A_0 tail current. Then, A_0's gain is derived as:

$$A_0 = \frac{m_2 ln(m1)}{2} \cdot \frac{R_{L1}}{R_{b1}} \quad (2)$$

which has weak dependency on the temperature and process when $R_{L1,2}$ is matched with R_{b1} and current mirror is also matched.

3.2. Amplifiers of Programmable Gain and Bandwidth

In Figure 1, to continue amplifying the output of T1 and also as an anti-aliasing stage, T2 uses two cascading closed-loop amplifiers. The former stage T21 is a differential to a single-ended amplifier [2], which sets the system's high-pass cut-off frequency $f_{HP,sys}$ and has a programmable gain of ($-C_2/C_3$). Adjusting C_3 changes T21's 3 dB low-pass cut-off frequency, so A_1 needs enough gain-bandwidth product (GBW). The latter-stage T22 has a similar structure but with fixed gain, and sets the system's low-pass cut-off frequency $f_{LP,sys}$. Because one channel's sampling frequency is about 20 kHz, $f_{LP,sys}$ is set around 6 kHz to keep the noise effective bandwidth within 10 kHz to avoid noise aliasing.

The pseudo-resistors R_{p2} and R_{p3} used by T21 and T22, respectively, adopt a structure similar to [17]. In Figure 3, R_{p2} is realized by two in-series thick PMOS $M_{p1,2}$, which can provide dc bias for A_1 and determine $f_{Hp,sys}$ in parallel with C_3. Despite PT variations, the level shifter formed by $M_{p3–5}$ and tunable $I_{b1,2}$ can reduce R_{p2} 's resistance spread. The resistance for R_{p2} is determined by the override voltage of $M_{p1,2}$, which can be written as:

$$V_{OV,p1,2} = (V_{OV,p4} + V_{OV,p5} - V_{OV,p3}) + (V_{TH,p4} + V_{TH,p5} - V_{TH,p3} - V_{TH,p1}) \quad (3)$$

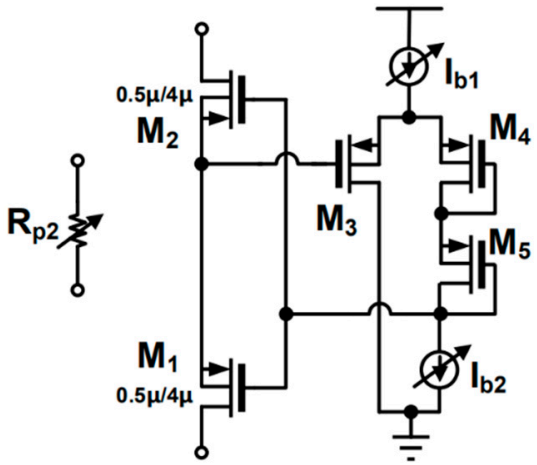


Figure 3. Pseudo-resistor structure for R_{p2}.

From (3), $V_{ov,p1,2}$ shows weak dependency on PMOS threshold voltage V_{TH} that has strong dependency on PT variations. This structure can also follow the output voltage of the amplifier, thus making R_{p2} steady in a wider voltage range than a conventional pseudo-resistor such as R_{p1}. In addition, with a 7-bit DAC current source realized by the MOSFET-only R-2R ladder structure [17], $I_{b1,2}$ can adjust $f_{Hp,sys}$ against PT variations or increase $f_{Hp,sys}$ to reset the amplifiers' bias in T2.

Within TCH = 50 µs, which is the sampling period for every channel, the T3 SC amplifier has to access eight channels' signals in sequence. However, because T22's bandwidth and time constant τ_2 are 6 kHz and 26.526 µs, respectively, the charging settling error can be 15% even if the charging time is 50 µs. To maintain 10-bit resolution, in Figure 4, a buffer using an auxiliary amplifier A_{2a} is added at the output of T22 to pre-charge C_6, and then T22 is switched to complete charging and filtering. The buffer with load C_6 is designed to have a bandwidth of 300 kHz with time constant τ_{2a}, and A_{2a}'s open-loop gain is 60 dB. If S2a_O<11> closes for $t_{2a} = T_{CH}/16$ and then S2_O<11> closes for $t_2 = T_{CH} \times 7/8$, the output charging settling error can be derived as:

$$er_{set} = \left[\frac{1}{1 + A_{2a}} + \frac{A_{2a}}{1 + A_{2a}} \exp\left(-\frac{t_{2a}}{\tau_{2a}}\right)\right] \exp\left(-\frac{t_2}{\tau_2}\right) \quad (4)$$

which equals about 0.07%. The error can be reduced by increasing A_{2a} or decreasing τ_{2a}. Consequently, before one channel's signal enters T3, A_{2a} precharges and then T22 charges a sample and hold (SH) capacitor C_6 in an 8-to-1 multiplexer.

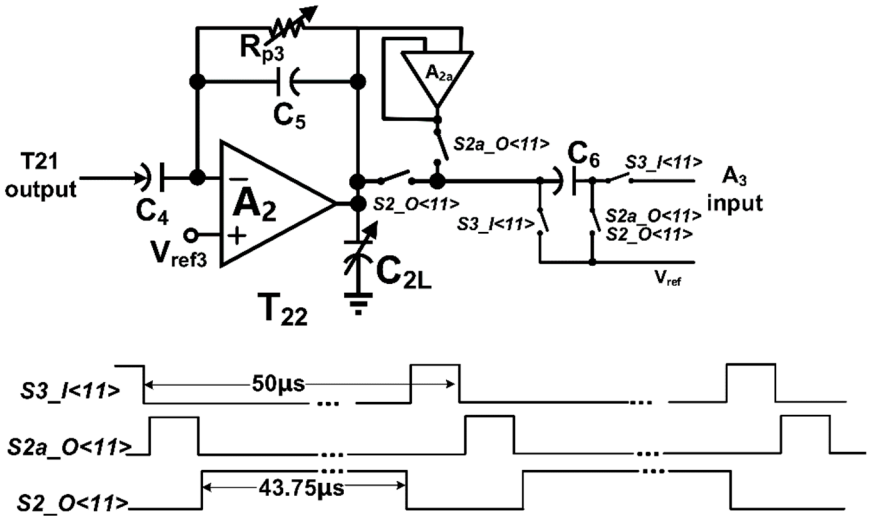


Figure 4. T22's realization and auxiliary buffer.

Because T1 and T2's total gain is able to reach 128 at most, T2's amplifier output's voltage headroom and open-loop gain should be large enough to maintain linearity. In Figure 5, a folded-cascode amplifier is used by A_1, A_2, and A_{2a}. The peak-to-peak value of output swing can be as large as 1.2 V, and auxiliary amplifiers are used to boost impedance and open-loop gain. In terms of low RTI noise, the amplifier consumes less power due to T1's gain. In order to reduce the noise contribution from $M_{23–26}$, $M_{21,22}$ are biased in the subthreshold region, while $M_{23–26}$ are biased in the strong inversion region and have a large size. In addition, the static current flowing through $M_{21,22}$ should be several times the static current of $M_{25,26}$.

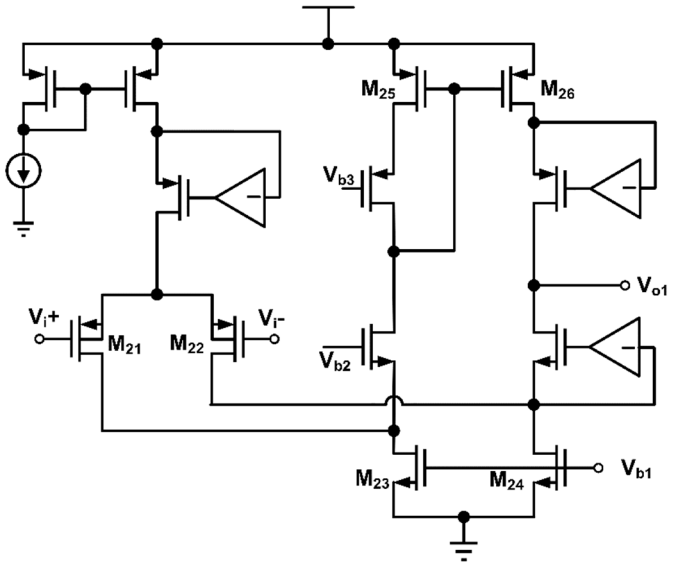


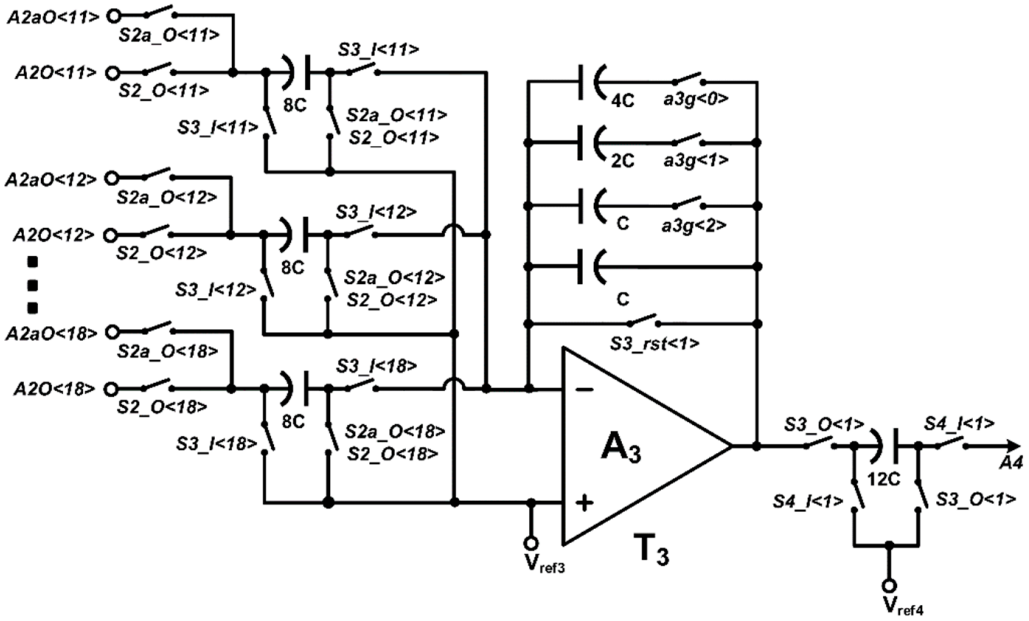
Figure 5. Schematic of A_1, A_2, and A_{2a}.

3.3. Switched-Capacitor Design of T3 and T4

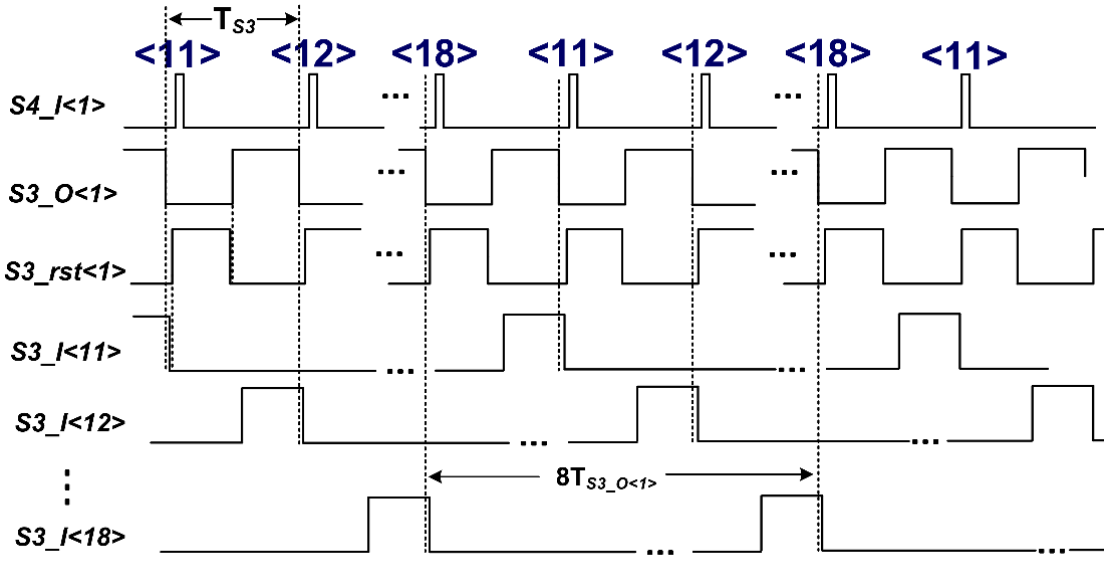
When T1 and T2's gains are set to 128, the aliasing noise from T3 and T4's SC circuits has a small effect. For time division multiplexing design, to reduce the memory effect

and improve the isolation between channels, the SC amplifier needs to be reset before amplifying one channel's signal. There are eight T3s and one T4.

Figures 6 and 7 show the design of T3 and T4, which both use the structure of non-inverting SC amplifier. Controlled by SPI, T3 has a programmable gain of {1,2,4,8}, and T4 has a programmable gain of {1,2,3,4}. The reference voltage for T3 and T4 is 0.9 V. All switches use CMOS transmission gates. Because the switching periods for T3 and T4 are T_{s3} = 1/160 KHz and T_{s4} = 1/1.28 MHz, respectively, the output impedance of the reference buffer for V_{ref4} and the CMOS switches in T4 is lower than that in T3.



(**a**)



(**b**)

Figure 6. (**a**) T3′s structure (**b**) T3′s timing sequence.

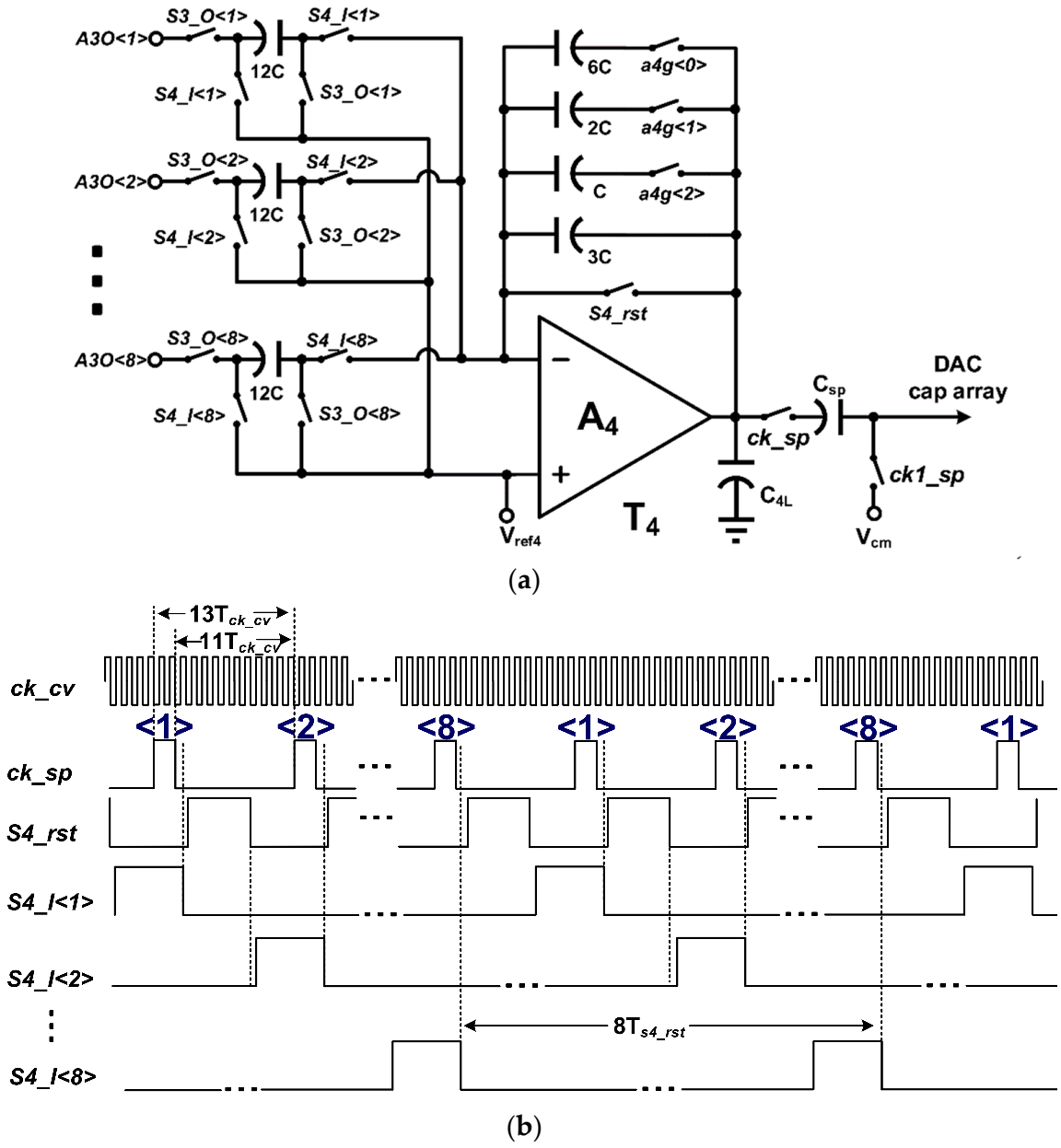


Figure 7. (**a**) T4′s structure (**b**) T4′s timing sequence.

In Figures 6b and 7b, the clocks with the opposite phases do not overlap each other. For T3, within a T_{s3}, there is the amplification phase S3_I <1 X> (X = 1–8) and the reset phase S3_rst <1>. The delay between T3's amplification phases for two adjacent channels is T_{s3}. Because the switch's charge injection and clock feed-through effect have greater influence on A_3's input than output, S3_O <1> is turned off earlier than each S3_I <1 X>. In Figure 7a, T4 not only serves as the multiplexed stage for the eight T3s but also drives the SH capacitor C_{sp} of SAR ADC. The period $T_{ck\text{-}sp}$ of ADC's sampling switch ck_sp is equal to T_{s4}, which equals 13 times that of T_{ck_cv}, which is the synchronous clock inside SAR ADC. The switch ck_sp keeps high for $2T_{ck\_cv}$. Within a T_{s4}, there is the amplification phase S4_I <1 X> (X = 1–8) and the reset phase S4_rst. The delay between T4's amplification phases for two adjacent T3s' outputs is T_{s4}.

The obtain 10-bit resolution, the open-loop gain and bandwidth of A_3 and A_4 should be large enough. When all gain control switches a3g in Figure 6a are open, the feedback factor of the T3 SC amplifier is 1/9. The open-loop gain of A_3 is over 80 dB to make a closed-loop gain error of less than 0.1%, and the GBW of A_3 is designed at about 3.6 MHz

to make a dynamic settling error of less than 0.1%. When all gain control switches a4g in Figure 7a are open, the feedback factor of the T4 SC amplifier is 1/5. The open-loop gain of A_4 is over 74 dB to make a closed-loop gain error of less than 0.1%. Because switch ck_sp is closed for only 2ck_cv when C_{sp} is charged, A_4 has a load capacitor C_{4L} and GBW of about 45 MHz to guarantee a settling error of less than 0.1%.

Because signal is further amplified by T3 and T4, T3 and T4 should be able to offer a nearly rain-to-rail output swing. There are some rail-to-rail CMOS buffers with slew rate enhancement, such as [31,32]. In this paper, a fully differential rail-to-rail amplifier's topology with slew rate enhancement is proposed in Figure 8. Using complementary input of PMOS and NMOS differential pairs with equalized transconductance over a wide common-mode input range, A_3 and A_4 can also tolerate a large input swing, which may happen in the SC circuit. For example, in Figure 7, A3O <1> is VDD or 0, when S4_I <1> is closed, due to T4.

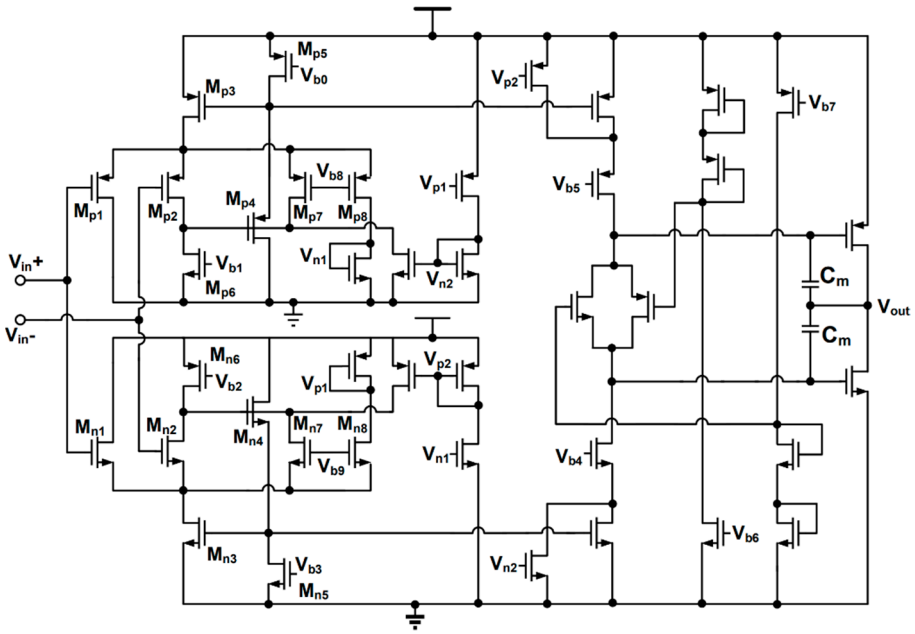


Figure 8. The schematic proposed for A_3 and A_4.

SC amplifier's limited bandwidth and large voltage offset will stay at A_4's input for a while, and at least one differential pair of the input stage is able to work. In order to improve open-loop gain, the amplifier's first stage is a current-mirror cascode structure, and the second stage is a Class-AB push–pull structure with a trans-linear bias circuit. A Miller compensation capacitor is added to obtain enough of a phase margin.

Moreover, this amplifier's first stage can output a boosted dynamic current larger than the conventional structure [2] whose output maximum current is limited by the tail current. In Figure 8, like for the PMOS differential pair, V_{in+} is biased by the reference voltage, and the current of M_{p2} is fixed by that of M_{p6}. Because of the super source follower formed by M_{p2-6}, the source of M_{p2} follows V_{in-}, and then the dynamic output current of the first stage is expressed as:

$$I_{outp} = \frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)_p (V_{in+} - V_{in-})^2 + g_{mp1}\cdot(V_{in+} - V_{in-}) \quad (5)$$

Because I_{outp} has a term proportional to $(V_{in+} - V_{in-})^2$ added to the conventional linear term, when there is a large differential input, the first stage's output current is boosted, and the SC amplifier's speed is enhanced.

4. Design of 10-Bit SAR ADC

A SAR ADC is time-multiplexed to quantify all channels' signals. In Figure 9a, ADC is mainly composed of a DAC capacitors array, comparator, and SAR logic and clock logic units. The connection of each bit capacitor's bottom plate is controlled by the D9–D0 logic value, where '0' is for the ground and '1' is for V_{ref}, which is provided from off-chip. The on-chip reference voltage Vcm is about 0.9 V. To save area space, the DAC capacitors array is divided into the six most significant bits (MSB) and the four least significant bits (LSB) by unit bridge capacitor C. The unit capacitor C is about 100 fF. Shown in Figure 9b, the comparator consists of three cascading preamplifiers and a dynamic Latch comparator.

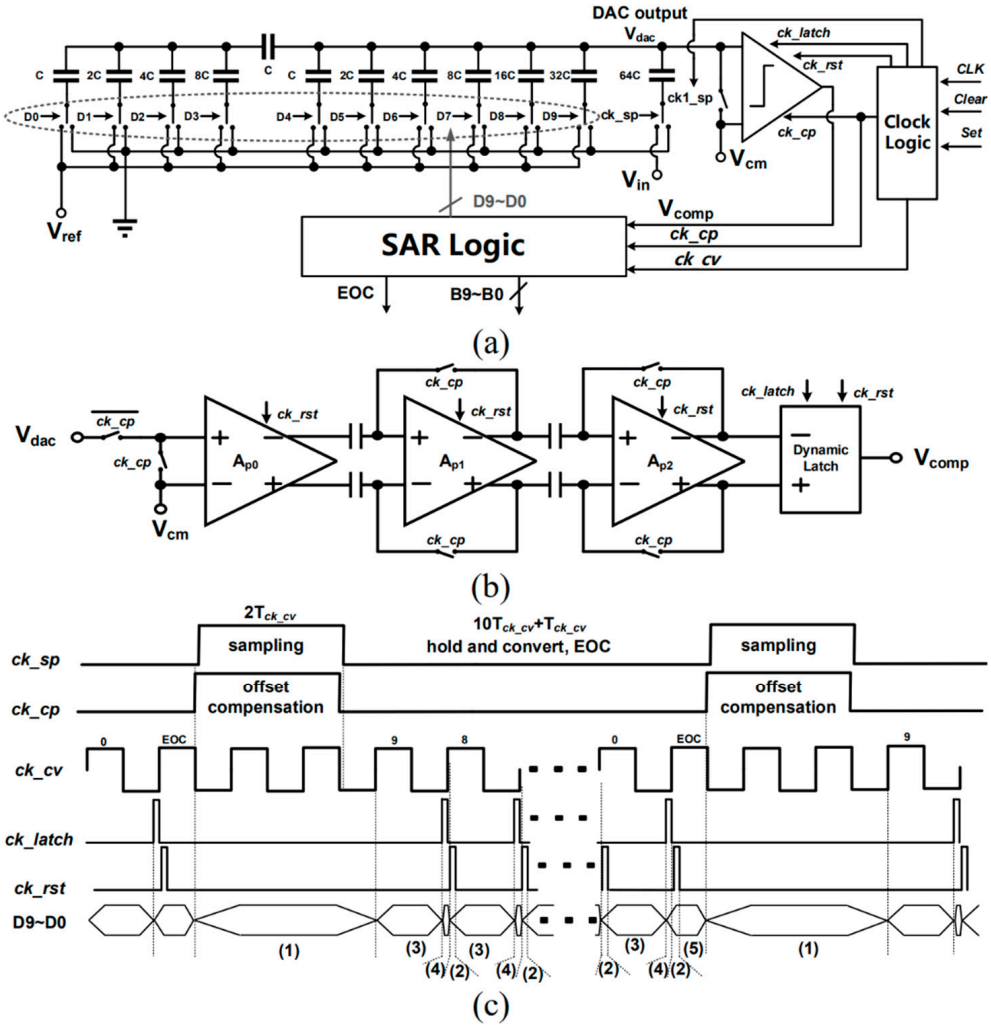


Figure 9. (**a**) The schematic of SAR ADC. (**b**) The schematic of comparator. (**c**) The timing diagram of SAR ADC.

In Figure 9c, according to the timing diagram of control clocks, SAR ADC works as follows. Sampling phase: (1) the output of T4 in the amplification phase is sampled by capacitor 64C, D9–D0 and EOC are cleared to '0', and the comparator uses the auto-zeroing technique to compensate the offset. This phase lasts for $2T_{ck\_cv}$. Comparing phase: to convert the sample to 10-bit data, from D9 to D0, DAC output is held and converted for 10 cycles, in which (2) DN is set to '1' and the comparator is reset, (3) preamplifier works, and (4) the latch comparator finishes this bit. After $10T_{ck\text{-}cv}$, (5) ADC outputs the end of conversion (EOC) '1' and keeps all 10-bit results for T_{ck_cv}, and ADC is ready for the next sampling phase. The sampling clock has a period the same as T_{s4} and 13 times that of T_{ck_cv}.

The DAC output before the comparator is expressed as:

$$V_{dac} = V_{cm} - \frac{64}{127 + \frac{15}{16}} \times \left(V_{in} - \frac{1}{2} D_9 V_{ref} - \frac{1}{2^2} D_8 V_{ref} - \ldots - \frac{1}{2^{10}} D_0 V_{ref} \right) \quad (6)$$

in which D_9–D_0 is equal to '1' or '0'. In the conversion state, because V_{dac} gradually approaches V_{cm} and V_{ref} ranges from 0 to 1.8 V, the variation in the comparator's input common-mode voltage can be no more than 0.225 V. Therefore, the input stage of the preamplifier can always work properly, and its input-referred offset variation is small. In Figure 10a of the preamplifier, A_{p0} has a gain of about 5, and $A_{p1,2}$ has a gain of about 10. When ck_rst is high, the output of the preamplifiers is shortened to eliminate the residue state caused by the last bit's conversion to avoid a hysteresis effect. Figure 10b shows a conventional-sense amplifier, including an inverter-based (INV) regenerative latch, followed by an NAND-based latch. When ck_latch is '0', consuming little static power, the INV latch has been reset and then follows A_{p2}'s output, while the NAND latch keeps the last state. When ck_latch is '1', the INV latch works, and the following inverter and NAND latch restores its output to the logic value V_{comp}, which is the compared result for the current bit.

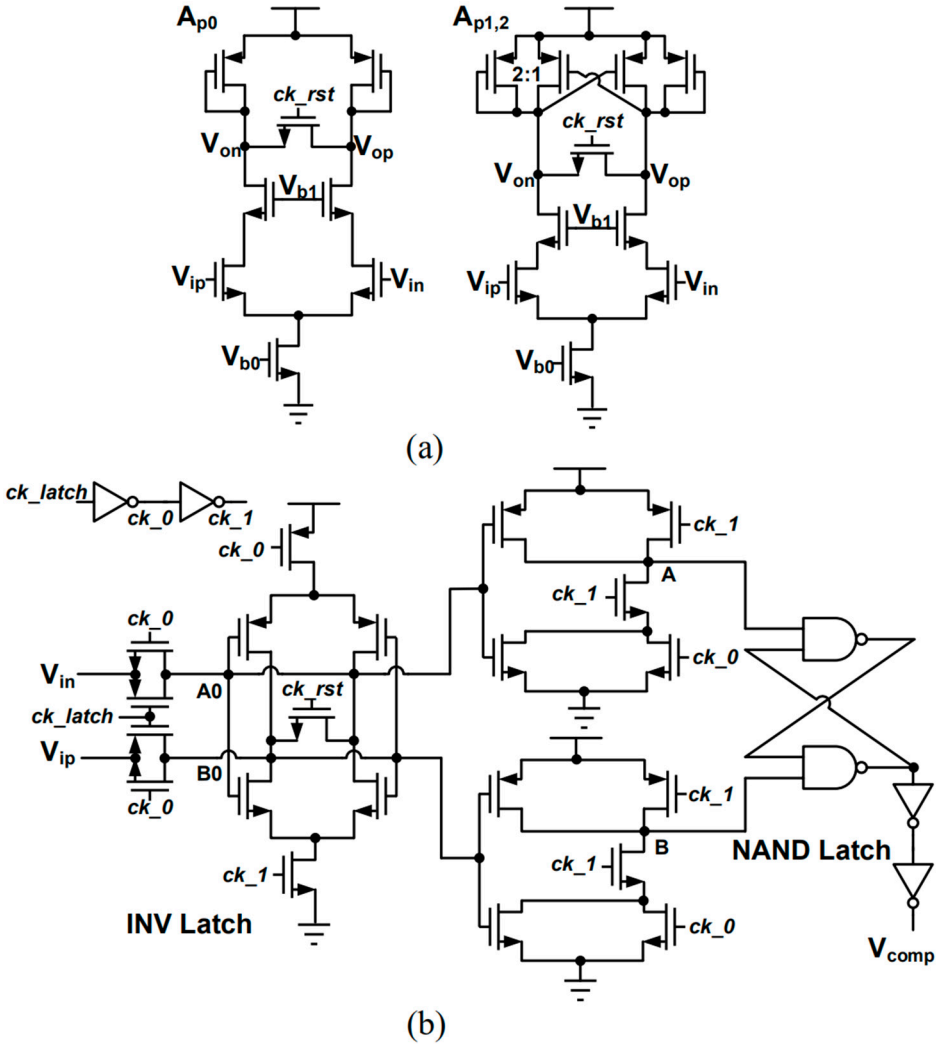


Figure 10. (**a**) The schematic of preamplifiers. (**b**) Dynamic latch comparator.

5. Synchronous Design of Timing Sequence

To properly record every channel's signal, the sampling clock of ADC has to be aligned with the channel switching clock, which is used for time division multiplexing in signal

conditioning circuitry. In Figure 7, to ensure that each channel's signal is successfully established at T4's output when ADC is sampling, the logic high state of the sampling clock ck_sp should fall within and close to the end of the logic high state of each S4_I <X>. As for the clocks of each analogue stage in Figures 4, 6 and 7, all of them can be realized by the clock S4_rst through a D flip-flop-based frequency divider and related digital logic circuits. In the D flip-flop, when CLR = '0', Q = '0', and when SET = '0', Q = '1'.

In Figure 11 of the proposed digital circuit, S4_rst can be generated. As the delayed clock of the external clock CLK, ck_cv is the synchronous clock for all D flip-flops. Before the synchronization of all clocks, by setting clear to '0' through SPI, all clocks and clock logic circuits are cleared. Once clear is set to '1', ADC starts to work. Before the first falling edge of the ADC sampling clock ck_sp, M0 and M2 are on, M1 and M3 are off, df7 outputs Q = '1', and S4_rst is '0'. After ck_sp's first falling edge, M0 turns off and M1 turns on, and the next rising edge of ck_cv triggers S4_rst = '1'. After 5 T_{ck_cv} and ck_cv's rising edge, df6 outputs Q = '1', M2 turns off and M3 turns on, and S4_rst remains as '1' for another T_{ck_cv}. Clock ck_cv's next rising edge triggers S4_rst = '0'. After 5 T_{ck_cv} and ck_cv's rising edge, df6 outputs Q = '0', M3 turns off and M2 turns on, df7 outputs Q = '0', and S4_rst remains as '0' for another 2 T_{ck_cv}. So far, ck_sp is aligned to S4_rst, and all the clocks can be synchronized in the following repeated cycle.

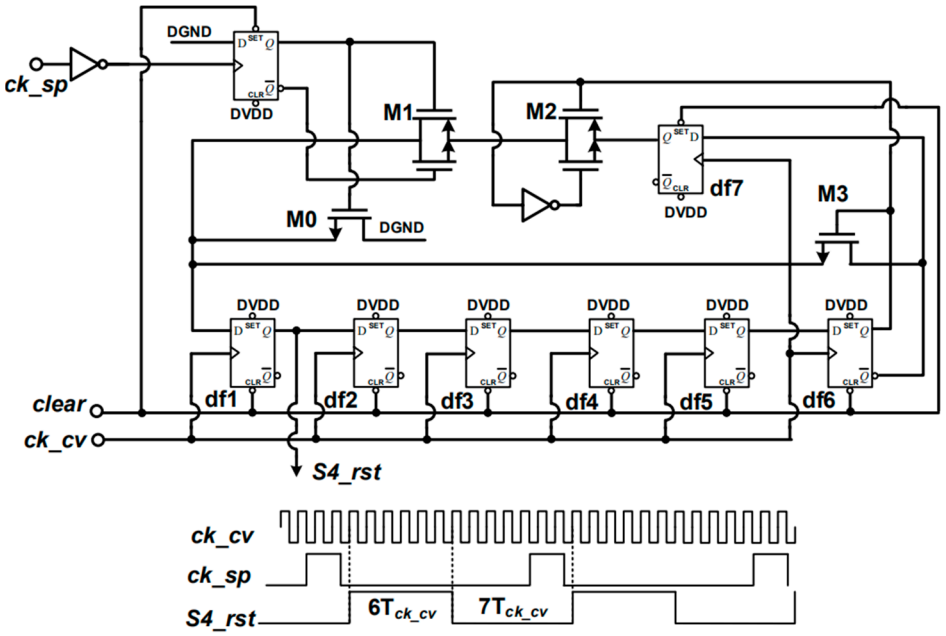


Figure 11. The proposed digital circuit to generate S4_rst.

In addition, ADC's output packets need to be matched with each channel. In this design, only 1-bit address is needed as the Flag for data allocation. In Figures 6b and 7b, if clock S4_I <1> and a clock 100 ns delayed by S3_I <11> enters an AND gate, the address Flag can be obtained. When Flag = '1', it indicates that after one ADC sampling period, ADC's first output is the first channel's quantified data, and the subsequent output can be allocated to other channels.

6. Chip Floorplan and Measurement Setup

Implemented in the SMIC 0.18 μm CMOS standard process, the 64-channel neural signal recording system chip has been taped out and packaged. Figure 12 shows the chip die of 4 × 4 mm^2 and its QFN-88 package of 10 × 10 mm^2. The chip has a total of 88 pins. The first three stages T1–T3 of the signal conditioning circuitry are divided into eight independent modules, each module contains eight channels, and the fourth stage T4 is

next to the ADC. Other parts include SPI and four 8-bit registers, bandgap reference and bias circuitry, a digital logic unit, and an on-chip decoupling capacitor.

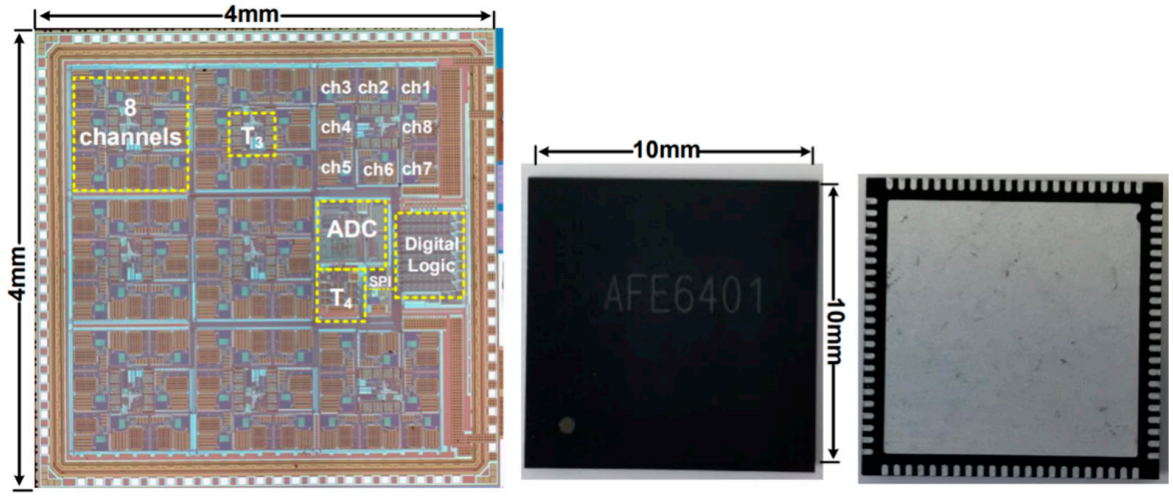


Figure 12. Chip floorplan and package.

Powered by battery, the measurement PCB and setup are shown in Figure 13. One LDO outputs 1.8 V for AVDD1 and AVDD2, and one LDO outputs 1.5 V for DVDD1. A crystal oscillator was used to provide a clock of 16 MHz, leading to the sampling rate of ADC being 1.23 MS/s and the average sampling frequency of each channel is 19.2 kHz, as is acceptable. Resistors and capacitors can be connected in series or parallel to emulate electrodes. The chip's input signal was provided by a Tektronix AFG3252 arbitrary waveform generator, which can generate sinusoidal and neural signals. In order to reduce test complexity, all channels used the same signal source, and the common reference input can be switched to the ground. The laptop used a device to convert USB to SPI to adjust the system's gain and bandwidth, select the recording channel, change the pseudo-resistor's value, reset and clear ADC and digital circuit. For collecting the system' digital output, the Agilent 16802A logic analyzer was used, which can be triggered by EOC and Flag.

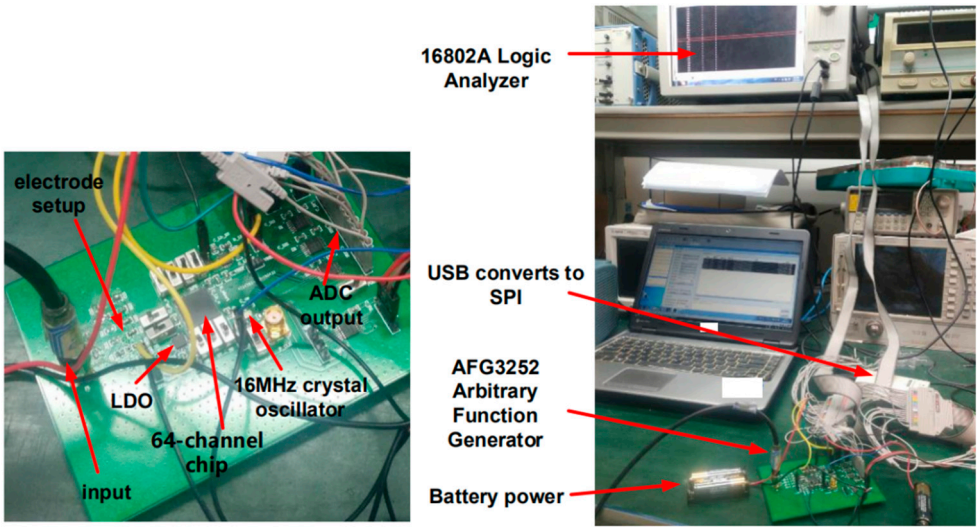


Figure 13. Measurement setup.

7. Measurement Results

When the chip worked with an input clock of 16 MHZ, the analogue part consumed 4.3 mA, including signal conditioning circuitry, ADC, bandgap reference and bias cir-

cuit, and the digital part consumed 0.3 mA. The total power consumption was about 8.28 mW with an average heat of 517.5 $\mu W/mm^2$, which is less than the heat budget of 800 $\mu W/mm^2$ [10]. The average power consumption of each channel was about 130 µW. After the operation for clock synchronization by using SPI, Figure 14 shows that from the logic high state of Flag, one ADC sampling period later, ADC output data of the first channel firstly and then other channels in the sequence of channel 1, 9, 17, 25, 33, 41, 49, 57, 2, 10, 18, 26, 34, 42, 50, 58, 3, 11, 19, 27, 35, 43, 51, 59, 4, 12, 20, 28, 36, 44, 52, 60, 5, 13, 21, 29, 37, 45, 53, 61, 6, 14, 22, 30, 38, 46, 54, 62 7, 15, 23, 31, 39, 47, 55, 63, 8, 16, 24, 32, 40, 48, 56 and 64.

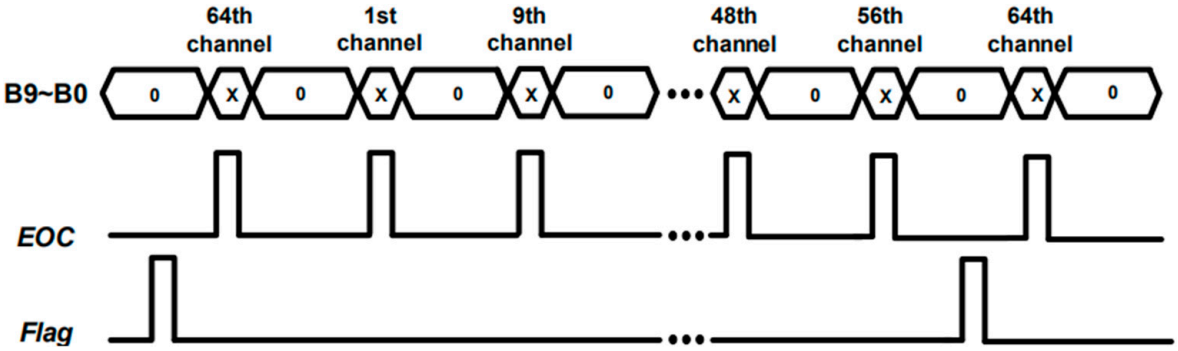


Figure 14. The chip's output data and timing sequence.

In noise measurement, one channel's differential inputs were shorted to the ground, and all corresponding ADC 10-bit data were selected and converted back to analogue signal. After dividing the output by the system gain, the RTI noise PSD was calculated and is plotted in Figure 15. It can be seen that with the increasing system gain, the RTI noise decreases to a constant value. When T1 and T2 had a total gain of 16, and T3 and T4 had a gain of 1, within 1 Hz–10 kHz, the system's integrated RTI noise was about 32 μV_{rms}, which was dominated by T3, T4, and ADC. When T1 and T2's gain was increased to 128, the integrated RTI noise was about 6.2 μV_{rms}. Furthermore, T3's gain was programmed to 2, the system gain became 256 or more, and the integrated RTI noise was about 5.5 μV_{rms}, which was dominated by T1 and T2.

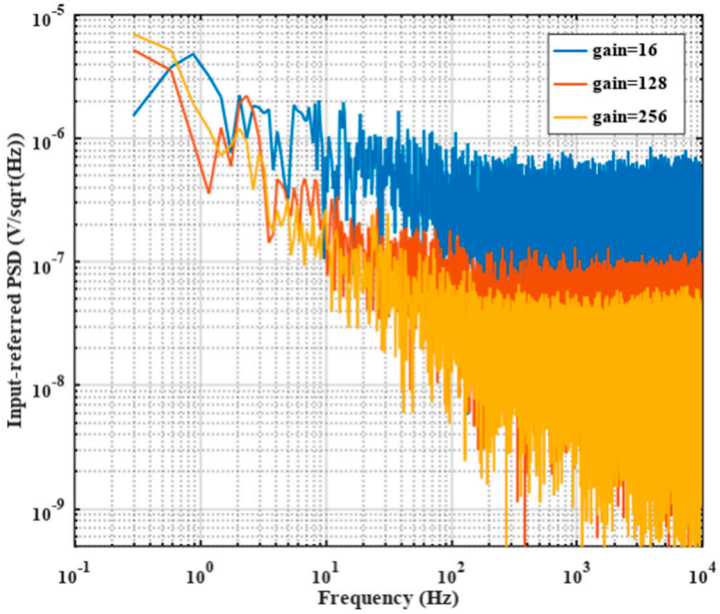
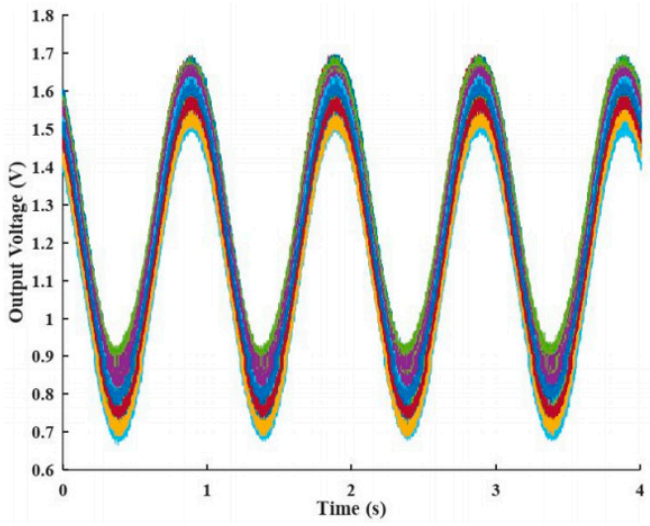


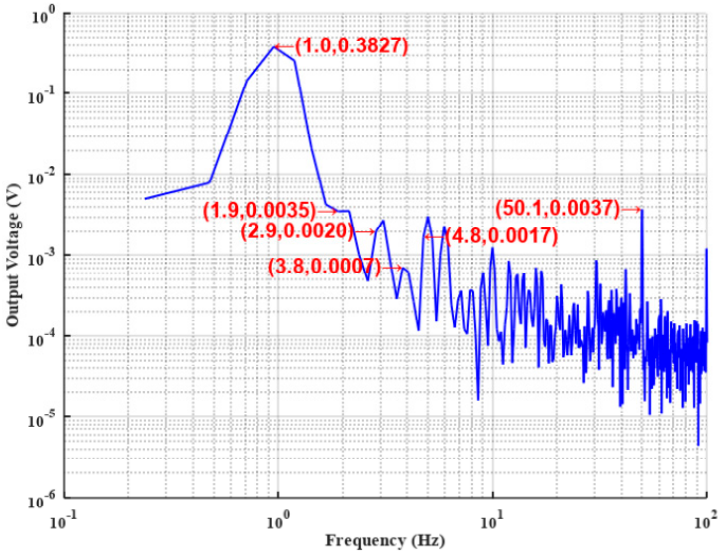
Figure 15. The RTI noise of system with different system gain.

The common-mode interference for implantable application usually comes from the Power frequency interference and is tens of millivolts. Therefore, the CMRR at 50 Hz is necessary. When the system's gain is 128, one channel's differential inputs are shorted to the same signal source to test CMRR, and the tested CMRR at 50 Hz is about 69 dB.

In order to verify that the system is able to normally record very-low-frequency signals, a sinusoidal signal of 3 mV and 1 Hz was input into all channels, and system gain was set to 128. Figure 16a shows all 64-channel output waveforms and Figure 16b shows the frequency spectrum of one of the 64 channels. It can be calculated that the measured system gain was about 127.5, and considering four harmonics, the total harmonic distortion (THD) was about −38.7 dB (1.16%). Because the system's first stage determines the linearity of entire channel and its input stage is an open-loop amplifier, the linearity is greatly affected by the input signal's amplitude. In Figure 17a, when system gain was set to 512 and a sinusoidal signal of 1 mV and 11 Hz was input to all channels, the measured system gain was about 511.4. Figure 17b shows the frequency spectrum of one of the 64 channels, and the THD was about −45.5 dB (0.53%). Therefore, neural signals of several hundred microvolts can be recorded with an acceptable distortion.

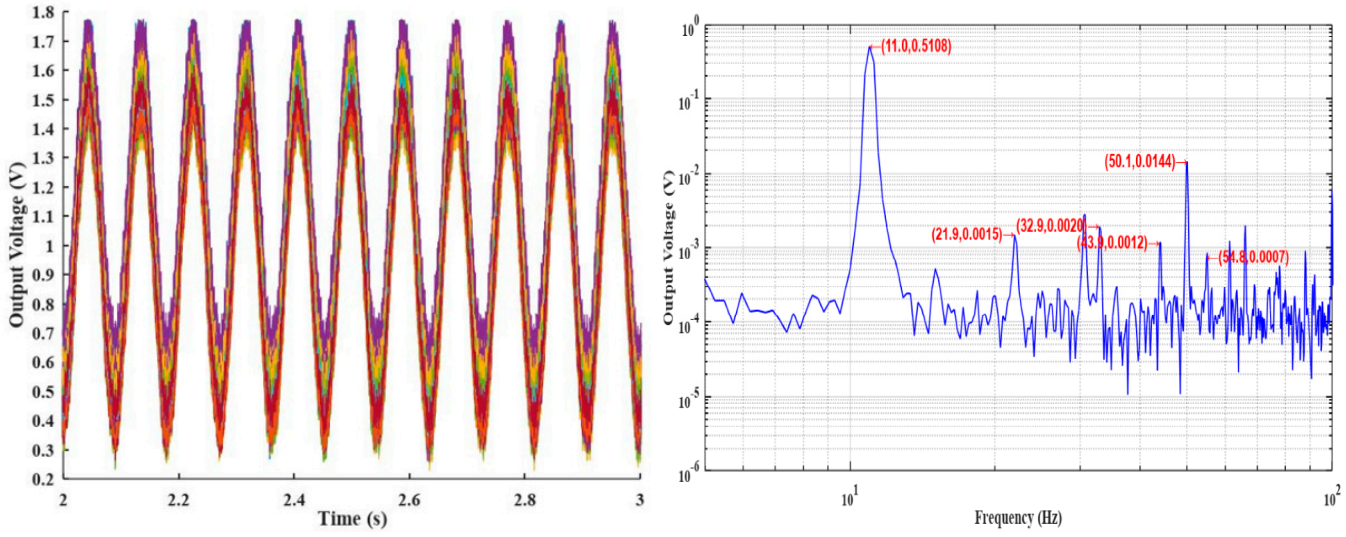


(**a**)



(**b**)

Figure 16. All channels' (**a**) output waveforms, (**b**) frequency spectra from 3 mV–1 Hz sinusoidal input.



(**a**) (**b**)

Figure 17. All channels' (**a**) output waveforms, (**b**) frequency spectra from 1 mV–11 Hz sinusoidal input.

From the output waveform, it can be seen that there was a dc offset between different channels, which is because the adopted pseudo-resistor has resistance and leakage current variations. In Figure 3, the parasitic diode in reverse biasing between PMOS N-well and P-substrate has a leakage current related to process, temperature, and light [33]. In Figure 4, because the negative input of A_2 is virtually ground and fixed by V_{ref}, R_{p3}'s leakage current flowing through itself can cause DC offset at the output of A_2. This offset may saturate the amplifier and the system; thus, the system's maximum gain is 512 for now to ensure enough voltage headroom.

From the CRCNS (Collaborative Research in Computational Neuroscience) website, the raw neural data were downloaded, which is provided by the laboratory of Professor Gyorgy Buzsáki of New York University. The neural data recorded the CA1 region of the hippocampus of anesthetics rats, including extracellular LFP signals and AP signals of about several hundred millivolts [34]. To minimize the noise floor of the test instrumentation and cables, neural signal was pre-amplified by 50 in Tektronix AFG3252, and then was input into the system through a 1/50 attenuation network and electrode impedance network. In the test, ADC's total output data were distributed to 64 channels and divided by 512 to obtain the equivalent input neural signal of each channel. Since neural signal is not concerned with the dc component, the data recorded in all channels were subtracted from the corresponding dc component. Figure 18a,b show arbitrary four-channel LFP and AP signals with amplitude fluctuations of about 200 μV and 300 μV, respectively. The AP signal is mainly composed of multiple fast spikes. In Figure 19 of the zoomed-in waveform of Figure 18b, the spike has a duration of about 2 ms.

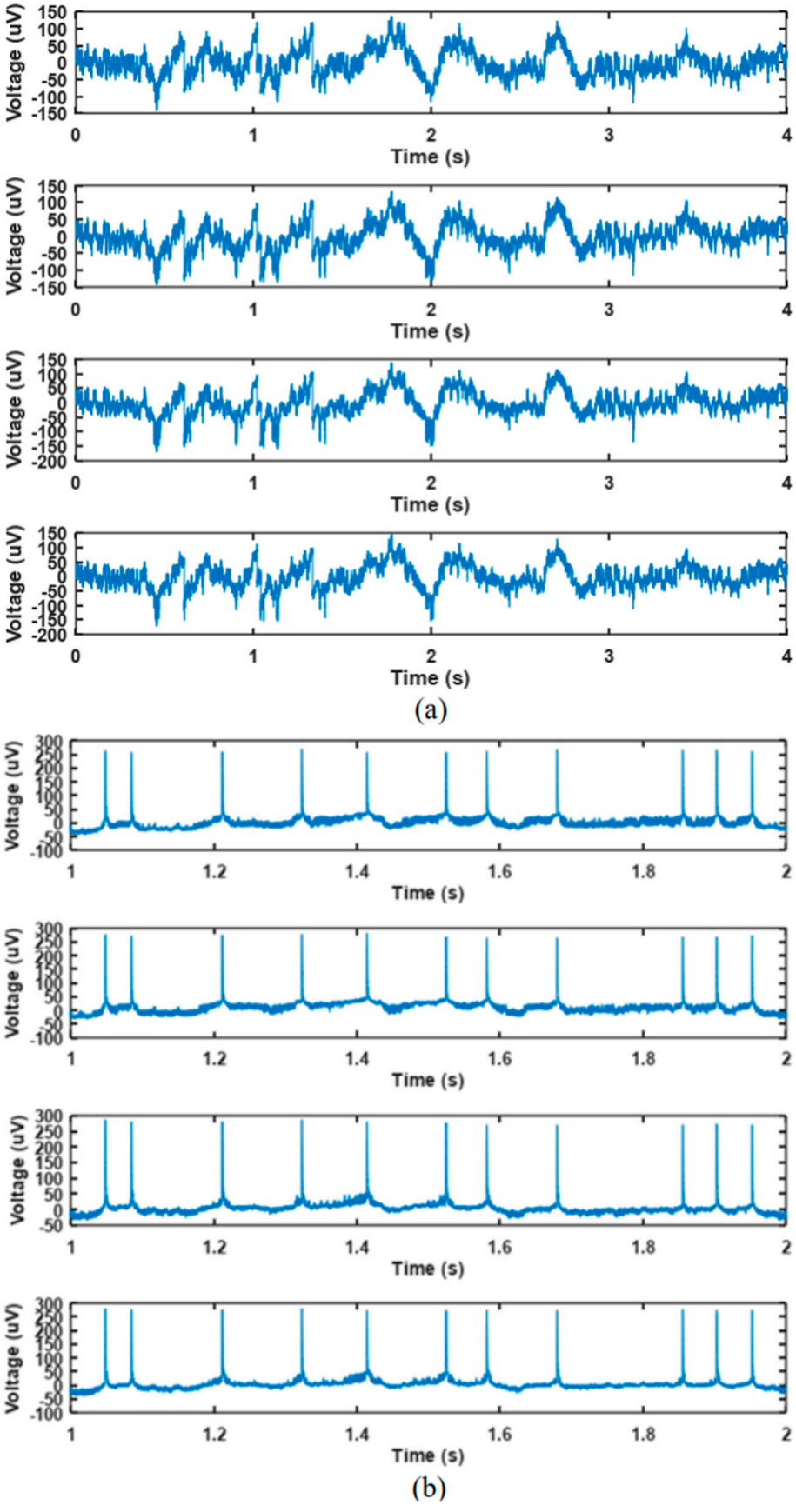


Figure 18. Arbitrary four-channel output from the same (**a**) LFP signal, (**b**) AP signal.

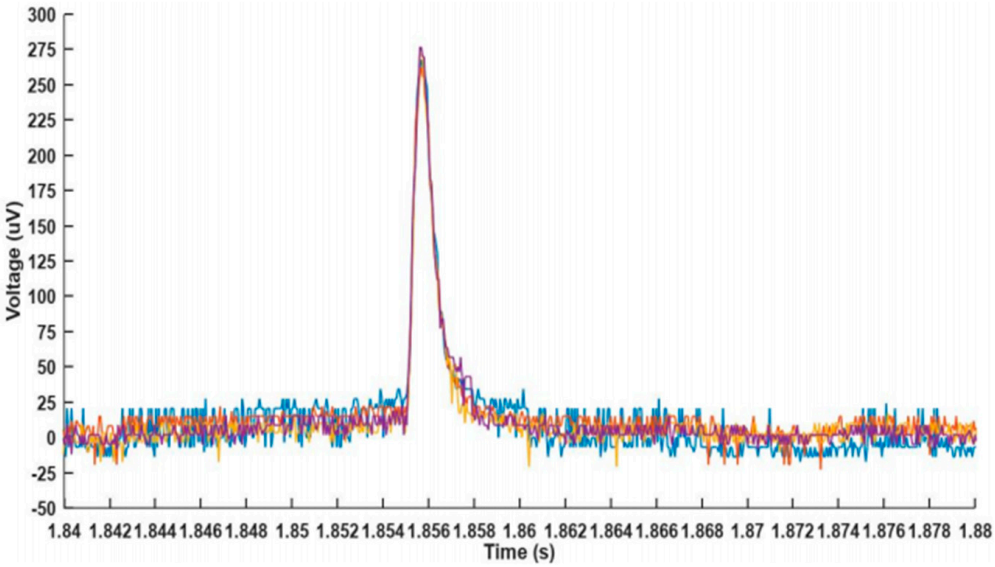


Figure 19. The spike shape of AP signal.

In Table 1, the performance of our design and other multi-channel neural recording systems are summarized. All of them have capacitively ac-coupled input, so their ability to reject electrode dc offset is rail-to-rail. The system records LFP and AP together, and external devices are able to separate them by an algorithm.

Table 1. Measured performance and comparison to prior art.

	This Work	[18]	[19]	[35]	[22]
Process (μm)	0.18	0.13	0.35	0.13	0.13
Channels	64	64	384	384	1024
Supply (V)	1.8	3–3.3	1.2/1.8	1.2	1.2
Power (μW)/Channel	130	110	49.06	95.1	46 [d]
RTI noise (μV_{rms})	5.5 (1–10 kHz) [a]	2.12 (300–3 kHz)	6.36 (300–10 kHz)	7.44 (300–10 kHz) 7.65 (0.5–1k)	7.5 (300–10 kHz) 12 (0.5–10k)
CMRR (dB)	69 (50 Hz)	70	60	75	>74 (50 Hz)
THD	0.53% (2 mVpp) [b]	1% [c]	0.4% (10 mVpp)	0.17% (10 mVpp)	0.71% (20 mVpp)
Gain	8–512	200–5000	50–2500	83.8	2–3000
HP corner (Hz)	0.1–20	0.02–750	0.53005001000	0.5	0.5300
LP corner (Hz)	6k–8k	6k–9.4k	1k–10k	10k	10k
ADC	10	10	10	14	10
Area (mm^2)/Channel	0.25	0.3	0.12	0.035	–

a: The RTI noise is related to the gain set by the system. When the gain is 256 or more, the RTI noise is 5.5 μV_{rms}; When the gain is 128, the RTI noise is 6.2 μV_{rms}; When the gain is 16, the RTI noise is 32 μV_{rms}. **b**: The gain was 512, and the tested signal frequency is 11 Hz. **c**: ref. [18] did not mention the amplitude of the test signal. **d**: This did not include the power consumption of the digital control circuit and the biasing circuit.

8. Conclusions

From system architecture to circuit design, this paper introduced a fully integrated 64-channel neural recording system, which can be used to record multiple LFP and AP signals simultaneously. Based on a SMIC 0.18 μm CMOS standard process, each channel of the chip occupies 0.25 mm^2, consumes an average power of 130 μW, and has an RTI noise of about 5.5 μV_{rms} from 1 Hz to 10 kHz. This 64-channel chip is our first research into multi-channel neural recording, and in future research, power consumption, noise, area, and reconfigurable functions will continue to be optimized. Additionally, system and package will be co-designed with the actual microelectrode array.

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