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Small Group Delay Variation and High Efficiency 3.1–10.6 GHz CMOS Power Amplifier for UWB Systems

Mayar Ali [1], Hesham F. A. Hamed [2,3] and Ghazal A. Fahmy [4,*]

[1] Higher Institute of Engineering and Technology, New Minia 11765, Egypt; mayar_elhamy@mhiet.edu.eg
[2] Faculty of Engineering, Minia University, Minia 61519, Egypt; hesham.fathy@eru.edu.eg
[3] Faculty of Engineering, Egyptian–Russian University, Cairo 11829, Egypt
[4] National Telecommunications Institute (NTI), Cairo 11768, Egypt
* Correspondence: ghazal.fahmy@nti.sci.eg

Abstract: A two-stage cascaded power amplifier (PA) employing a proposed Resistor-Capacitor (RC) interstage was provided and simulated. The current-reuse topology is employed at the first stage to lower the power consumption, while the RC interstage helps to enrich the gain flatness and the wideband matching. The shunt peaking topology in a common source configuration is adopted at the second stage to enhance the power gain. The postlayout simulation is performed using the TSMC 65 nm CMOS process operating in a frequency band of 3.1 GHz to 10.6 GHz. The postlayout simulation results indicate that a high flat gain of approximately 22.8 ± 1.2 dB, small group delay variation of ±50 ps, and good input and output matching of less than −10 dB are achieved over the desired working band. Moreover, a saturated output power of 10 dBm and maximum power-added efficiency (PAE) of 29.5% is achieved at 6 GHz. The proposed PA consumes the low power of 15.5 mW from 1.2 V supply voltage.

Keywords: power amplifier; ultra-wide band; low-power applications; wireless communication

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1. Introduction

Ultra-wideband (UWB) systems became more attractive in today's world owing to their capability to transmit data at a high rate and low power over a broad frequency. UWB systems are commonly used in short-distance wireless local area networks and be suitable for wireless personal area networks (WPAN) applications, sensor networks, and imaging systems [1]. The power amplifier is considered one of the most critical element in the UWB systems for being the major power consumption block among the system blocks. It is responsible for transmitting the RF signal to the required power level to meet the requirements of various applications. The design of the power amplifier needs to provide high power gain with broadband input and output matching, suitable efficiency, good linearity, low power consumption, and low group delay variations within the broad frequency spectrum. Therefore, the power amplifier design requires a better balance between efficiency, linearity, and gain requirement. The CMOS PAs for UWB applications presented in the literature adopt different techniques and operate over different frequency bands [2–14].

The distributed amplifier (DA) topology provides wideband matching and good gain flatness but consumes more power and a large chip of area based on the distribution of several amplifying stages and transmission line configuration linked between them [2]. However, the DA in [3] achieved not only a high flat gain over the bandwidth (BW) of operation, but also achieved 25 mW low power consumption by employing the technique of tapered transmission line. The resistive shunt feedback topology adopted in [4] attained a flat gain with wide bandwidth and low group delay variation of ±18.3 ps; in addition, it consumed low power of 19 mW. [5] adopted both the active RC feedback for linearity enhancement and bandwidth extension and the double resonance network for flat gain

and good broadband matching. The RLC matching topology introduced in [6] offered a wideband matching with low power consumption, but the design provided a low average power gain of 10 dB. [7] adopted the shunt peaking topology for the first and second stages to realize the high flat gain, good linearity, and group delay variation, whereas it adopted the shunt resistive feedback for the first stage for wideband input matching. The inductive degeneration topology demonstrated in [8,9] helped to attain a high flat gain with high power-added efficiency, but the matching was not as impactful as with resistive feedback topology. The common gate amplifier combined with RC-shunt feedback and inductive degeneration was adopted in [10] to realize a good matching with a high flat gain and good linearity. The interstage transformer topology [11] provided broadband linearity and consumed low power, but the gain was limited. Stagger-tuning topology [12] exposed three-stage amplifiers; each stage was tuned to a different frequency for broadband operation and flatten gain, but that caused the consumption of the high power. Current-reuse topology is adopted in the UWB-PA design to attain a low power consumption, better isolation, low group delay, and enhance gain flatness as in [13] but, this topology introduced poor matching and low power gain. [14] improved the broadband matching by employing a common gate amplifier combined with the current reused topology for the input stage. Furthermore, Designing UWB-PA that covers the whole band from 3.1 to 10.6 GHz and satisfies all the ultra-wideband specifications is a challenge. In this paper, a low group-delay variation, a well-matched CMOS PA, covering the band of 3.1 to 10.6 GHz, with a low power consumption and a high power-added efficiency (PAE) for UWB systems is designed and simulated using the 65 nm TSMC CMOS process. Figure 1 shows the block diagram of the proposed UWB-PA. The first stage is a current reuse topology for a low power consumption; the interstage employs the proposed *RC* circuit for wideband matching and gain flatness; and the second power stage is a shunt peaking common source (CS) amplifier that maximizes the gain and PAE. The remainder of the paper is arranged as follows: Section 2 discusses the principle and analysis of the suggested UWB power amplifier design. Section 3 illustrates the simulation results and the comparison table of recently published *PAs*. Finally, Section 4 presents the paper's conclusion.

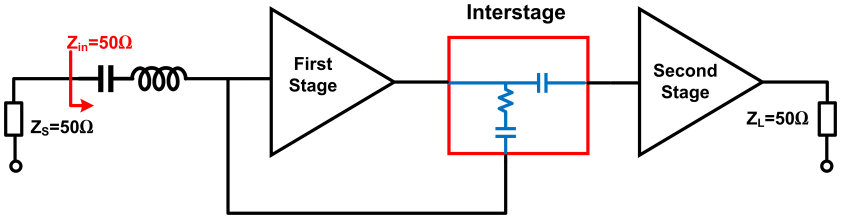

Figure 1. Block diagram of suggested ultra-wideband (UWB) power amplifier.

2. Design Methodology and Circuit Analysis

The proposed UWB-PA design and its small signal-equivalent circuit are shown in Figures 2 and 3, respectively. The design adopts two-stage cascaded configuration of an amplifier with a proposed RC interstage for acquiring a sufficient power gain and wide bandwidth. The first stage involves the current-reuse cascade common source technique, and the second stage adopts the shunt peaking topology. The current-reuse structure has a power saving advantage compared to that of a cascade amplifier because the current of the transistor M_1 is reused by the transistor M_2, so the gain is boosted without any additional power consumption. Based on the current reuse structure, the amplified signal at the drain of M_1 is passed to the gate of M_2 through the low impedance path formed by the series resonance of (L_3 and C_3), in addition to the parasitic capacitance of the gate of M_2. A large impedance of L_{D1} and a bypass capacitor C_{b2} block any RF signal from passing to the source of M_2 over the working frequency band. The current reuse structure suffers from the increment of parasitic capacitance, which degrades the PA gain performance, and therefore the two stages of amplifier are employed to reach a sufficient power gain while maintaining a low power consumption. The gain flatness can be improved by connecting

the proposed RC interstage with R_f, C_f and C_{INT} between the first stage and the second stage. The feedback, R_f and C_f, can be optimized so that a good input match, broadband flatten gain, and low noise figure (NF) can be achieved simultaneously. The choice of the feedback resistor determines the operating bandwidth. A small value of the feedback resistor increases the operating bandwidth but decreases the gain. The optimum value of the resistor R_f should be carefully chosen to meet the gain and matching demands. The effect of R_f on the amplifier gain flatness is indicated in Figure 4. The second stage is a shunt peaking CS amplifier to enhance the gain, maximize the PAE, and realize the small group delay variation. The M_3 transistor size should be large for enhancing the output power. L_{D3} has peaking characteristics, which can widen the bandwidth and reduce the return loss of the output. LC networks of (L_1 and C_1) and (L_{OUT} and C_{OUT}) are employed to improve the broadband input and output matching, respectively, over the entire bandwidth. Bypass capacitors C_{b1} to C_{b5} approximate a short circuit at high frequency and reject the effect of noise from the power supply. The resistor R_2 is used to supply a bias voltage for the transistor M_2. The biasing circuit formed by M_{b1}, R_{b1},and R_{b2} to bias M_1 transistor and also M_{b2}, R_{b3}, and R_{b4} to bias M_3 transistor. Table 1 presents the size of the PA design parameters.

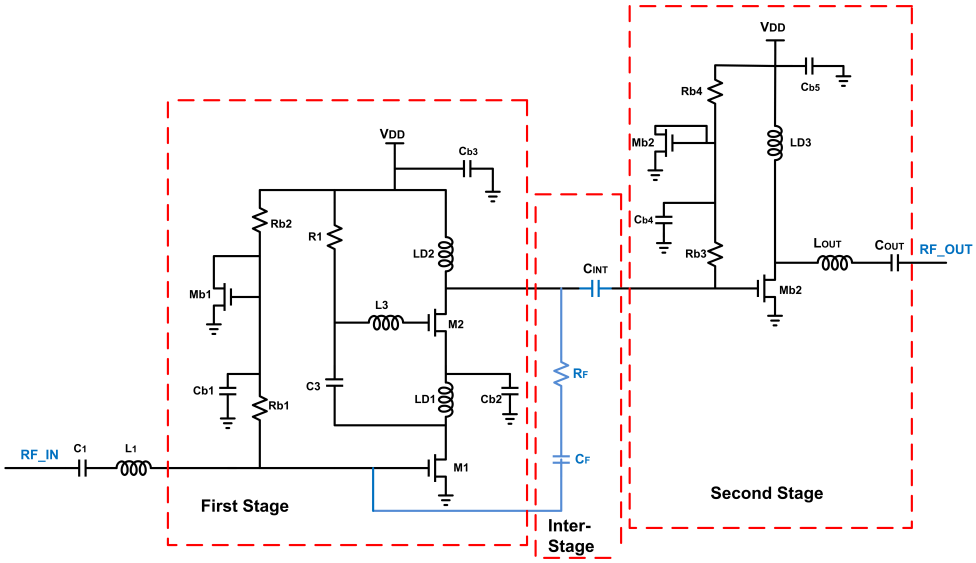

Figure 2. Schematic of proposed UWB power amplifier.

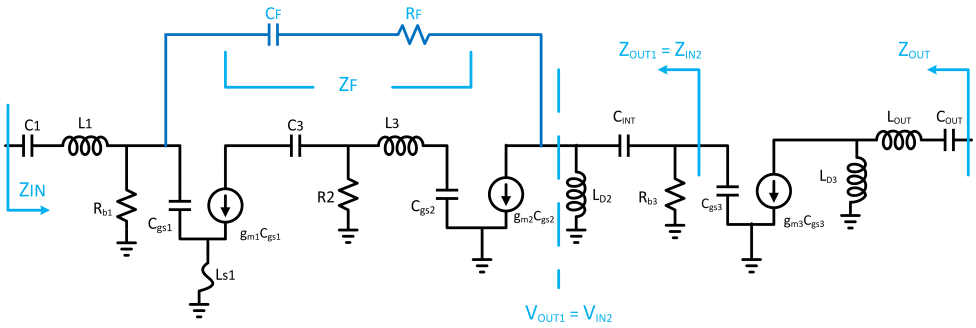

Figure 3. Small signal-equivalent circuit model.

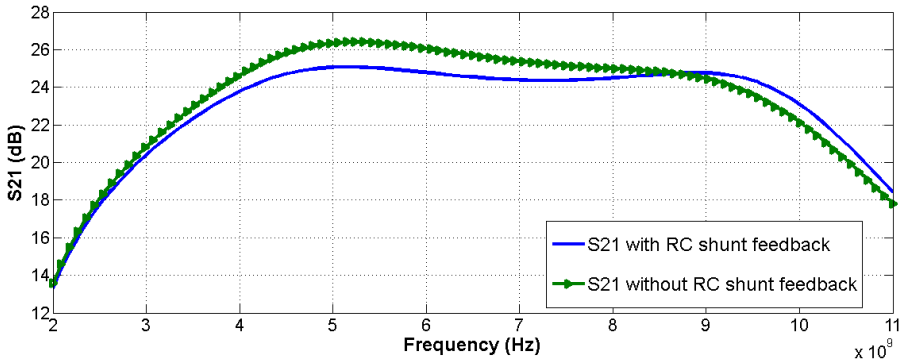

Figure 4. Simulated S21 with and without feedback resistor.

Table 1. Design parameter values of proposed UWB-PA.

Design Parameter	Values	Design Parameter	Values
M_1	L = 0.06 µm, W = 100 µm	L_{D1}	1.2 nH
M_2	L = 0.06 µm, W = 100 µm	L_{D2}	3.7 nH
M_3	L = 0.06 µm, W = 100 µm	L_{D3}	3.7 nH
C_1	2 pF	L_{OUT}	610 pH
C_3	50 fF	R_{b1}	200 Ω
C_{INT}	1 pF	R_{b2}	400 Ω
C_F	500 fF	R_{b3}	1 KΩ
C_{OUT}	1 pF	R_{b4}	400 Ω
L_1	1.8 nH	R_F	3.9 KΩ
M_{b1}/M_{b2}	L = 0.06 µm, W = 60 µm	L_3	186 pH

2.1. Input Matching

Wideband-input impedance matching is required to enhance the accessible power from the source to the *PA* to boost the UWB-PA PAE. The DC-blocking capacitor C_1 is a part of the input matching circuit with the inductor L_1. The resistor R_f and the capacitor C_f helps in attaining wideband input matching. The small-signal equivalent circuit for the input impedance is shown in Figure 5. For simplicity, by neglecting the miller effect of the gate to drain capacitance C_{gd}, the input impedance Z_{in} is deduced as follows:

$$Z_{in} = \frac{1}{SC_1} + SL_1 + [R_{b1}//Z_f// \left(\frac{1}{SC_{gs1}} + \omega_{t1}L_{s1} + SL_1\right)] \quad (1)$$

$$\omega_{t1} = \frac{g_{m1}}{C_{gs1}}$$

ω_{t1} is the current gain cutoff frequency, g_{m1} is M1 transistor transconductance, and C_{gs1} is the M1 transistor's gate to source capacitance.

$$Z_{in} \cong \frac{1}{SC_1} + SL_1 + \left(Z_f//R_{b1}\right) \quad (2)$$

$$Z_{in} = \frac{S^2L_1C_1 + SC_1(Z_f//R_{b1}) + 1}{SC_1} \quad (3)$$

where;

$$Z_f = \frac{R_f + 1/SC_f}{1 + A_1} \quad (4)$$

A_{v1} is the voltage gain of the first stage. From Equation (3), the biasing resistor R_{b1}, network (L_1 and C_1), and the feedback impedance Z_f were more carefully chosen, as smaller Z_f provides better matching but degrades the amplifier gain.

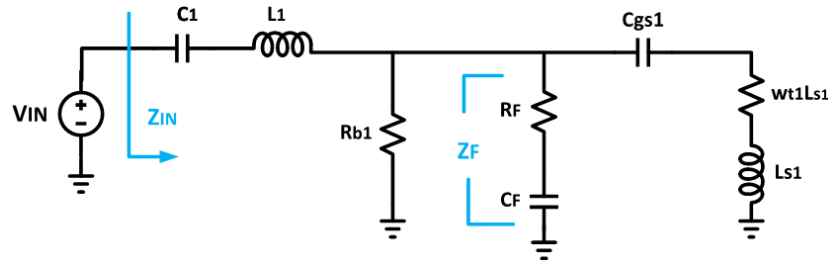

Figure 5. Input impedance equivalent circuit.

2.2. Interstage Impedance Matching

As presented in Figure 1, The RC circuit interstage matching is recommended in this work instead of the conventional LC matching circuit. The circuit C_{INT}, R_F, and C_F are optimized for maximizing the PAE that ensures the optimal power transfer through the amplifier stages. Figure 6 presents the small-signal equivalent circuit for the interstage impedance transformer. As outlined from Equation (6), R_{b3}, Z_f, C_{INT}, and L_{D2} are carefully optimized and chosen for a good impedance matching and high PAE, taking into account the gain flatness and group delay variation.

$$Z_{out1} = Z_{in2} = R_{b3} // [\frac{1}{SC_{INT}} + (SL_{D2} // Z_f)] \tag{5}$$

$$Z_{out1} = R_{b3} // \frac{S^2 Z_f L_{D2} C_{INT} + SL_{D2} + Z_f}{S^2 L_{D2} C_{INT} + SC_{INT} Z_f} \tag{6}$$

where;

$$Z_f = \frac{R_f + 1/SC_f}{1 + 1/A_1} \tag{7}$$

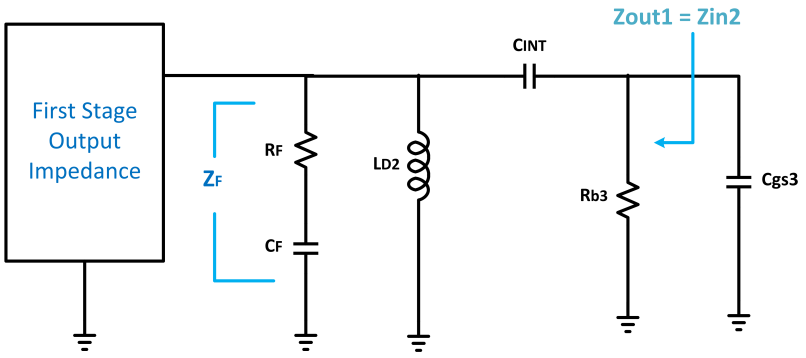

Figure 6. Interstage impedance matching network transform equivalent circuit.

2.3. Output Matching

Figure 7 presents the small-signal equivalent circuit for the output impedance. The capacitor C_{OUT} along with the inductor L_2, and L_{D3} are optimized for enhancing the *PAE* and achieving a small-group delay variation. The equivalent output impedance is outlined by:

$$Z_{OUT} = SL_{D3} + \frac{1}{SC_{OUT}} + SL_{OUT} \tag{8}$$

$$Z_{OUT} = \frac{S^2 L_{D3} C_{OUT} + S^2 L_{OUT} C_{OUT} + 1}{SC_{OUT}} \tag{9}$$

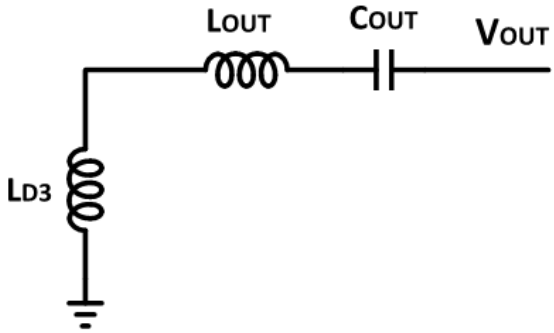

Figure 7. Output impedance equivalent circuit.

3. Simulation Results and Discussions

The proposed UWB-PA is simulated with cadence simulator in TSMC 65 nm CMOS process with 1.2 V supply voltage, consuming only the 15.5 mW DC power. Figure 8 shows the *S*-parameters postlayout simulation, where the input (S_{11}) and the output (S_{22}) return loss of below −7 dB and −10 dB, respectively, are achieved, and an average high flat power gain (S_{21}) of 22.8 ± 1.2 dB is realized over the full frequency band of 3.1 to 10.6 GHz. Figure 9 shows the frequency behavior of the normalized input and output matching (S_{11} and S_{22}) on Smith chart, while Figure 10 shows the impedance curves of both input and output matching networks. The optimal input and output impedance are around the 50 Ohms through the entire bandwidth.

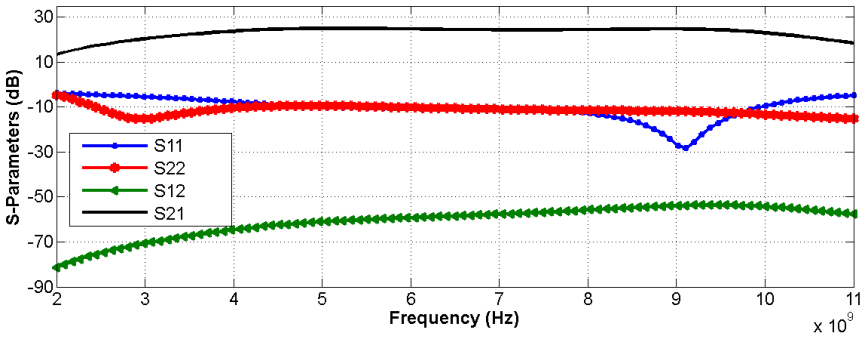

Figure 8. Postlayout simulation of s-parameters (S_{11}), (S_{22}) ,(S_{12}), and (S_{21}).

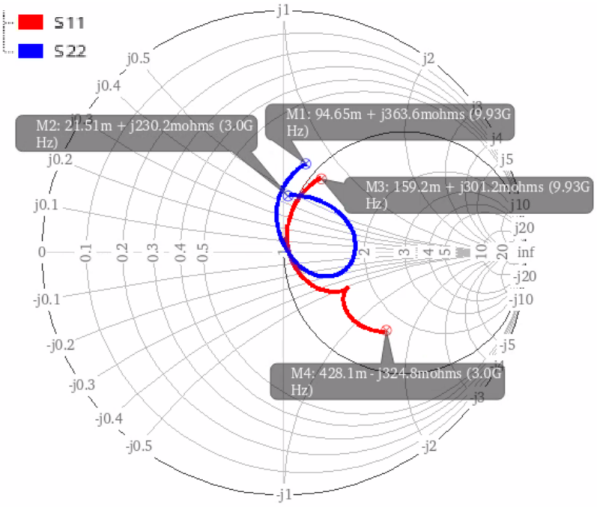

Figure 9. Frequency behavior of (S_{11}) and (S_{22}) on Smith chart.

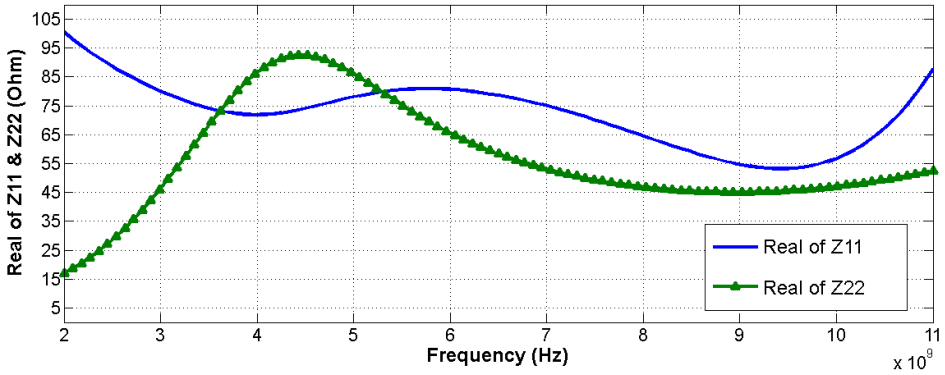

Figure 10. Impedance curves of input and output matching network (Z11 and Z22).

The PAE is a key parameter to measure the PA performance and is enhanced by improving the input, output, and interstage matching. Figure 11 demonstrates that the proposed UWB-PA attains the maximum PAE of 29.5% at 6 GHz, 26% at 8 GHz, and 22.6% at 10 GHz. By using Figure 12, to achieve a higher PAE, the values of R_f, C_{INT}, and R_{b3} are reiterated several times and finally are selected to be 3.9 KΩ, 1 pF, and 1 KΩ, respectively. The proposed *PA* attains the saturated output power P_{OUT} of about 10 dB at 6 GHz, 9.7 dBm at 8 GHz, and 8.9 dBm at 10 GHz. It also achieves 1-dB output compression point (P_{1dB}) of 6.8 dBm at 6 GHz, 5.7 dBm at 8 GHz, and 4.6 dBm at 10 GHz, respectively as displayed in Figure 13.

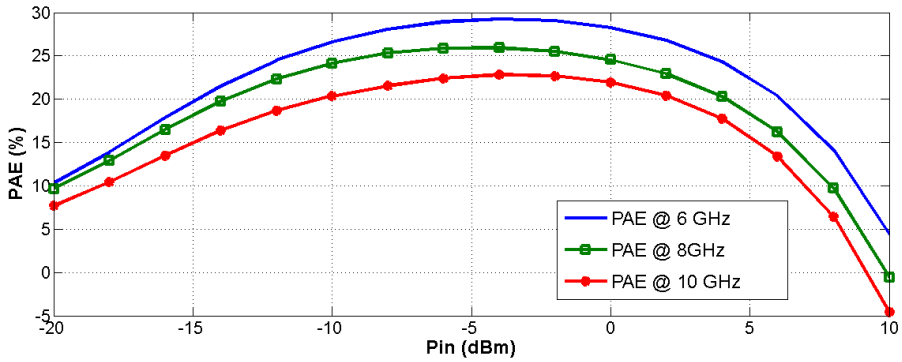

Figure 11. Simulated *PAE* versus P_{IN} at different frequencies within mentioned band.

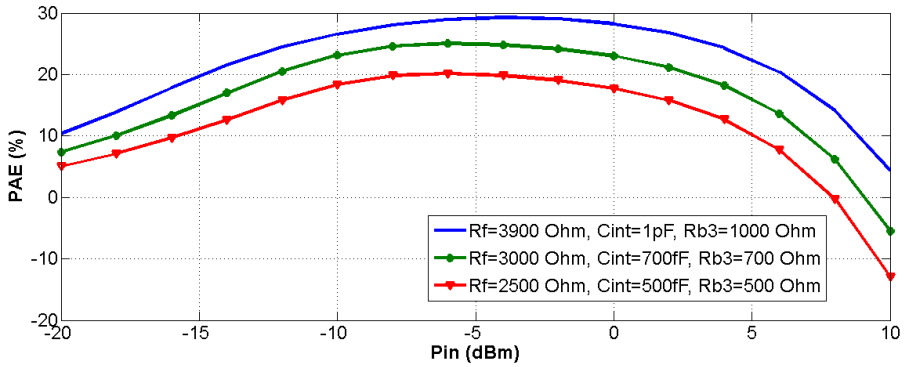

Figure 12. Effect of resistors R_f and R_{b3} and capacitor C_{INT} on PAE.

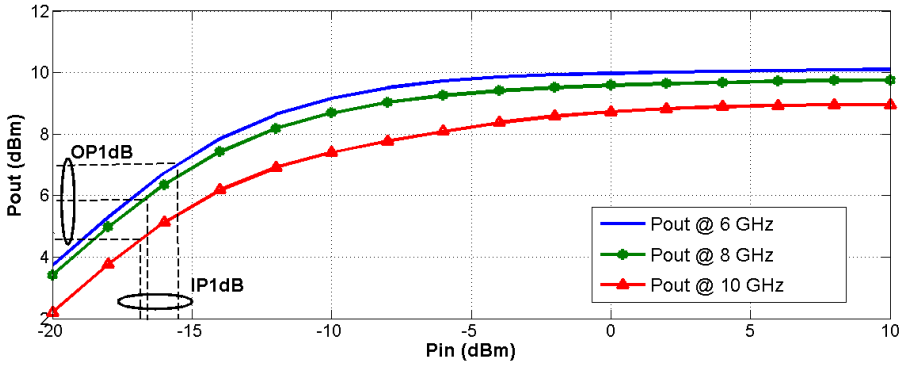

Figure 13. P_{OUT} versus P_{IN} at different frequencies within desired band.

One of the major criteria used to measure the amplifier phase nonlinearity is the group delay (GD). In wideband communication, the GD variations should be kept low for better phase linearity. Minimizing the variations in the frequency domain saves the time domain amplified signal from distortion; besides, large variations GD implicate more phase distortion and the output does not retain its original input. Small variations of ±50 ps are achieved over the full desired band being indicated from the postlayout simulation, as shown in Figure 14, which indicates that all the frequencies will be delayed by an equal amount.

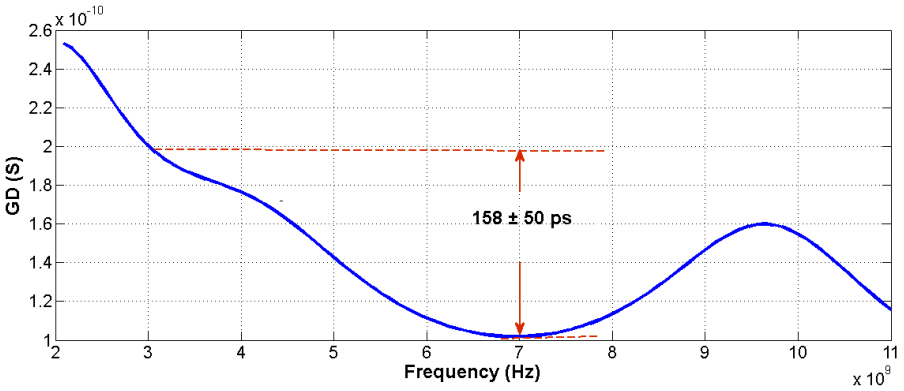

Figure 14. Postlayout simulation of group delay.

The Rollet's condition, also known as the $Kf - \Delta$ test, is used to determine the stability of the proposed power amplifier. A circuit will be unconditionally stable if $Kf > 1$ and Δ less than 1 are satisfied by the $Kf - \Delta$ simulation test [15]. Kf and Δ of the PA are represented in Figure 15, and Kf more than one and Δ less than 1 are attained for the complete range, thereby ensuring that the PA is unconditionally stable. Figure 16 indicates the NF of less than 7 dB along with the full band. Noise figure reduction is a very good achievement, as it implies the good performance of the UWB-PA. Figure 17 presents the layout of the proposed PA, which occupies a chip area of 1300 um × 900 um. Table 2 shows the post-layout simulation results of the proposed UWB- PA and compares its performance with that of recently published UWB- PAs research. The proposed PA consumes the lowest power and has a small GD variation under the full band while attaining good gain flattens, high PAE, and good matching behavior.

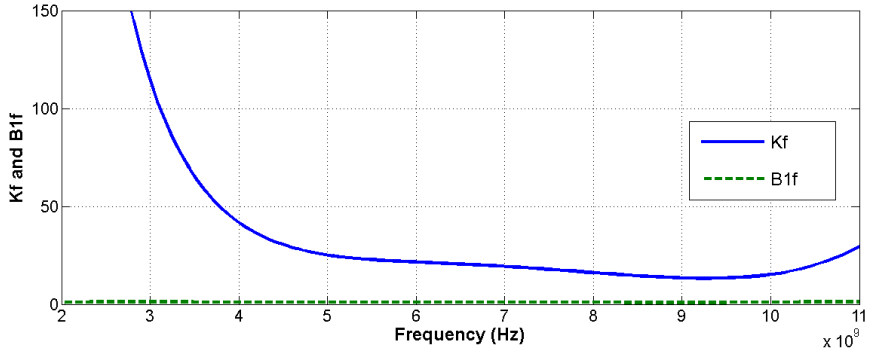

Figure 15. Kf and $\Delta(B1f)$ simulation results.

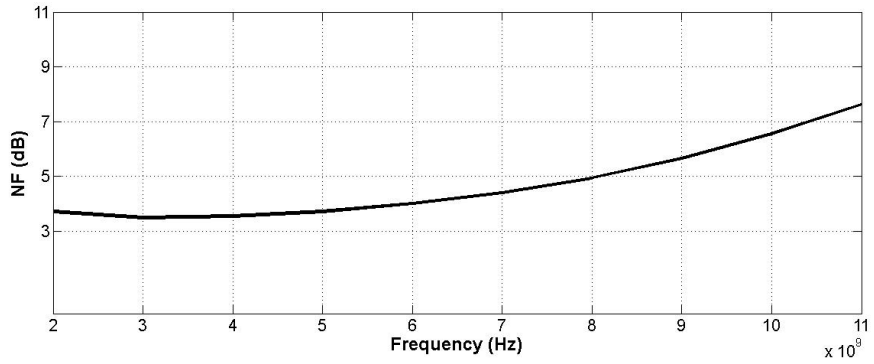

Figure 16. Noise floor (NF) simulation result.

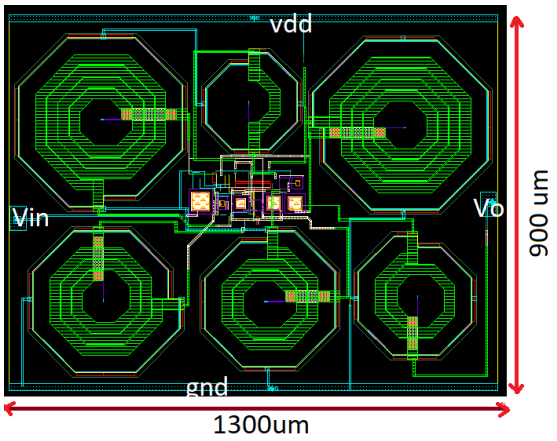

Figure 17. Layout of proposed PA.

Table 2. Postlayout simulation results of proposed UWB-PA in comparison with that of other published CMOS UWB-PAs.

Ref.	[4] *	[16] *	[17] *	[18] *	[19] **	This Work *
CMOS Technology (nm)	180	180	180	130	65	65
frequency (GHz)	3.1–10.6	3.1–10.6	3–5	3.1–5.1	3–10	3.1–10.6
Gain (dB)	12.4 ± 1.1	12.5 ± 1	16.2	20.3 ± 0.8	12.65 ± 1.25	22.8 ± 1.2
S11 (dB)	<-8.6	<-4.5	<-6	<-1.5	<-10	<-7
S22 (dB)	<-8.6	<-8.5	<-0.5	<-6	<-10	<-10
Dissipated Power (mW)	19	36	25	27.3	N/A	15.5
GD (ps)	± 18.3	± 50	± 75	± 121.3	± 21.5	± 50
PAE (%)	N/A	32.5	47	N/A	20.15 ± 7.55	29.5@6 GHz
OP1dB (dBm)	N/A	11	10.1	N/A	16 ± 2.1	6.8
Area (mm^2)	0.69	0.55	N/A	N/A	0.498	1.17

* Simulated. ** Measured.

4. Conclusions

In this work, A 3.1 to 10.6 GHz UWB 65 nm CMOS PA with the RC interstage is proposed to enhance the gain flatness and wideband matching. The proposed amplifier adopts the current reuse topology at the first stage for low power consumption and the shunt peaking topology at the second stage for gain and PAE enhancement. The postlayout simulation results show that the proposed PA consumes the low power of 15.5 mW at 1.2 V supply voltage. In addition, it achieves a small group delay variation of ±50 ps with a good flatten power gain of 22.8 ± 1.2 dB across the whole frequency band. Moreover, maximum PAE of 29.5% is attained.

Author Contributions: Conceptualization, M.A. and G.A.F.; Formal analysis, M.A., H.F.A.H. and G.A.F.; Writing—original draft, M.A. and G.A.F.; Writing—review and editing, H.F.A.H. and G.A.F. All authors have read and agreed to the published version of the manuscript.

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