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A Flash Frequency Tuning Technique for SC-Based mm Wave VCOs

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Abstract: This paper presents a flash frequency tuning technique for switched-capacitor-based, voltage-controlled oscillators operating at mm wave frequencies. The proposed strategy exploits a capacitor array and a small varactor for coarse and fine tuning, respectively, which are simultaneously operated thanks to a flash A/D-based control circuit. This avoids additional delay in the frequency calibration, thus enabling very fast-frequency locking operation. The VCO was fabricated in a 28 nm FD-SOI CMOS technology and provides an oscillation frequency around 39 GHz with an overall tuning range of 3.3 GHz. The circuit dissipates 8.4 mW from a power supply as low as 0.7 V, while occupying a silicon area of 210 µm × 150 µm.

Keywords: switched-capacitor array; VCO; wireless communications; radar sensors; mm wave PLL; FD-SOI CMOS technology

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1. Introduction

Mm wave phase-locked loops (PLL) are highly demanded in a wide range of applications, such as medical imaging [1–3], wireless communications (e.g., WLAN [4–6], 5G generation cellular networks [7,8], etc.) and automotive radar sensors [9–13]. Whatever the addressed application, a mm wave PLL must provide a proper tuning range (TR) to cover the desired operating band. Moreover, a fast settling time must also be achieved to meet the high-speed requirements of modern communication systems that claim data transfer with low latency along with bit rates up to Gbps [14].

The key building block of a PLL is the voltage-controlled oscillator (VCO), which sets the tuning range and mainly contributes to the PLL's overall performance.

Currently, nanometer CMOS technologies are the best choice for the implementation of mm wave circuits, since they are able to meet the required performance while providing system-on-chip (SoC) solutions that guarantee compactness and a low cost. However, the technology scaling leads to a substantial reduction in the supply voltage, which is advantageous for battery-operated devices [15] since it lowers power consumption, but it affects the circuit voltage swing, thus giving rise to several drawbacks. Specifically, a lower power supply reduces both the VCO control voltage swing and the oscillation amplitude, making the trade-off between tuning range and phase noise (PN) very critical in mm wave applications.

Meeting the tuning range requirement in mm wave VCOs with low power supplies is not a trivial task. Indeed, the lower the power supply is the larger the varactor size should be to preserve tuning range. However, a large varactor leads to heavy losses, which affect phase noise. Moreover, varactor parasitic capacitances greatly increase their contribution to the overall tank capacitor, thus still reducing tuning range.

To overcome such limitations, arrays of switched capacitors (SCs) along with fully digital or analog/digital control circuits are employed for a coarse frequency calibration [16–21], leaving the fine tuning to a small varactor. This approach has the advantage of avoiding large area varactors to cover the overall tuning range with the double benefit of increasing the tank Q-factor and reducing parasitic capacitances. Indeed, the capacitors usually adopted in an SC array exhibit lower losses and parasitic capacitances than the varactor counterpart.

Unfortunately, such techniques are responsible for an additional delay during calibration, which increases the PLL settling time, thus affecting speed performance [17]. Figure 1 shows a typical settling time, τ_{PLL}, of a PLL exploiting an SC-based tuning approach. It is given by the sum of the times for coarse, τ_{CT}, and fine, τ_{FT}, tuning phases, which have to be sequentially performed. The solution in [20] uses an SC array with a $\Delta\Sigma$ converter that combines coarse- and fine-tuning operations in a single time slot (step). However, 1-MHz RC filters are needed, which inherently lead to low operation speed.

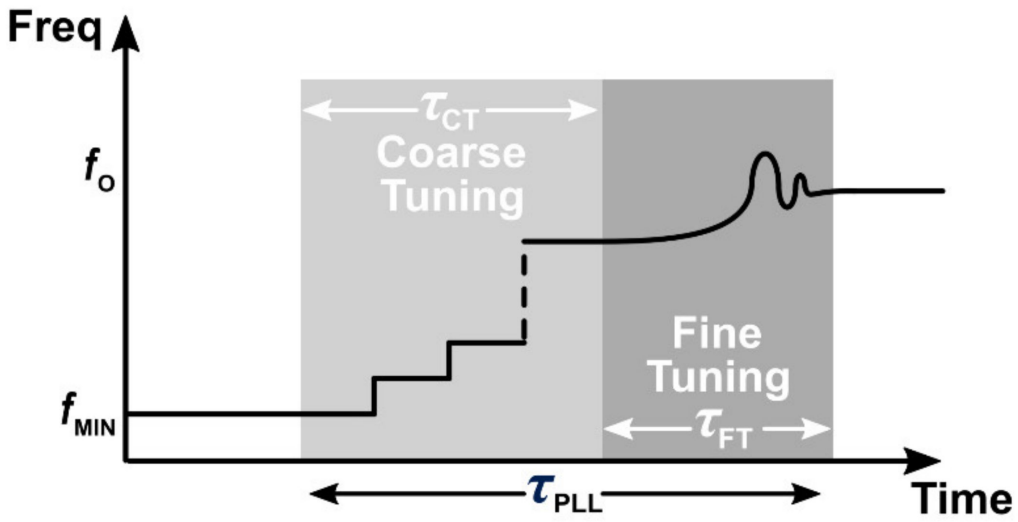


Figure 1. Typical transient response of an SC-based PLL.

In this paper, a novel tuning strategy for SC-based, voltage-controlled oscillators is presented, which overcomes the tuning delay limitations of state-of-the-art solutions, thus achieving high-speed frequency locking. The proposed technique uses a flash A/D-based control circuit [22], which allows coarse- and fine-tuning operations to be simultaneously performed. To demonstrate the effectiveness of the proposed tuning strategy, an SC-based mm wave VCO was designed, which provides a wide tuning range while operating at a power supply as low as 0.7 V.

The paper is organized as follows. Section 2 deals with the description of the VCO topology and tuning strategy. Experimental results are presented in Section 3, which also includes a comparison with the state of the art. Finally, conclusions are drawn in Section 4.

2. Circuit Description

A simplified schematic of the designed VCO is shown in Figure 2a. It is based on a NMOS topology with transformer-coupled tank. Specifically, the tank is made up of the secondary coil of transformer T_1, a small accumulation MOS varactor, C_V, and an SC array. The control voltage, V_C, is applied to the center tap of the tank inductor to properly drive the varactors while preventing power supply noise from affecting the phase noise performance. A 3-D view of the VCO tank transformer along with the adopted metal stack and its main parameters are shown in Figure 2b.

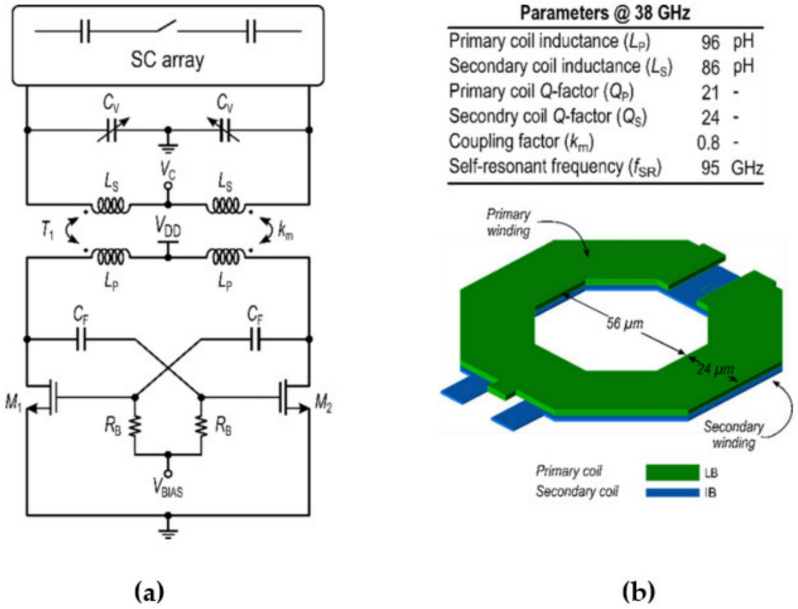


Figure 2. Voltage-controlled oscillator: (**a**) schematic, (**b**) 3-D view of transformer T_1 with the adopted metal stack and its main parameters.

The proposed tuning circuit is shown in Figure 3. It is made up of a flash A/D converter driving a capacitor array for coarse frequency tuning and a small-area varactor, C_V, for fine tuning. The converter in this implementation uses a set of 11 comparators with hysteresis and a resistor string. The latter sets the comparator threshold voltages that in turn define the segments of the coarse conversion, which are properly overlapped to reduce the varactor size. As far as the capacitor array is concerned, it is made up of high-Q MOM capacitors, C, connected to MOS switches that are implemented as shown in Figure 3 [21]. Each element of the SC array is driven by a comparator and provides an equivalent unit capacitor, C_U, equal to $C/2$. Assuming that the high and low threshold voltages of the k-th comparator are $V_{Tk,H}$ and $V_{Tk,L}$, respectively, the varactor is sized to guarantee the following condition

$$C_V(V_{Tk,H}) - C_V(V_{Tk,L}) > C_U \tag{1}$$

that is required to achieve fine tuning within the coarse-tuning segments. Specifically, the maximum variation of the varactor capacitance within the comparator hysteresis window was set 10% larger than C_U to compensate for process tolerances and temperature variations. For the sake of completeness, the simulated varactor response as a function of the control voltage is shown in Figure 4.

The tuning circuit works as follows. As soon as control voltage V_C reaches the value of threshold voltage $V_{Tk,H}$, the k-th comparator switches high, and a further unit capacitor is placed in parallel to the varactor, thus increasing the overall tank capacitor. After comparator switching, control voltage V_C will increase toward $V_{Tk+1,H}$ or will decrease toward $V_{Tk,L}$, depending on the PLL output frequency, f_O. Specifically, if f_O after switching is, for instance, higher than the value imposed by the PLL reference and divider, V_C will go higher than $V_{Tk,H}$, and if it reaches $V_{Tk+1,H}$ a further unit capacitor will be added in parallel to the varactor. If instead after switching of the k-th comparator f_O is close to its steady-state value, this means that $V_{Tk,H}$ is the coarse conversion of V_C, which will settle around $V_{Tk,H}$ according to the condition

$$V_{Tk,L} < V_C < V_{Tk+1,H} \tag{2}$$

thanks to the varactor that performs the fine frequency tuning. It is worth mentioning that the comparator hysteresis along with the condition in (1) are key concepts for the

stability in this tuning strategy. Without hysteresis, control voltage V_C and hence the PLL output frequency would oscillate around the steady-state value defined by the coarse conversion. Actually, hysteresis enables the flash A/D converter and allows fast, discrete coarse conversion and continuous fine conversion to be simultaneously achieved without any additional delay.

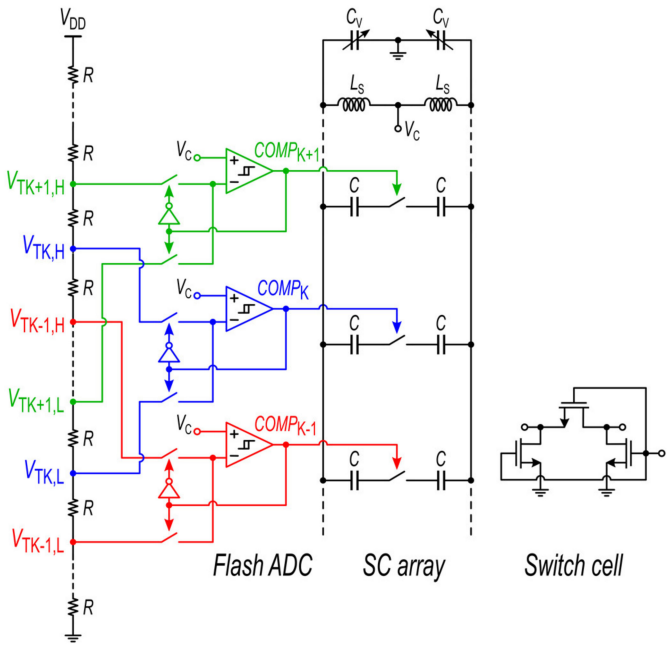


Figure 3. Simplified schematic of the proposed tuning circuit.

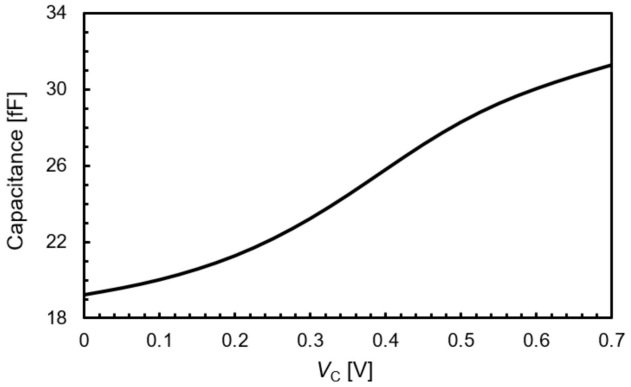


Figure 4. Simulated varactor response as a function of the control voltage.

3. Experimental Results

The VCO was fabricated in a 28 nm FD-SOI CMOS technology by STMicroelectronics, which provides a very fast active device with f_T and f_{MAX} up to 300 GHz [23] and a standard back end of line (BEOL). The die microphotograph is shown in Figure 5. The VCO core silicon area is 210 µm × 150 µm.

A block diagram and a photograph of the adopted measurement setup are shown in Figure 6a,b, respectively. The VCO was embedded within an on-chip PLL designed for testing purposes, which uses an off-chip second-order low-pass filter (LPF). Integrated switches SW_1 and SW_2 were externally driven to enable/disable the SC array. The integrated PLL exploits a frequency divider, N, by 384, which leads to a reference frequency of around 100 MHz. The measurement setup includes a spectrum analyzer and a digital oscilloscope for spectrum and transient measurements, respectively. A signal generator

was also used to generate the PLL reference signal. Measurements were performed at 0.7-V power supply.

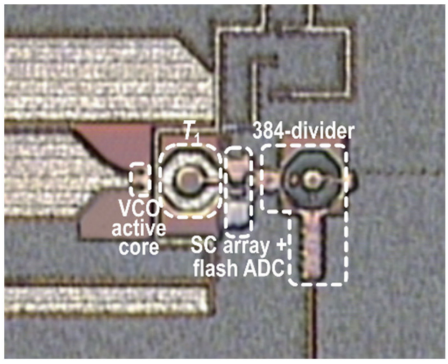
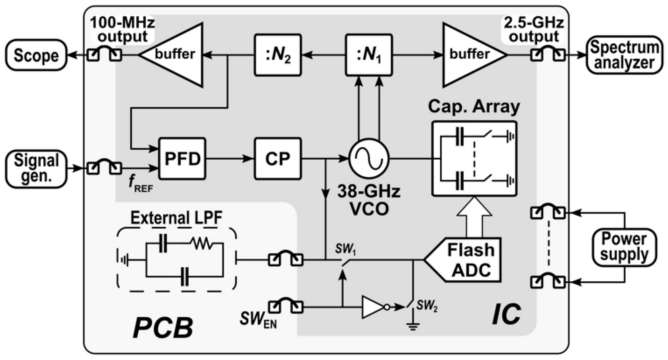
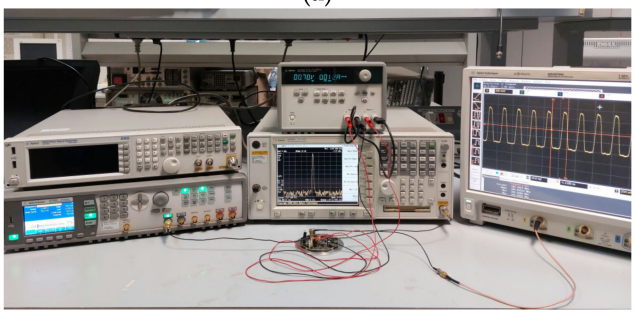


Figure 5. Die microphotograph.



(**a**)



(**b**)

Figure 6. Adopted measurement setup: (**a**) block diagram, (**b**) photograph.

Figure 7 depicts the measured VCO tuning range. The oscillation frequency ranges from 37.4 to 40.7 GHz when varactor control voltage V_C sweeps from 0 to 0.7 V. For the sake of completeness, the tuning range provided by the varactor (i.e., with the tuning array disabled) is also reported. The VCO tuning curve is set by the varactor as long as the capacitor array is not operated. This is true for a control voltage that is lower than the high threshold voltage, $V_{T1,H}$, of the first comparator, which was set to about 220 mV. Indeed, Figure 7 shows that for low control voltages the overall tuning curve and the varactor tuning curve are overlapped. Once the control voltage overcomes $V_{T1,H}$, the first switched capacitor is inserted, and fine and coarse tuning are simultaneously performed. As is apparent, the varactor performs a small fraction of the overall tuning range, which instead is mainly provided by the SC array.

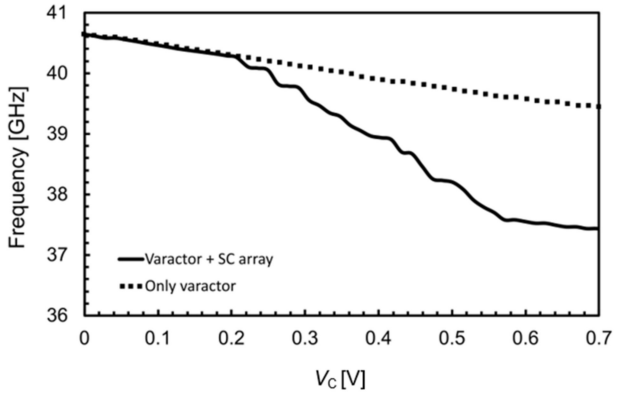


Figure 7. Measured tuning range.

Figure 8 shows the VCO frequency transient response. The PLL bandwidth was set to 5 MHz, and a frequency step from 97.6 MHz to 105.6 MHz was applied to the PLL frequency reference. Under these conditions, the VCO frequency settles in about 0.2 µs, which is the overall PLL locking time including both array and varactor operations. For the sake of clarity, the response to a frequency step was carried out setting the PLL bandwidth to a low value (i.e., 20 kHz) to better show the staircase frequency transient response due to the switched capacitor array. Figure 9 displays the VCO output frequency, f_{VCO}, the input frequency step, f_{REF}, normalized to f_{VCO} (i.e., $f_{\mathrm{REF}} \times N$), and the control voltage, V_C. As is apparent, the transient response is mainly set by the slew rate due to the high dominant-pole capacitor in the loop filter. Note that the slope in each step is the effect of the varactor on the frequency variation within the hysteresis window. It demonstrates that coarse and fine tuning can be operated at the same time without any delay.

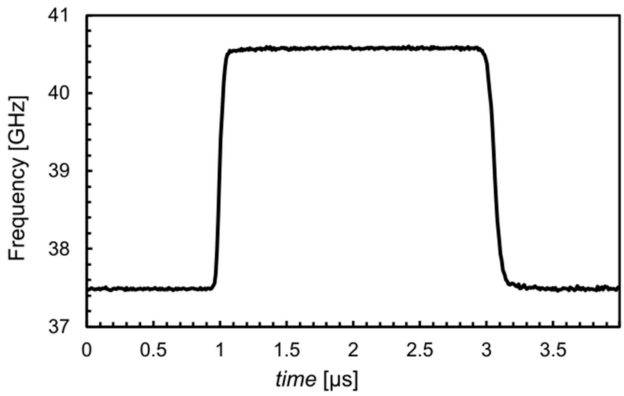


Figure 8. Transient response of the VCO oscillation frequency with 5-MHz PLL bandwidth.

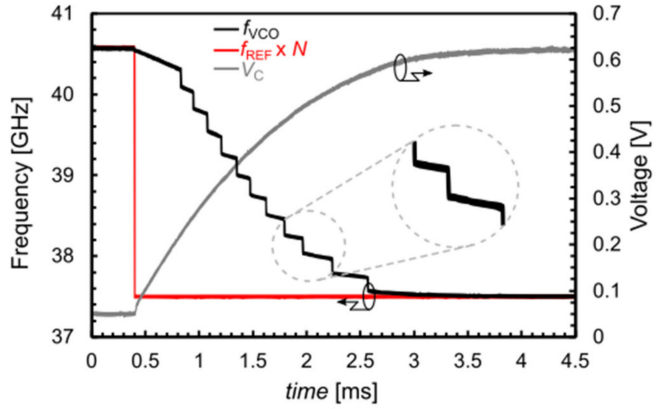


Figure 9. Transient response of the VCO oscillation frequency with 20-kHz PLL bandwidth.

Figure 10 depicts the measured PLL output frequency for a frequency-modulated reference signal with a triangular shape. Specifically, a period of 40 µs and a 3-GHz frequency variation was set. As is apparent, continuous-time operation with variable PLL reference frequency is possible. Such a dynamic response is enabled by the proposed tuning strategy, which avoids any tuning delay.

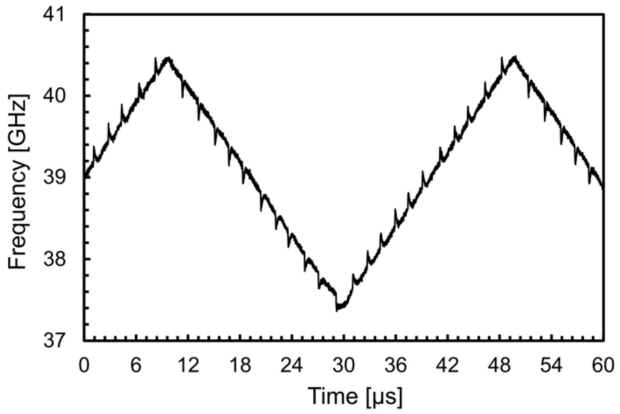


Figure 10. Measured dynamic frequency locking with a triangular reference frequency.

For the sake of completeness, the phase noise of the VCO was also measured by setting the PLL bandwidth as low as 20 kHz to make the VCO noise contribution dominant at the PLL output. The measurement was carried out by taking the noise at the 2.5-GHz output of the loop divider. This noise was about −118 dBc/Hz at 1-MHz offset frequency, as shown in Figure 11. The phase noise evaluated at 39 GHz was about equal to −94 dBc/Hz.

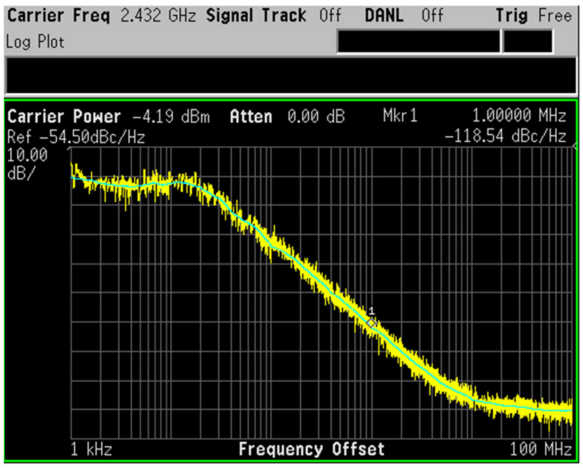


Figure 11. Measured phase noise at 2.5-GHz carrier frequency.

The overall measured performance is summarized and compared with recent state-of-the-art mm wave CMOS VCOs in Table 1. The proposed solution does not suffer from the additional delay of conventional coarse-tuning techniques based on SC arrays. Moreover, the VCO exhibits a phase noise and tuning range that are similar to state-of-the-art, SC-based VCOs, despite a lower power supply.

Table 1. Performance summary and comparison with the state of the art.

		Ek JSSC'18 [8]	Ma JSSC'20 [13]	Deng JSSC'20 [24]	This Work
CMOS technology		28 nm FD-SOI	65 nm	65 nm	28 nm FD-SOI
Power supply	**(V)**	1.2	1	1	0.7
Power consumption	**(mW)**	3.3	-	11.6	8.4
Tuning approach		SC + varactor	SC + varactor	SC + Varactor	SC + varactor
Center frequency	**(GHz)**	18	39.6	20	39
Tuning range	**(GHz)**	16.3 to 19.7	37.2 to 42	17.4 to 22.4	37.4 to 40.7
PN[(a)] @ 1 MHz	**(dBc/Hz)**	−92.3 [(b)]	−93.4	−96.9	−94
Calibration extra time		YES	YES	YES	NO

[(a)] Normalized around 39 GHz. [(b)] Simulated.

4. Conclusions

A novel frequency tuning strategy for switched-capacitor-based mm wave VCOs has been presented, which overcomes the settling-time limitations of conventional SC tuning techniques. Indeed, by exploiting a customized flash A/D control circuit, coarse and fine tuning are simultaneously performed, thus getting rid of VCO calibration extra time. Thanks to the effectiveness of the proposed technique, high-speed frequency locking can be performed, which is usually required in advanced wireless communication systems.

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Conflicts of Interest: The authors declare no conflict of interest.

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