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A P-Q Coordination Control Strategy of VSC-HVDC and BESS for LVRT Recovery Performance Enhancement

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Abstract: Voltage source converter (VSC)-based multi-terminal direct current (MTDC) transmission technology has been a research focus, and the low-voltage ride-through (LVRT) and recovery in receiving-end systems is one of the major problems to consider. A coordinated control strategy for a VSC-MTDC system is proposed to improve the frequency and voltage dynamics in the receiving-end system during the LVRT and recovery processes. A battery energy storage system (BESS) plays a significant role in providing frequency and voltage support with its flexible power control capability. During the LVRT process, the BESS can provide reactive current injection and active current absorption to improve system stability in the AC side, and during the recovery process, an adaptive current limitation method is proposed for the BESS converter to dynamically adjust the active and reactive power outputs according to the frequency and voltage deviation severity. Meanwhile, the coordination of the sending-end systems and DC chopper can reduce the power output to avoid DC overvoltage during LVRT, and it can also provide frequency support to the receiving-end system with the DC voltage transmitting frequency information during the recovery process. A simulation was carried out on the MATLAB/Simulink platform, and a three-terminal VSC-MTDC system was used to validate the effectiveness of the proposed strategy.

Keywords: VSC-MTDC; LVRT; BESS; frequency and voltage support; coordinated control

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1. Introduction

Wind power has rapidly developed, playing a significant role in power supply, and voltage source converter (VSC)-based high-voltage direct current (HVDC) has been the most promising and rapidly developing technique for offshore wind farm (WF) connection due to its outstanding advantages compared with the conventional line-commutated converter-based HVDC (LCC-HVDC) transmission, e.g., independent active and reactive power control, black start capability, self-commutation, etc. [1]; hence, it is widely used in engineering projects [2]. For instance, there has been a certain number of VSC-HVDC projects for offshore WF connection reported in Germany and Britain [3], and some HVDC projects in Jiangsu and Guangdong have also been put into operation in recent years in China [4–6]. For a VSC-HVDC system, low-voltage ride-through (LVRT) is always a problem. When a serious grid fault occurs in the receiving-end system, the transmitted power via the receiving-end converter will possibly drop dramatically, and the power from the sending-end AC system and WF will then accumulate on the DC link, causing a DC voltage rise and triggering the DC overvoltage protection [7]. Furthermore, the grid fault will result in a risk of frequency disturbance in the receiving-end system; hence, frequency support should also be taken into consideration in the control strategy during LVRT and system recovery [8].

As for the VSC-MTDC LVRT technique, there are two main issues that need to be solved: (1) AC voltage sag and (2) DC voltage rise. To support the AC voltage, it is necessary to inject a certain reactive current to the grid according to a grid code [9]. Aside

from extra static synchronous compensators [10,11], converters also have the ability to provide reactive power compensation. As for VSC-HVDC converters, the reactive current can be provided and prioritized over the active current to restore the grid voltage during LVRT [12]. The wind turbine converters can also provide reactive power support via an additional fault current limiter as an auxiliary device [13] or by introducing a feedforward compensation term in the rotor- and grid-side converter control loops [14]; however, these methods can only be applied to WFs that connect to the grid via an AC transmission line, and the frequency support has not been taken into account. On the other hand, the main reason that DC voltage rise occurs is due to a power imbalance in the DC link. To solve this issue, one direct method is to install energy dissipation equipment, such as DC choppers [15] and dynamic braking systems [16]. However, this may require the electronic devices to withstand a large surplus current, which may increase the investment cost. Another way to reduce the imbalanced power is via a fast active power reduction in the sending-end systems. For instance, the researchers of [17–19] have intentionally decreased the AC voltage of a WF to activate the WF LVRT and reduce the WF power output when a grid fault occurred. Nevertheless, a large burst in the current in the braking resistors still exists in the early stage of the grid fault [19], and the LVRT and recovery of the WF may bring out other protection or synchronization instability problems [20,21]. Hence, the coordination of converters and energy dissipation equipment can be further explored to avoid DC overvoltage during the LVRT process.

After the fault is cleared, the receiving-end grid needs to return to a steady state as soon as possible. During this process, the fluctuations in both the system frequency and voltage should be suppressed. The flexible power control proposed in [12] makes the most use of reactive power support capability for grid voltage restoration during the LVRT and recovery processes without considering frequency support. Some researchers have proposed an active energy control to recover the WF's active power and the energy of the WF converter [22], and some have paid attention to DC voltage restoration [23], but the dynamics of the AC grid have not been discussed. In [8], a voltage and frequency regulation control strategy for wind turbines based on a super capacitor (SC) has been proposed. The functional mode of the SC can be switched so that it can provide reactive power support during the fault and active power support in the recovery stage. Similarly, a frequency voltage support method has been proposed for distributed energy resources in [24], such as a converter-interfaced battery energy storage system (BESS). The active and reactive power outputs will increase or decrease linearly according to the frequency and voltage variation but without coordination. The above two methods do not realize the coordination of active and reactive powers. Another control strategy for a BESS in a low-voltage distribution grid was developed in [25], in which frequency and voltage coordination control were realized by adjusting the reference current magnitude and its angle. However, this control strategy is not suitable for high-voltage transmission systems such as VSC-HVDC. Additionally, the common disadvantage of the methods in [24,25] is that the rated capacity of the converter is not considered. In fact, the capacity of the converter can be adaptively distributed for active and reactive powers, and then the converter can realize the coordinated control of the frequency and voltage support, which can be fully utilized in our research. Additionally, sending-end systems can also participate in receiving-end system frequency regulation, further improving the system frequency dynamics.

Based on the above analysis, this paper proposes a P-Q coordination control strategy for a VSC-MTDC power system integrated with a BESS to improve the system frequency and voltage dynamics during the LVRT and system recovery processes. The converters will coordinate to provide AC voltage support and avoid DC overvoltage with the help of the DC chopper when a grid fault occurs in the receiving-end system, and then participate in frequency and voltage fluctuation suppression during the recovery process. With a fast response and flexible power control capability, the BESS will play an important role in the whole process to provide frequency and voltage support.

The main contributions of this paper are listed as follows:

(1) An active power absorption control rule is proposed for a BESS to absorb active power according to the voltage drop during the LVRT process. Such a design can improve the system frequency regulation dynamics and enhance the system transient stability.
(2) An adaptive current limitation method is proposed for a BESS in which the active and reactive current references will be limited according to the frequency and voltage deviation during the recovery process. In this way, the active and reactive powers can be dynamically adjusted while considering the frequency and voltage fluctuation degree and the constraint of the converter-rated capacity to provide both frequency and voltage support.
(3) The coordination sequence of the sending-end systems and DC chopper is improved to reduce the surplus power that needs to be dissipated and to lower the requirement for electronic devices. Additionally, such coordination can also allow the sending- end systems to provide frequency regulation, with the DC voltage transmitting frequency information during the recovery process.

The rest of this paper is organized as follows: Section 2 demonstrates the problems in the existing control strategy. Section 3 presents the proposed P-Q coordination control strategy in detail. The design of the key parameters and the system stability analysis are conducted in Section 4. The simulation is based on the MATLAB/Simulink platform and the results are given in Section 5. Finally, the conclusions are drawn in Section 6.

2. System Configuration and Problem Description

2.1. System Configuration

In Figure 1, a typical three-terminal VSC-HVDC system is used to represent a typical VSC-MTDC topology, and a wind farm is interconnected via a converter station with the system, which can be regarded as a typical VSC-HVDC application scenario and be widely used in a real power system [5,6]. The receiving-end system, AC1, is a modified three-machine nine-bus system with three synchronous generators (SGs), G1–G3, and load nodes, L1–L3. The sending-end system, AC2, is represented by one SG for the sake of simplicity. A single doubly fed induction generator (DFIG)-based wind turbine (WT) is used to represent the whole aggregated WF. The two AC systems and the WF are interconnected via three converters, namely REVSC, SEVSC, and WFVSC. The power from the sending-end system, AC2, and the WF are transmitted to the receiving-end system, AC1, through the HVDC link. A DC chopper is connected to the DC terminal of REVSC in parallel. Additionally, a BESS near REVSC is connected to AC1 via BAVSC. The arrows in Figure 1 denote the positive power flow direction. Other details will be explained in Section 5.

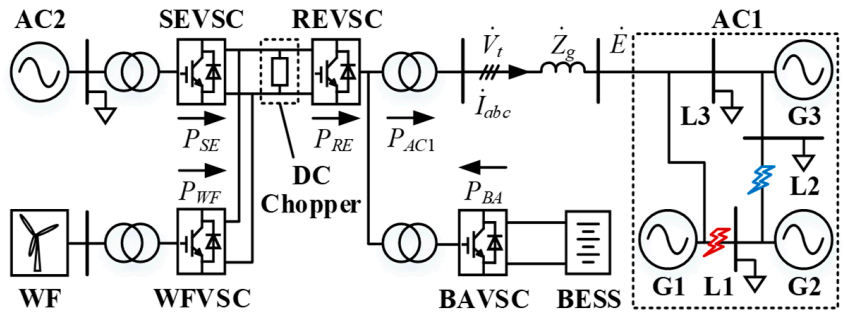


Figure 1. The diagram of the studied three-terminal VSC-HVDC system.

2.2. Conventional Control Strategy

In a conventional control strategy, when a grid fault occurs in AC1, the possible control methods for converters and the DC chopper in Figure 1 include the following:

(1) BAVSC P-f and Q-V control [24], which enables BAVSC to generate/absorb active and reactive power with the ramp rate control when the grid frequency and voltage deviate from the nominal values.

(2) REVSC reactive current control [12], which injects the reactive current as a priority for voltage support as per the grid code during LVRT and adjusts the active current reference according to the change in the reactive current reference.
(3) WFVSC AC voltage reduction control and WF active power reduction control [19], which change the AC voltage to 0.2 p.u. after detecting that the DC voltage exceeds the limit, intentionally leading to the LVRT process of the WF and reducing the WF power output.
(4) SEVSC active power reduction control [26], which controls the sending-end AC system to reduce the power output when the DC voltage exceeds the limit.
(5) DC chopper control [19], which triggers the DC chopper to dissipate the surplus power in the DC link when the DC voltage increases to the limit value.

In this way, based on the aforementioned control methods, during the LVRT process, the system dynamics can be improved on both AC and DC sides: (1) On the AC side, BAVSC and REVSC can provide certain reactive power to support the AC voltage drop. (2) On the DC side, WFVSC, SEVSC, and the DC chopper can cooperate to avoid DC overvoltage.

However, such a control strategy mainly focuses on the grid voltage support but gives little consideration to frequency regulation, especially during system recovery. Although the BAVSC control can provide both frequency and voltage support in the whole process, it lacks collaboration between the active and reactive powers and ignores the rated capacity of the converter as a constraint. Furthermore, the present coordination sequence of the sending-end systems and DC chopper still require the DC chopper to dissipate the rated power output from the sending-end systems in the early stage of the grid fault; hence the rated current of electronic devices should be large enough to withstand the power flow in the first few hundred milliseconds.

3. The Proposed P-Q Coordination Control Strategy

3.1. Overall Description

To avoid the aforementioned problems, a P-Q coordination control strategy is developed to improve the frequency and voltage dynamics by utilizing all potential equipment in the following two processes as follows: (1) During the LVRT process, the BESS and the receiving-end converters adopt the reactive current control to provide voltage support, while the sending-end converter and the WF reduce the power output via droop control, and the DC chopper is activated to dissipate the surplus power to avoid DC overvoltage. (2) During the recovery process, the BESS converter adopts the proposed adaptive current limitation to enhance both the frequency and voltage dynamics, and the sending-end converter and the WF can further participate in frequency regulation via DC voltage modulation.

The overall control diagram is shown in Figure 2. It can be seen that all the converters and the DC chopper only need local signal measurements (frequency and AC and DC voltages) to be activated. The system's AC voltage measurement can be used to estimate whether the system is under the LVRT process, and it can also be used as the trigger signal to switch the control modes of each controller in different periods. This paper will mainly focus on the time scale of frequency and voltage regulation; the inner control loops and the PWM generation blocks of certain control blocks in Figure 2 are not discussed, and the typical PI control loop parameters used in [27] are used in the study and shown in Appendix A.

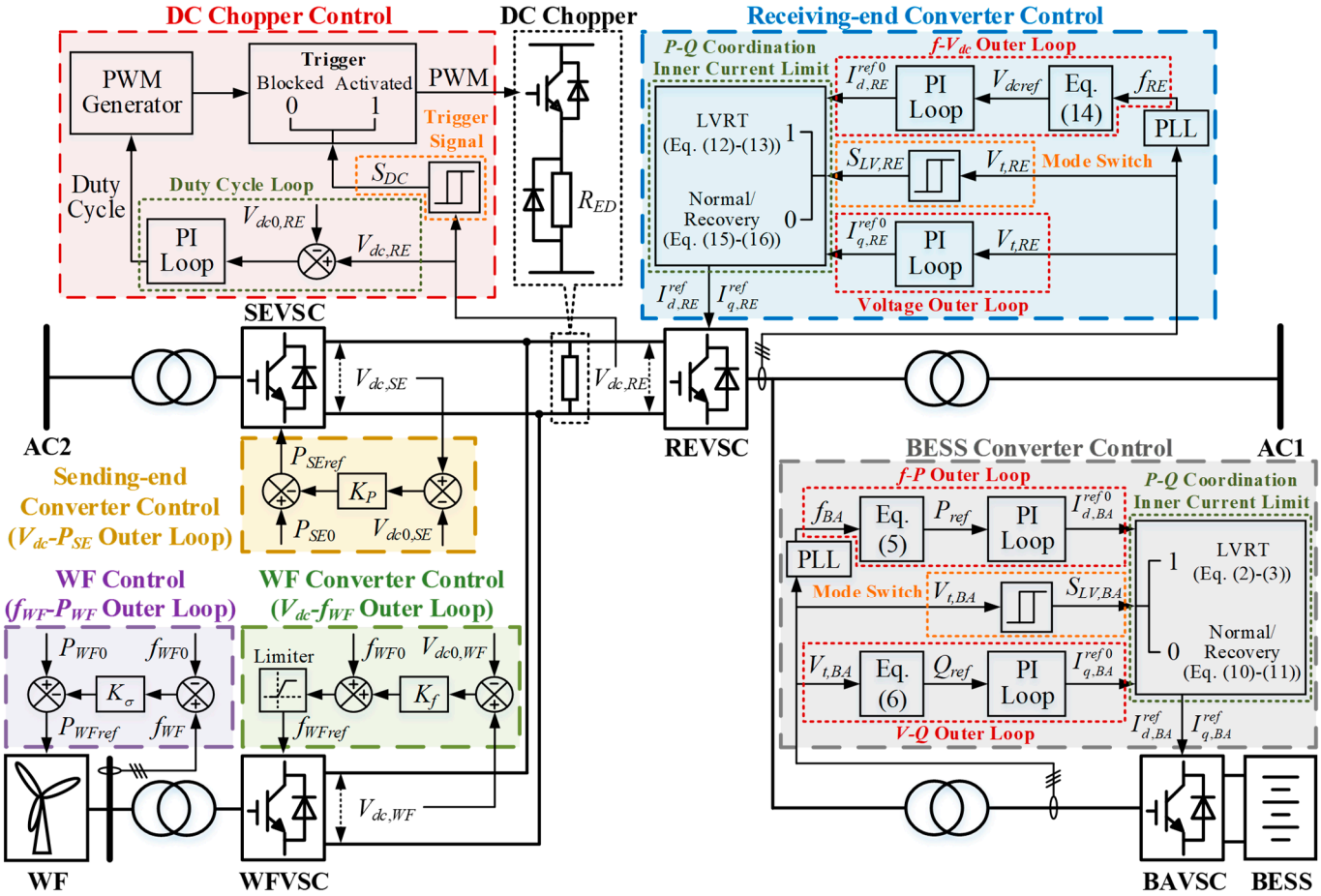


Figure 2. The diagram of the overall control strategy.

3.2. BESS Converter Control

During the LVRT process, the main target of the BESS converter control is to support the system voltage, and the frequency support and system stability enhancement should also be taken into account. The following is the generator swing equation:

$$2H_G \frac{d\omega}{dt} = P_m - P_e \tag{1}$$

where H_G is the inertial time constant; ω is the angular frequency; and P_m and P_e are the mechanical power and electrical power, respectively.

When a grid fault occurs, a dramatic drop in the system voltage results in P_e sharply reducing, while P_m can be considered unchanged at the moment; hence, the rotor speed increases, i.e., the system frequency increases. From this aspect, the BESS needs to absorb active power to improve frequency regulation.

According to the requirement of LVRT in the grid code [9], converter-interfaced equipment should provide a certain reactive current for voltage support, while there are few specific requirements for the active current. Considering the fact that the voltage drop degree can reflect the frequency deviation level during LVRT, and referring to the calculation of the reactive current in the grid code [9], the active current absorption is designed to be proportional to the value of the AC voltage drop. Therefore, by considering the reactive current control during the LVRT process, the control rule of the BESS converter can be designed as follows:

$$I^{ref}_{q,BA} = -\min\{k_q(0.9 - V_{t,BA}),\ I_{\max}\} \tag{2}$$

$$I_{d,BA}^{ref} = -\min\left\{k_d(0.9 - V_{t,BA}),\ \sqrt{I_{\max}^2 - \left(I_{q,BA}^{ref}\right)^2}\right\} \tag{3}$$

where $V_{t,BA}$ is the converter terminal voltage; k_q and k_d are the proportional coefficients of the reactive and active current references, respectively; and $I_{\max}$ is the converter current limit defined as in [27]:

$$I_{\max} = \min\{1.2I_n,\ S_{BA}/V_{t,BA}\} \tag{4}$$

where I_n is the rated converter current, and S_{BA} is the rated converter capacity.

It can be seen from (2) and (3) that, during LVRT, the BESS converter can provide reactive power and, in the meantime, absorb active power. Such a design can not only provide frequency support, but also help improve the system's transient stability, which will be further demonstrated in Section 4.

After the fault is cleared, the system frequency and voltage should return to the nominal values as soon as possible. The active and reactive power references, P_{ref} and Q_{ref}, in Figure 2 can be calculated as follows [28]:

$$P_{ref} = K_{Bf} \cdot (f_{BA} - f_{BA0}) \tag{5}$$

$$Q_{ref} = K_{BV} \cdot (V_{t,BA} - V_{t0,BA}) \tag{6}$$

where K_{Bf} and K_{BV} are the droop coefficients of the active and reactive power references, respectively; f_{BA} and f_{BA0} are the measured system frequency and its rated value, respectively; and $V_{t0,BA}$ is the rated value of the converter terminal voltage.

Then, the original active and reactive current references, $I_{d,BA}^{ref0}$ and $I_{q,BA}^{ref0}$, can be generated via outer PI loops, as shown in Figure 2. To avoid the current exceeding the maximum value, the current references should also be limited. Traditional methods for current limitation mainly include the following: (1) reactive current injection in priority, which has been adopted during the LVRT process, and (2) active current injection in priority. However, during the recovery process, both the frequency and voltage fluctuations should be well suppressed. Hence, an adaptive current limitation method is proposed in which the active and reactive current references should be limited according to the frequency and voltage deviations. The more the frequency/voltage deviates from the nominal value, the more the active/reactive current reference should be distributed. The coordination index M is proposed to compare the frequency and voltage deviations in the same dimension:

$$M = \frac{M_f}{\sqrt{M_V^2 + M_f^2}} \tag{7}$$

$$M_f = \begin{cases} \frac{f_{BA} - f_0}{f_{\max} - f_0} & f_{BA} > f_0 + \Delta f_{db} \\ 0 & f_0 - \Delta f_{db} \le f_{BA} \le f_0 + \Delta f_{db} \\ \frac{f_0 - f_{BA}}{f_0 - f_{\min}} & f_{BA} < f_0 - \Delta f_{db} \end{cases} \tag{8}$$

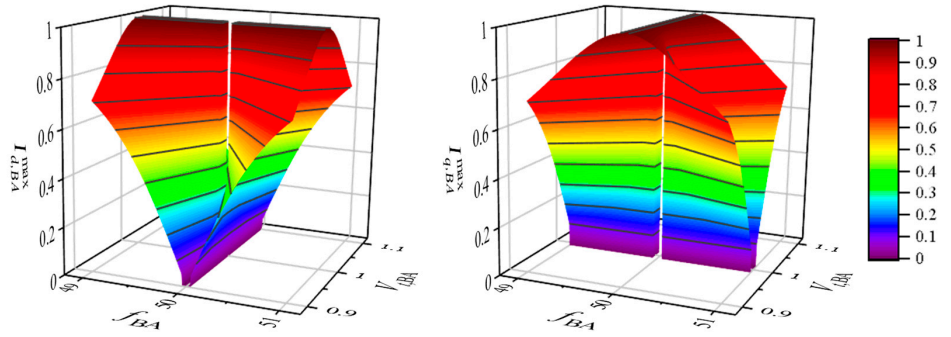
$$M_V = \begin{cases} \frac{V_{t,BA} - V_{t0}}{V_{t\max} - V_{t0}} & V_{t,BA} > V_{t0} + \Delta V_{t,db} \\ 0 & V_{t0} - \Delta V_{t,db} \le V_{t,BA} \le V_{t0} + \Delta V_{t,db} \\ \frac{V_{t0} - V_{t,BA}}{V_{t0} - V_{t\min}} & V_{t,BA} < V_{t0} - \Delta V_{t,db} \end{cases} \tag{9}$$

where f_{BA}, f_0, $V_{t,BA}$, and V_{t0} are the measured and rated system frequency and converter terminal voltage values, respectively; $f_{\max}$ and $f_{\min}$ are the maximum and minimum allowable frequency values, respectively; $V_{t\max}$ and $V_{t\min}$ are the maximum and minimum allowable voltage values, respectively; and Δf_{db} and $\Delta V_{t,db}$ are the dead-band ranges of the frequency and voltage, respectively. Specifically, if both M_f and M_V are 0, M equals 0. Then, the active and reactive current references can be limited, as shown below, and their maximum limitation values, $I_{d,BA}^{\max}$ and $I_{q,BA}^{\max}$, changing with f_{BA} and $V_{t,BA}$, are shown in Figure 3:

$$I_{d,BA}^{ref} = \text{sign}(I_{d,BA}^{ref0}) \cdot \min\left\{\left|I_{d,BA}^{ref0}\right|,\ I_{d,BA}^{\max}\right\} \tag{10}$$

$$I_{q,BA}^{ref} = \text{sign}(I_{q,BA}^{ref0}) \cdot \min\left\{\left|I_{q,BA}^{ref0}\right|,\ I_{q,BA}^{\max}\right\} \tag{11}$$

where sign(x) is the sign function and denotes the sign of the variable x; $I_{d,BA}^{\max} = M \cdot I_{\max}$; and $I_{q,BA}^{\max} = \sqrt{1 - M^2} \cdot I_{\max}$.



(**a**) (**b**)

Figure 3. The effects of f_{BA} and $V_{t,BA}$ on the active and reactive current limitations. (**a**) The effect of f_{BA} and $V_{t,BA}$ on active current limitation; (**b**) the effect of f_{BA} and $V_{t,BA}$ on reactive current limitation.

Based on (7)–(11) and Figure 3, it can be seen that M_f and M_V reflect the system frequency and voltage deviations, while M reflects the ratios of M_f and M_V and is also used to adjust the limitation values of the active and reactive currents. In this way, the active and reactive powers can be provided in a proper ratio to support both the system frequency and voltage, and can thus improve the system recovery comprehensively.

Additionally, the trigger signal $S_{LV,BA}$ in Figure 2 is used to estimate whether the system is undergoing the LVRT process, and it enables the converter to switch to the corresponding control rules. The signal is obtained via a hysteresis comparator with the terminal voltage as the input signal. Once the system voltage drops to below the threshold value $V_{t,LV}$, $S_{LV,BA}$ turns to 1 and enables the converter to adopt the control rules in (2) and (3); when the system voltage rises above the threshold value $V_{t,rcv}$, $S_{LV,BA}$ turns to 0 and the converter switches to the control rules in (10) and (11). The above process corresponds to the "P-Q Coordination Inner Current Limit" and "Mode Switch" blocks in Figure 2.

Note that the state of charge (SOC) of the BESS may have an impact on the control accuracy of the converter, which has been studied in our previous work [26]. In this paper, the influence of the SOC on the BESS is ignored.

3.3. Receiving-End Converter Control

Similar to the BESS converter, the receiving-end converter also needs to support the system voltage, while the receiving-end converter also needs to try to maintain the DC voltage and cannot inject active power into the DC link. Hence, the control rule of the receiving-end converter during the LVRT process is as follows [9,12]:

$$I_{q,RE}^{ref} = -\min\{k_q(0.9 - V_{t,RE}),\ I_{\max}\} \tag{12}$$

$$I_{d,RE}^{ref} = \sqrt{I_{\max}^2 - \left(I_{q,RE}^{ref}\right)^2} \tag{13}$$

where $V_{t,RE}$ is the converter terminal voltage; $I_{\max}$ is the converter current limit and can also be defined as (4), with the subscripts "BA" replaced by "RE"; and S_{RE} is the rated converter capacity.

In this way, the control rules in (12) and (13) enable the receiving-end converter to provide reactive power support as a priority during LVRT. It can be seen that the severity of the system voltage drop has a strong impact on active power transmission, since a deep

voltage drop may enlarge the value of $I_{q,RE}^{ref}$ and then greatly reduce $I_{d,RE}^{ref}$ and the active power output.

During the recovery process, the converter restarts to control the DC voltage. In order to suppress frequency deviation rapidly, the DC voltage can be used to transfer frequency information to the sending-end AC system and wind farm and enable them to participate in frequency regulation, and the DC voltage reference V_{dcref} can be calculated as follows [29]:

$$V_{dcref} = V_{dcref0} + K_V \cdot (f_{RE} - f_{RE0}) \tag{14}$$

where V_{dcref0} is the rated DC voltage reference; K_V is the droop coefficient; and f_{RE} and f_{RE0} are the measured system frequency and its rated value, respectively. In this way, the system frequency deviation can be transferred into DC voltage deviation and can be detected by the sending-end and WF converters.

As for the current reference limitation, considering that the receiving-end converter needs to control the DC voltage and transfer the active power, the active current should be injected as a priority during the recovery process, and the active and reactive current references can be obtained as follows:

$$I_{d,RE}^{ref} = \min\left\{ I_{d,RE}^{ref0},\ I_{\max} \right\} \tag{15}$$

$$I_{q,RE}^{ref} = \text{sign}(I_{q,RE}^{ref0}) \cdot \min\left\{ \left| I_{q,RE}^{ref0} \right|,\ \sqrt{I_{\max}^2 - \left(I_{d,RE}^{ref}\right)^2} \right\} \tag{16}$$

where $I_{d,RE}^{ref0}$ and $I_{q,RE}^{ref0}$ are the original active and reactive current references generated via outer PI loops, as shown in Figure 2.

Similarly, the trigger signal $S_{LV,RE}$ in Figure 2 can also be obtained via the hysteresis comparator with the same threshold parameters as in the BESS converter: when $S_{LV,RE} = 1$, the converter adopts the control rules in (12) and (13); otherwise, it adopts (15) and (16). The process also corresponds to the "P-Q Coordination Inner Current Limit" and "Mode Switch" blocks in Figure 2.

3.4. Sending-End Systems Control

The sending-end systems include the sending-end AC system and WF. Based on the previous analysis and control rules, there are two possible reasons why the DC voltage rises: (1) the receiving-end system is under the LVRT process or (2) the receiving-end system frequency is larger than the rated value. Under either circumstance, the sending-end systems should reduce the power output. In this way, as for the sending-end converter, the power reference P_{SEref} changes according to the DC voltage as follows [26]:

$$P_{SEref} = P_{SE0} + K_P \cdot (V_{dc,SE} - V_{dc0,SE}) \tag{17}$$

where P_{SE0} is the initial power reference; K_P is the droop coefficient; and $V_{dc,SE}$ and $V_{dc0,SE}$ are the measured DC voltage and its rated value, respectively.

As for the WF, to avoid the protective and synchronous problems caused by LVRT in the WF [20,21], the WF converter will change the WF frequency reference f_{WFref} based on the DC voltage instead of changing the WF voltage, and then the WF can adjust its power output reference P_{WFref} according to the WF frequency deviation [26,29]. Moreover, to prevent the WF frequency from exceeding the limitation $f_{WF\max}$, a limiter is further added in the WF converter, as shown in Figure 2. The control rules can be expressed as follows [26,29]:

$$f_{WFref} = f_{WF0} + K_f \cdot (V_{dc,WF} - V_{dc0,WF}) \tag{18}$$

$$P_{WFref} = P_{WF0} - K_\sigma \cdot (f_{WF} - f_{WF0}) \tag{19}$$

where f_{WF0} is the rated WF frequency; $V_{dc,WF}$ and $V_{dc0,WF}$ are the measured DC voltage and its rated value, respectively; P_{WF0} is the initial WTG power output, generally determined

by the MPPT control mode; f_{WF} and f_{WF0} are the measured WF frequency and its rated value, respectively; and K_f and K_σ are the droop coefficients for the WF converter and WF, respectively.

Based on the control rules in (17)–(19), the sending-end systems can decrease the power output to reduce the power imbalance when a grid fault occurs in the receiving-end system, and they can also adaptively change the power output during the system recovery process to help suppress the frequency deviation.

3.5. DC Chopper Control

When a severe fault occurs in the receiving-end system, the power transmission will be seriously affected, and the DC voltage may rise sharply. At this time, power reduction from the sending-end systems is not enough to keep DC voltage stability. Thus, a DC chopper should be activated for energy dissipation.

The DC chopper is connected to the DC terminal of the receiving-end converter in parallel. The IGBTs and centralized braking resistor are connected in series, and PWM is used to control all the IGBTs, with the absorbed power being determined by the duty cycle [15]. It should be noted that the adopted topology of the DC chopper may not be the best, but improving the topology is not the key point of this paper. The main purpose of this paper is to demonstrate the effect of the DC chopper and the coordination of each equipment during the LVRT and recovery processes.

It can be seen from the "Duty Cycle Loop" in Figure 2 that the duty cycle of the PWM is determined by the DC voltage. The higher the DC voltage, the more imbalanced power should be absorbed, and the larger the duty cycle should be. Moreover, since the receiving-end converter will control the DC voltage to transmit system frequency deviation during the recovery process, a hysteresis comparator is also adopted here to avoid misoperation: when the DC voltage rises above the threshold value $V_{dc,LV}$, the trigger signal S_{DC} turns to 1 and activates the DC chopper for energy dissipation; when the DC voltage drops below the threshold value $V_{dc,rcv}$, then S_{DC} turns to 0 and blocks the DC chopper, which corresponds to the "Trigger Signal" block in Figure 2.

3.6. Discussion

Based on the aforementioned design, the control rules of each equipment can coordinate with each other for frequency and voltage support during the LVRT and recovery processes, and the corresponding algorithm flow chart is shown in Figure 4.

(1) During the LVRT process, the system's AC voltage decreases rapidly. When detecting that the AC voltage is lower than $V_{t,LV}$, the BESS and receiving-end converters will inject a reactive current as a priority with (2), (3), (12), and (13) as per the grid code requirement. Meanwhile, the BESS will absorb certain active power with (3) to help reduce the frequency deviation and improve the system stability if the reactive power output does not reach the converter capacity.

As for the DC side, since the system voltage reduction lowers the power transmission capability of the receiving-end converter, the power imbalance may cause the DC voltage to rise. Consequently, the sending-end and WF converters can detect the DC voltage deviation and change the power outputs to reduce the imbalanced power with (17)–(19). If the DC voltage continues rising and exceeds the threshold value $V_{dc,LV}$, the DC chopper will then be activated to absorb the surplus power. In this way, the system dynamics during LVRT in both the AC and DC sides can be improved.

(2) During the recovery process, it is important to suppress the system frequency and voltage fluctuations as soon as possible. When the AC voltage rises above $V_{t,rcv}$, both the BESS and receiving-end converters turn to normal/recovery mode and can provide frequency and voltage support with (10), (11), (15), and (16). Considering that traditional current limitation methods take only active or reactive current as a priority, a new current limitation method in (7)–(9) is proposed in which the active and reactive currents can be limited according to the frequency and voltage deviation severity, enabling active and

reactive powers to be provided in a proper ratio. Only the local signal measurement is needed, and the calculation is updated in real time.

Moreover, during the recovery process, the DC chopper will be blocked when detecting that the DC voltage is lower than $V_{dc,rcv}$. Additionally, the receiving-end converter can further change the DC voltage according to the system frequency with (14) so that the frequency information can be transmitted to the sending-end systems, and AC2 and WF can also participate in frequency regulation with (17)–(19), improving system recovery.

It can be seen that full use has been made of the BESS to improve both the frequency and voltage dynamics during the whole process, which illustrates its significant role in providing system support. Furthermore, it should be noted that the coordination sequence of the sending-end systems and DC chopper has been improved in the proposed control. In the conventional control, the power reduction in the sending-end systems is activated at the same time when the DC chopper is triggered, while in the proposed control, the power output from the sending-end systems will decrease as soon as the DC voltage increases, and the DC chopper will be activated later when the DC voltage exceeds the threshold value. Such a difference is significant to enable the sending-end systems to take part in the receiving-end system frequency regulation during the recovery process and reduce the surplus power that needs to be dissipated by the DC chopper.

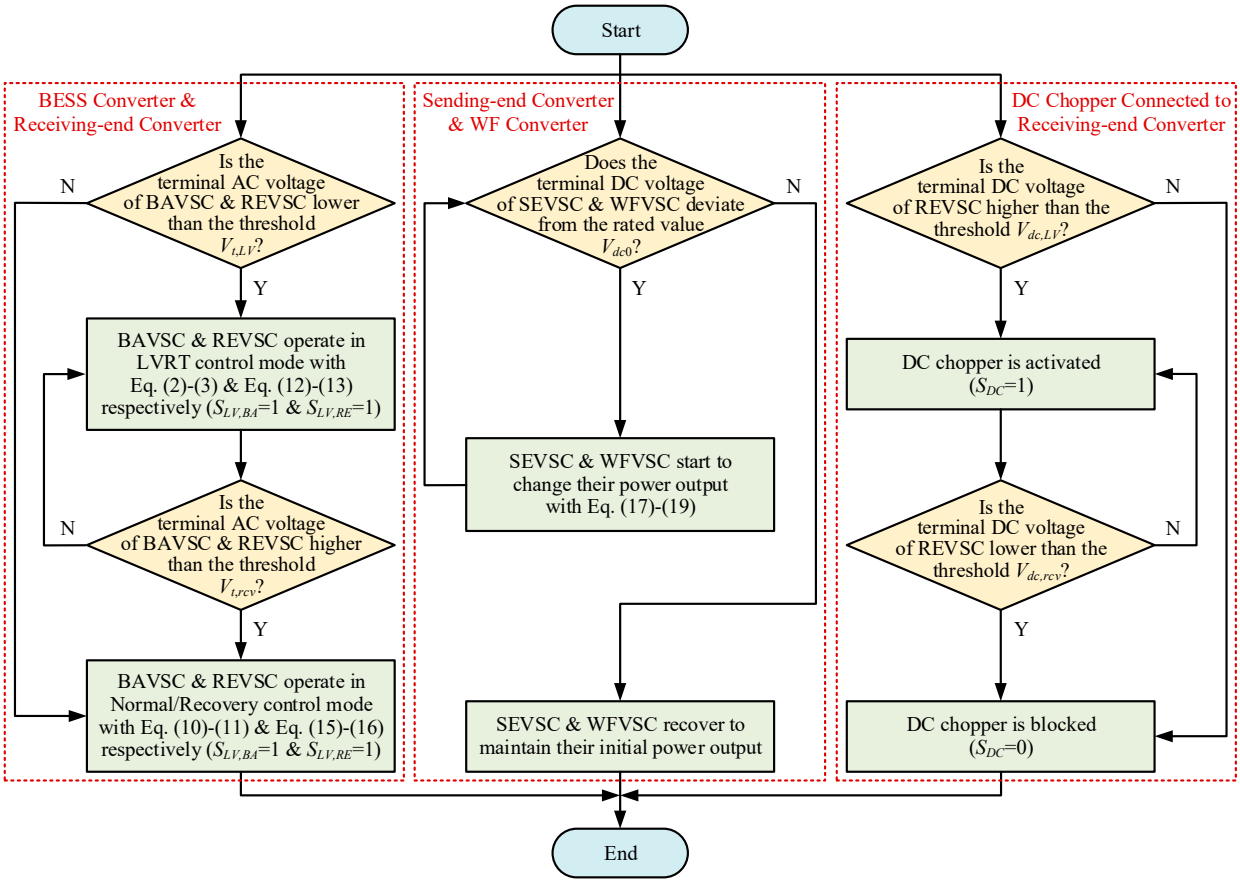


Figure 4. The coordination chart of the equipment under the proposed control strategy during the LVRT and recovery processes.

4. Key Parameters Affecting Analysis and Design

4.1. Transient Voltage Stability Analysis during LVRT

4.1.1. Relationship between Terminal Voltage and Active Current

According to Figure 1, the current of the converter side satisfies $\dot{I}_{abc} = \dot{I}_{abc,BA} + \dot{I}_{abc,RE}$, where $\dot{I}_{abc,BA}$ and $\dot{I}_{abc,RE}$ are the current vectors of the BAVSC and REVSC terminals. Then, it can be transformed into the *dq* frame:

$$\begin{bmatrix} I_d \\ I_q \end{bmatrix} = \begin{bmatrix} I_{d,BA} \\ I_{q,BA} \end{bmatrix} + \begin{bmatrix} I_{d,RE} \\ I_{q,RE} \end{bmatrix} \tag{20}$$

It neglects the inner loop of the converter, i.e., $I_{d,BA} = I_{d,BA}^{ref}$, $I_{q,BA} = I_{q,BA}^{ref}$, $I_{d,RE} = I_{d,RE}^{ref}$, $I_{q,RE} = I_{q,RE}^{ref}$. Moreover, when neglecting the transformer saturation and loss, the terminal voltage values of the BESS and receiving-end converters are considered equal, i.e., $V_{t,BA} = V_{t,RE} = V_t$. By combining (2), (3), (12), (13), and (20), the relationship between the terminal voltage V_t and the active current I_d on the converter side (namely "control curve" in the following) can be obtained as follows:

$$I_d = \max\left\{ \sqrt{I_{\max}^2 - \left[k_q(0.9 - V_t)\right]^2} - k_d(0.9 - V_t) \cdot \frac{S_{BA}}{S_{RE}},\ \sqrt{I_{\max}^2 - \left[k_q(0.9 - V_t)\right]^2} \cdot \left(1 - \frac{S_{BA}}{S_{RE}}\right),\ 0 \right\} \tag{21}$$

where the term S_{BA}/S_{RE} is used to unify the base value of the current between the two converters. For the sake of simplicity, the values of k_q in (2) and (12) are the same.

As for the grid side, the network equation can be expressed as follows:

$$\dot{V}_t = \dot{E} + \dot{Z}_g \dot{I} \tag{22}$$

where $\dot{E}$ is the grid voltage, and $\dot{Z}_g = Z_g \angle \theta_g$, which is the line impedance of the grid.

By transforming (22) into a V_t-oriented dq frame and combining (2) and (12), the relationship between V_t and I_d on the grid side (namely the "system curve" in the following) can be derived as follows:

$$\begin{cases} \left[V_t - Z_g(I_d \cos\theta - I_q \sin\theta)\right]^2 + \left[Z_g(I_d \sin\theta + I_q \cos\theta)\right]^2 = E^2 \\ I_q = k_q(0.9 - V_t) \cdot \left(1 + \frac{S_{BA}}{S_{RE}}\right) \end{cases} \tag{23}$$

Therefore, (21) and (23) constitute the system quasi-steady model during LVRT, and the intersection of the two curves is the system equilibrium point.

4.1.2. Key Factors Influencing Transient Voltage Stability

According to (21) and (23), the two curves are mainly influenced by the grid voltage E, the grid impedance amplitude Z_g and its angle θ_g, and the proportional coefficients k_q and k_d, which also affect the existence of the equilibrium point as well as the system transient voltage stability. The influence of these factors on the equilibrium point will be analyzed based on the V_t-I_d plane. The default values of the parameters are set as E = 0.3 p.u., Z_g = 0.5 p.u., θ_g = 80°, k_q = 2, and k_d = 3, and only one parameter will vary, while the others will be fixed in each figure.

(1) Grid voltage E

The system V_t-I_d characteristics when changing the grid voltage drop E are shown in Figure 5a. All of the system equilibrium points are stable (for example, it can be seen that the control curve shows a negative feedback characteristic at point A). It can be seen from Figure 5a that with the decreasing grid voltage, the system equilibrium point does not exist. In other words, under an extremely deep voltage drop, the system may not be able to maintain stability.

(2) Grid impedance amplitude Z_g

The system V_t-I_d characteristics when changing the grid impedance amplitude Z_g are shown in Figure 5b. Point B is an unstable equilibrium point since the control curve shows a positive feedback characteristic. It can be seen from Figure 5b that with the increasing grid impedance amplitude, the system equilibrium point does not exist, i.e., a large impedance may deteriorate the system's stability.

(3) Grid impedance angle θ_g

The system V_t-I_d characteristics when changing the grid impedance angle θ_g are shown in Figure 5c. It can be seen from Figure 5c that when changing grid impedance angle, the system equilibrium point always exists, which means the change in the grid impedance angle has little influence on the existence of the system equilibrium point.

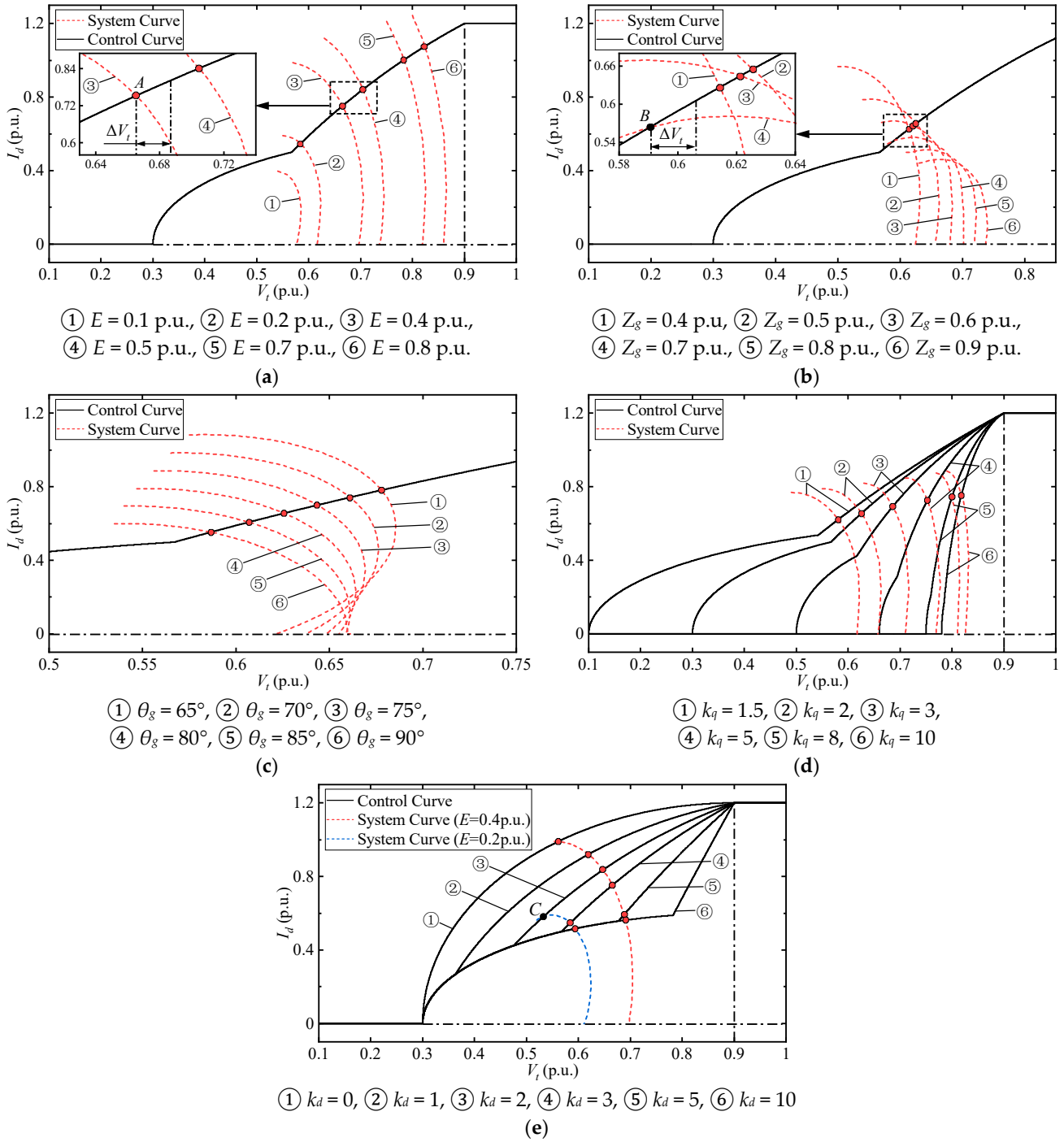


Figure 5. The diagrams of the system V_t-I_d characteristics. (**a**) when the grid voltage drop E changes; (**b**) when the grid impedance amplitude Z_g changes; (**c**) when the grid impedance angle θ_g changes; (**d**) when the proportional coefficient k_q changes; (**e**) when the proportional coefficient k_d changes.

(4) Proportional coefficient k_q

The system V_t-I_d characteristics when changing the proportional coefficient k_q are shown in Figure 5d. It can be seen from Figure 5d that changing the k_q value will influence

the two curves, and the system's stable equilibrium point always exists, which means there is no limitation to the value of k_q. However, if k_q is too large, the curves will be sharp, and a small disturbance in V_t may cause a large variation in I_d. Considering the requirements of the grid code that the recommended value of k_q ranges from 1.5 to 3 [9], k_q is set to be 2 in this paper.

(5) Proportional coefficient k_d

The system V_t-I_d characteristics when changing the proportional coefficient k_d are plotted in Figure 5e. Two system curves, shown as red and blue lines, correspond to E = 0.4 and 0.2 p.u., respectively. Specifically, the control curve ① corresponds to k_d = 0, which means that the BESS does not absorb active power during LVRT.

It can be seen from Figure 5e that k_d only influences the control curve. When E = 0.4 p.u., the system curve can intersect with all of the control curves with different k_d values. But when E = 0.2 p.u., and with a decreasing k_d value, the system equilibrium point tends to be unstable (such as point *C*) or even does not exist (the control curve does not intersect with the system curve in blue), which demonstrates that a certain active power absorption of the BESS converter during LVRT can improve the system's transient stability. According to Figure 5e, the value of k_d should not be smaller than 3. Considering the fact that a k_d value that is too large may also lead to a large variation in I_d under a small disturbance in V_t, k_d is set to be 3 in this paper.

4.2. Key Parameter Design

4.2.1. Droop Coefficients

As for the BESS converter control rules in (5) and (6), it can be considered that when the system frequency or voltage reaches the maximum allowable deviation, the active or reactive power output should also reach the maximum [26]. Considering that the maximum reactive power $Q_{BA\max}$ is theoretically only related to the converter capacity, i.e., $Q_{BA\max}$=S_{BA}, the droop coefficients K_{Bf} and K_{BV} can be designed as follows:

$$K_{Bf} = P_{BA\max}/\Delta f_{\max} \tag{24}$$

$$K_{BV} = S_{BA}/\Delta V_{t\max} \tag{25}$$

where $\Delta f_{\max} = f_{\max} - f_0$ is the maximum allowable frequency deviation and $\Delta V_{t\max} = V_{t\max} - V_{t0}$ is the maximum allowable voltage deviation, set to be 0.5 Hz and 0.1 p.u., respectively [9,30], and $P_{BA\max}$ is the nominal maximum power of the BESS.

In the same way, as for the control rules in (14) and (17)–(19), it can be considered that when the system frequency reaches the maximum allowable deviation, the DC voltage should also reach the limited allowable value, and in the meantime, the power reduction in the sending-end systems should also reach the maximum. Thus, referring to [26], the droop coefficients K_V, K_P, K_f, and K_σ can be designed as follows:

$$K_V = \Delta V_{dc\lim}/\Delta f_{\max} \tag{26}$$

$$K_P = \Delta P_{SE\max}/\Delta V_{dc\lim} \tag{27}$$

$$K_f = \Delta f_{WF\max}/\Delta V_{dc\lim} \tag{28}$$

$$K_\sigma = \Delta P_{WF\max}/\Delta f_{WF\max} \tag{29}$$

where $\Delta V_{dc\lim}$ is the limited DC voltage deviation during the recovery process, set to be 0.05 p.u. to ensure operational safety; $\Delta P_{SE\max}$ is the maximum power output variation in the sending-end AC system, and the value is the same as the initial power output of the system P_{SE0}; $\Delta f_{WF\max}$ is the maximum frequency deviation in the WTG normal operating range, i.e., 0.5 Hz [30]; $\Delta P_{WF\max} = \sigma_{\max} P_{WF0}$ is the maximum power output variation of WF; P_{WF0} is the WF's initial power output; and $\sigma_{\max}$ is the maximum power reduction ratio, generally set as 0.2.

4.2.2. Threshold Values of Hysteresis Comparators

In the proposed strategy, several hysteresis comparators are used for trigger signal generation. The hysteresis comparators in the BESS and receiving-end converters are used for LVRT estimation. Generally, the system is considered to be undergoing the LVRT process when $V_t < 0.9$ p.u. [9]. To avoid frequent state switch due to voltage fluctuation, the two thresholds, $V_{t,LV}$ and $V_{t,rcv}$, are set to be 0.9 p.u. and 0.95 p.u., respectively, in this paper.

Similarly, the hysteresis comparator in the DC chopper control strategy is added for DC chopper activation. Combined with the improved coordination sequence of the sending-end systems and DC chopper, when the DC voltage deviation exceeds $\Delta V_{dc\mathrm{lim}}$, this indicates that the rise in the DC voltage is caused by a grid fault, and the DC chopper should be activated. Thus, the upper threshold $V_{dc,LV}$ is set to be $V_{dc0} + \Delta V_{dc\mathrm{lim}}$, i.e., 1.05 p.u., while the lower threshold $V_{dc,rcv}$ is set to be 1.03 p.u. in this paper.

4.2.3. Resistor in DC Chopper

Based on the previous analysis, the centralized braking resistor should handle all of the surplus power during LVRT. Considering that the DC voltage exceeds the maximum limit, the value of the resistor can be calculated as follows:

$$R_{DC} = \frac{V_{dc\mathrm{max}}^2}{P_{dc}} \tag{30}$$

where $V_{dc\mathrm{max}}$ is the maximum allowable DC voltage and is set as 1.1 p.u. [23], and P_{dc} is the surplus DC power. As for the conventional control, the worst condition is that the surplus power equals the initial power output of AC2 and the WF; hence, $P_{dc\_C} = P_{SE0} + P_{WF0}$. As for the proposed control, since the activation sequence has been improved, the surplus power is equal to the remaining power of the WF, i.e., $P_{dc\_P} = (1 - \sigma_{\max})P_{WF0}$.

5. Case Study

The studied three-terminal VSC-HVDC system in Figure 1 is modeled on the MATLAB/Simulink platform. All of the system parameters and the control parameters based on the parameter design in Section 4 can be found in Appendix A. A comparison study is conducted using three strategies: (1) no auxiliary support (NAS) from any converters, (2) the conventional control strategy (CCS) in Section 2, and (3) the proposed control strategy (PCS) in Section 3. A comparison of the control rules used under the CCS and PCS is listed in Table 1. In this study, a series of three-phase grounding faults, regarded as the most serious type of faults in the power system, will be set to test the proposed control strategy.

Table 1. A comparison of the control rules under the CCS and PCS.

Equipment	CCS		PCS	
	Control Rules	**Activation**	**Control Rules**	**Activation**
BAVSC	$I_{q,BA}$ injection as a priority $I_{d,BA}$ injection as a priority	$V_{t,BA} < V_{t,LV}$ $V_{t,BA} > V_{t,rcv}$	$I_{q,BA}$ injection as a priority and $I_{d,BA}$ absorption adaptive current limitation control	$V_{t,BA} < V_{t,LV}$ $V_{t,BA} > V_{t,rcv}$
REVSC	$I_{q,RE}$ injection as a priority $I_{d,RE}$ injection as a priority	$V_{t,RE} < V_{t,LV}$ $V_{t,RE} > V_{t,rcv}$	$I_{q,RE}$ injection as a priority $I_{d,RE}$ injection as a priority	$V_{t,RE} < V_{t,LV}$ $V_{t,RE} > V_{t,rcv}$
SEVSC	V_{dc}-P_{SE} droop control	$V_{dc,SE} > V_{dc,LV}$	V_{dc}-P_{SE} droop control	$V_{dc,SE} \neq 0$
WFVSC	decrease WF voltage to 0.2 p.u.	$V_{dc,WF} > V_{dc,LV}$	V_{dc}-f_{WF} droop control	$V_{dc,WF} > 0$
WF	LVRT and reduce power output	$V_{t,WF} < V_{t,LV}$	f_{WF}-P_{WF} droop control	$f_{WF} > f_{WF0}$
DC Chopper	activated block	$V_{dc,RE} > V_{dc,LV}$ $V_{dc,RE} < V_{dc,rcv}$	activated block	$V_{dc,RE} > V_{dc,LV}$ $V_{dc,RE} < V_{dc,rcv}$

5.1. Case 1: Deep Voltage Drop in AC1

A three-phase grounding fault occurs between G1 and L1 in Figure 1 at t = 2 s, and the fault is cleared after 0.5 s. The system response results under different control strategies are plotted in Figure 1.

The frequency performance and voltage performance of AC1 are given in Figure 6a,b. The instant voltage drop is a deep drop level of more than 0.5 p.u. It can be seen that both the CCS and PCS can effectively provide frequency and voltage support during LVRT and recovery. Specifically, during the LVRT process, the voltage improvement with the PCS is nearly the same as that with the CCS, and it is not significantly improved compared with NAS. This is because, during LVRT, the reactive current control of the PCS and CCS are the same, while the current output of the converter is finite, and the AC terminal voltage is low when the fault occurs; hence, the maximum reactive power support from REVSC and BAVSC is also quite limited, further limiting the voltage improvement objectively.

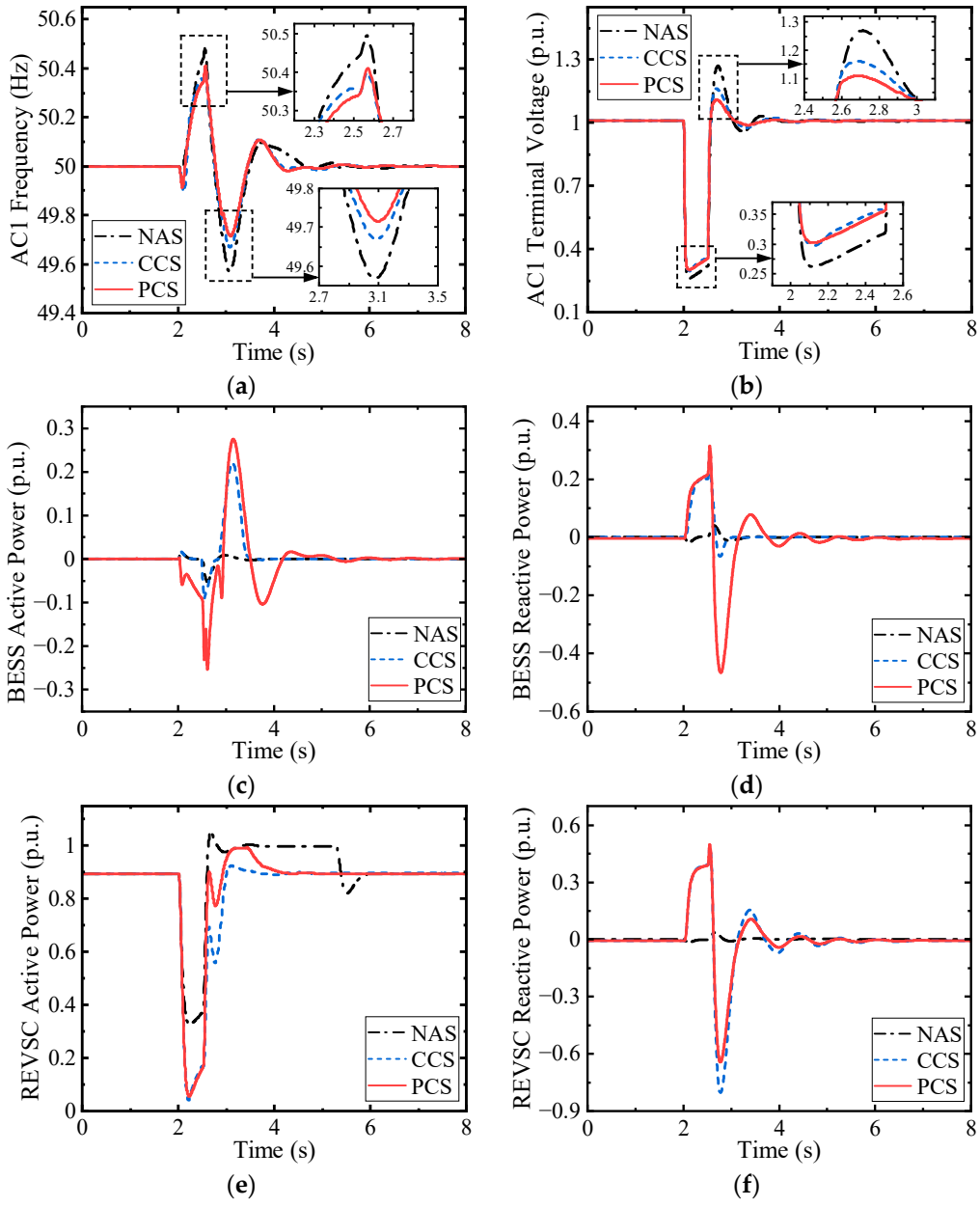


Figure 6. *Cont.*

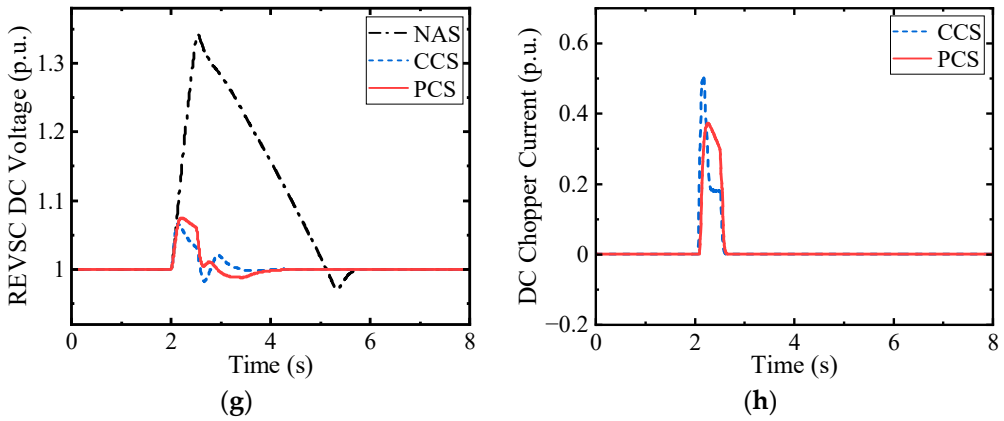


Figure 6. The simulation results for deep voltage drop in receiving-end system AC1. (**a**) The frequency in system AC1; (**b**) the terminal voltage in system AC1; (**c**) the active power output of the BESS converter; (**d**) the reactive power output of the BESS converter; (**e**) the active power output of the receiving-end converter; (**f**) the reactive power output of the receiving-end converter; (**g**) the DC voltage of the DC transmission line; (**h**) the current in DC chopper.

On the other hand, BAVSC is further enabled to absorb a certain active current in the PCS during LVRT, thus improving the frequency dynamics to some extent compared with the CCS, which is one of the contributions of the paper. Moreover, during the recovery process, the frequency and voltage dynamic improvement with the PCS is much better than that obtained with the CCS, augmenting the system recovery significantly. This is because the proposed P-Q coordination control in BAVSC under the PCS can adjust active and reactive currents dynamically according to the fluctuations in frequency and voltage; thus, the converter capacity can be fully utilized in comparison with the active current control in CCS.

As for the DC side, it can be seen from Figure 6g that both the CCS and PCS can avoid the DC overvoltage, and the CCS can maintain the DC voltage at a lower level during LVRT compared to the PCS. However, according to Figure 6h, the maximum DC chopper current under the PCS is about one-third lower than that under the CCS, which only requires electronic devices with a smaller rated current, hence reducing the cost.

5.2. Case 2: Light Voltage Drop in AC1

A three-phase grounding fault occurs between G2 and L2 in Figure 1 at t = 2 s, and the fault is cleared after 0.5 s. The system response results under different control strategies are plotted in Figure 1, where the instant voltage drop is a light drop level.

It can be seen from Figure 7a,b that the PCS can provide better frequency and voltage support than the CCS during both the LVRT and recovery processes. It should be noted that, since the fault is remote to the converter terminal, the voltage drop is not quite deep, so the REVSC active power transmission is not seriously affected. Hence, the power imbalance in the DC link does not lead to the DC voltage exceeding 1.05 p.u., as shown in Figure 7g, and power reduction is not activated from the sending-end systems nor the DC chopper under the CCS. On the contrary, it can be seen from Figure 7h that, under the PCS, AC2 and the WF will change the power output when the DC voltage changes in the LVRT process, so the imbalanced power can be reduced to some extent, and the DC voltage deviation can be suppressed. Meanwhile, during the recovery process, the DC voltage can further transmit frequency information, and AC2 and the WF can then participate in frequency support.

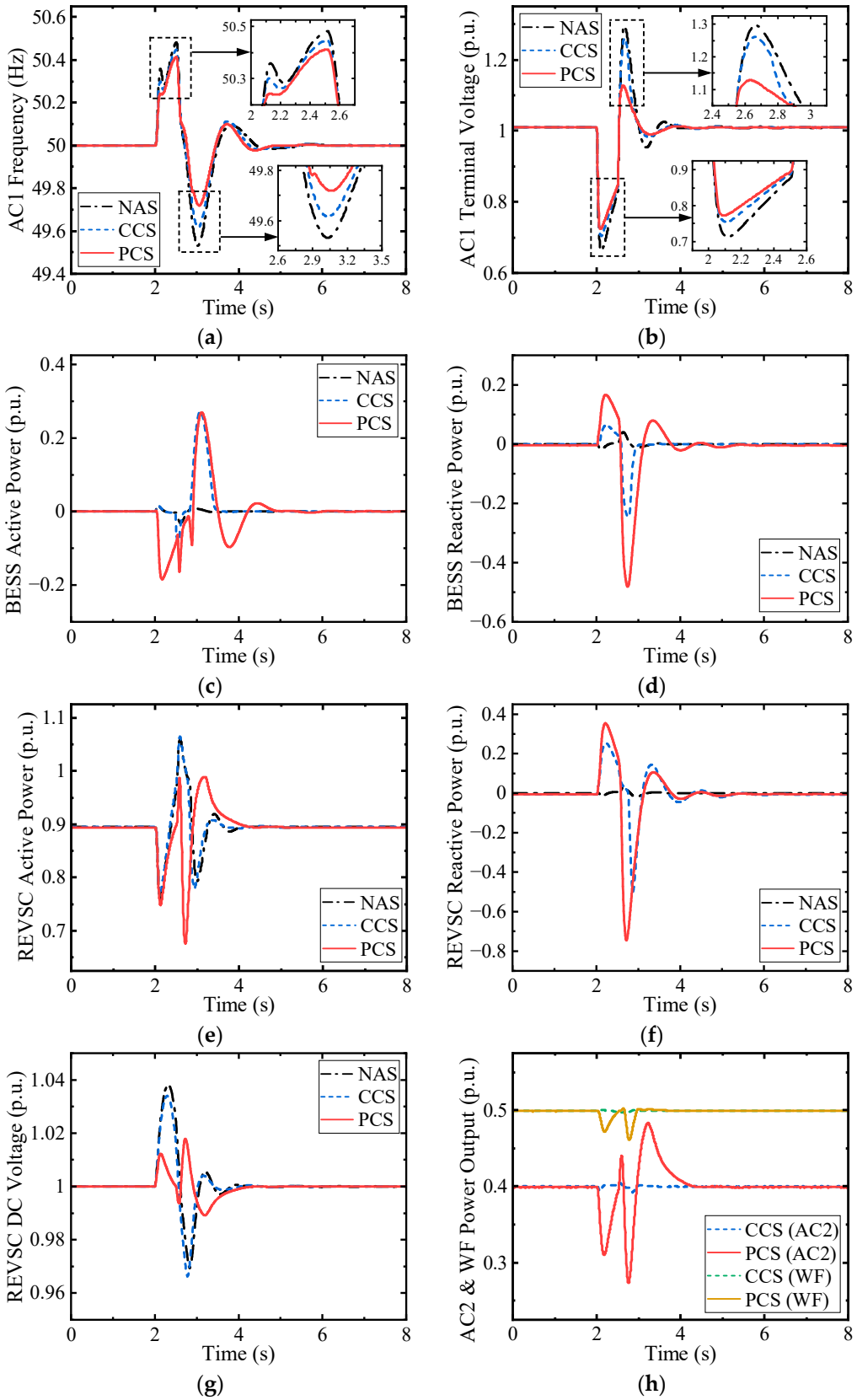


Figure 7. The simulation results for light voltage drop in receiving-end system AC1. (**a**) The frequency in system AC1; (**b**) the terminal voltage in system AC1; (**c**) the active power output of the BESS converter; (**d**) the reactive power output of the BESS converter; (**e**) the active power output of the receiving-end converter; (**f**) the reactive power output of the receiving-end converter; (**g**) the DC voltage of the DC transmission line; (**h**) the active power output of the sending-end system AC2 and WF.

5.3. Case 3: Deep Voltage Drop in AC2

The efficacy of the proposed control strategy for LVRT and its recovery when a grid fault occurs in the receiving-end system has been validated. In fact, the control rules of the receiving-end converter during the LVRT and recovery processes can also be adopted in the sending-end converter. To carry out the validation, the AC2 sending-end system can be modified, as shown in Figure 8, which consists of SGs G4–G6, load nodes L4–L6, and a local BESS1 connected with BAVSC1, and their parameters are the same as that of the SGs G1–G3, load nodes L1–L3, and BESS in AC1, respectively, as shown in Table A2. The control rules (12), (13), (15), and (16) and the hysteresis comparator for mode switch in REVSC have been adopted in SEVSC, and the control strategy for BAVSC has also been adopted in BAVSC1. A three-phase grounding fault occurs between G4 and L4 in Figure 8 at t = 2 s, and the fault is cleared after 0.5 s. The system response results under different control strategies are plotted in Figure 9.

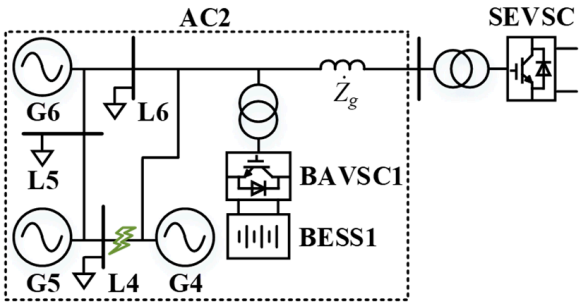


Figure 8. The diagram of the modified sending-end system AC2 with SGs, load nodes, and a BESS.

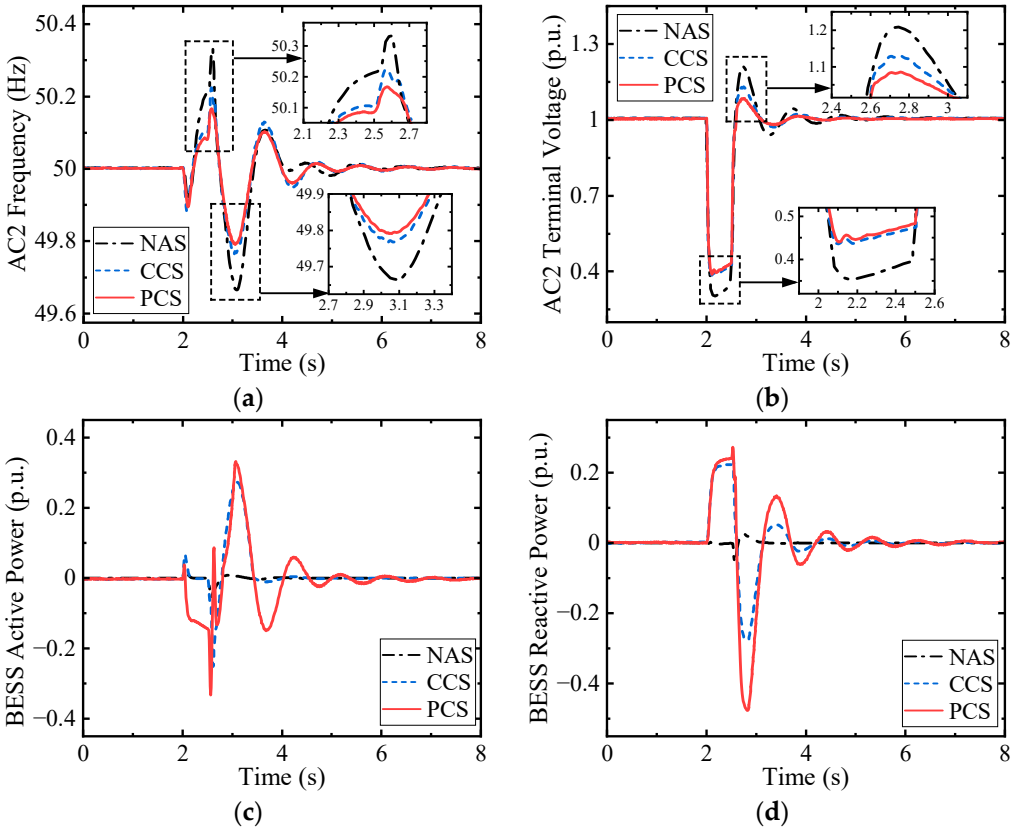


Figure 9. *Cont.*

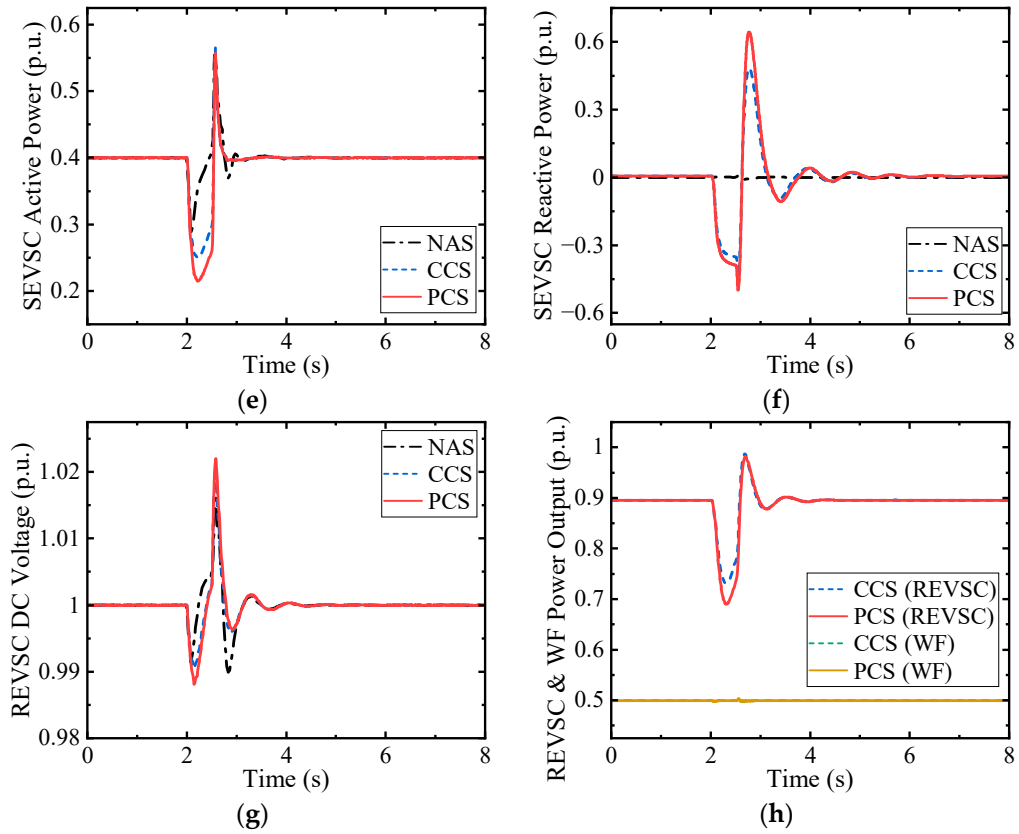


Figure 9. The simulation results for deep voltage drop in sending-end system AC2. (**a**) The frequency in system AC2; (**b**) the terminal voltage in system AC2; (**c**) the active power output of the BESS converter; (**d**) the reactive power output of the BESS converter; (**e**) the active power output of the sending-end converter; (**f**) the reactive power output of the sending-end converter; (**g**) the DC voltage of the DC transmission line; (**h**) the active power output of the receiving-end converter and WF.

It can be seen from Figure 9a,b that the PCS can also be adopted in the sending-end converter to enhance system frequency and voltage stability during both the LVRT and recovery processes. Note that there are some differences between the results in Cases 1 and 2 and Case 3. On one hand, since the fault occurs in the sending-end system, the reactive power flow of SEVSC, as shown in Figure 9f, is opposite to that of REVSC when the fault occurs in the receiving-end system, as shown in Figures 6f and 7f. On the other hand, the grid fault in AC2 results in a reduction in the SEVSC power output and a slight decrease in the DC voltage, as shown in Figure 9e,g. Therefore, according to the control rules, the DC chopper will not be activated, and the WF will maintain the initial power output, as shown in Figure 9h. This also means that only BESS1 provides frequency support, but there is no additional power support from the WF or AC1 during the recovery process.

6. Conclusions

In this paper, a P-Q coordination control strategy for VSC-MTDC system frequency and voltage performance enhancement during LVRT recovery is proposed, and the BESS plays a significant role in the whole process. During the LVRT process, the BESS as well as the receiving-end converter can provide reactive power injection as per the grid code, and the BESS can further absorb active power to suppress the frequency fluctuation and enhance system stability; additionally, the improved coordination sequence of the sending-end systems and DC chopper can not only effectively avoid DC overvoltage but also lower the requirement for electronic devices of the DC chopper. As for the recovery process, an adaptive current limitation method is proposed for the BESS converter to realize the dynamic adjustment of active and reactive powers with the coordination index and provide

frequency and voltage support accordingly; additionally, the receiving-end converter can control the DC voltage to transmit frequency information to the sending-end systems and enable them to participate in frequency regulation. The proposed control strategy can also be adopted in other system topologies, and the generalized control strategy for more operation conditions (such as high-voltage ride-through) will be studied in our future work.

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Appendix A

In the system, the base power, base AC voltage, and base DC voltage are 400 MVA, 220 kV, and 400 kV, respectively.

Table A1. The parameters of the converters and HVDC link.

Symbol	Item	Value	Symbol	Item	Value
S_{VSC}/p.u.	Rated VSC capacity (except BAVSC)	1	f_0/Hz	Rated system frequency	50
S_{BA}/p.u.	Rated BAVSC capacity	0.5	f_{WF0}/Hz	Rated WF frequency	50
V_{VSC}/p.u.	Rated VSC AC RMS voltage	0.909	L_T, R_T/p.u.	Transformer inductance and resistance	0.1, 0.005
S_{dc}/p.u.	Rated DC power	1	Z_g, θ_g/p.u.	Line impedance and angle	0.5, 80°
V_{dc0}/p.u.	Rated DC voltage	1	R_{DC}/p.u.	Resistor in DC chopper	3.03

Table A2. The parameters of SGs (G1–G3), loads (L1–L3), and BESS in the AC1 system.

Symbol	Item	Value	Symbol	Item	Value
$S_{G1/G2/G3}$/p.u.	Rated power	2.5, 2.5, 2.5	$T_{CH1/CH2/CH3}$/s	Turbine time constant	0.2, 0.2, 0.2,
$V_{G1/G2/G3}$/p.u.	Rated terminal voltage	1, 1, 1.	$P_{G1/G2/G3ref}$/p.u.	Initial power output	0.85, 0.78, 0.69
$H_{G1/G2/G3}$/s	Inertia time constant	6, 6, 6	$P_{L1/L2/L3}$/p.u.	Load	1+j0, 3.8+j0, 4.4-j1.2
$K_{G1/G2/G3}$	Droop coefficient	40, 40, 40	$P_{BA\max}$/p.u.	BESS maximum power	0.5
$T_{G1/G2/G3}$/s	Governor time constant	0.08, 0.08, 0.08			

Table A3. The parameters of SG and load in the AC2 system.

Symbol	Item	Value	Symbol	Item	Value
S_G/p.u.	Rated generator power	4.0	T_G, T_{CH}/s	Governor and turbine time constants	0.08, 0.2
V_G/p.u.	Rated terminal voltage	1.0	P_G/p.u.	Initial generator power output	3.6
H_G/s	Inertia time constant	8	P_L/p.u.	Initial load	3.2
K_G	Droop coefficient of generator	40	P_{SE0}/p.u.	Initial power reference of SEVSC	0.4

Table A4. The parameters of the wind farm.

Symbol	Item	Value	Symbol	Item	Value
S_n/p.u.	Rated DFIG power	2.778×10^{-3}	v_n/m·s^{-1}	Rated wind speed	12
P_n/p.u.	Rated active power	2.5×10^{-3}	H_{WT}/s	Inertia time constant	4.32
N_{wt}	Number of DFIGs	200	σ_m	Maximum power reduction ratio	0.2

Table A5. The control parameters of the converters and DC chopper.

Symbol	Item	Value	Symbol	Item	Value
K_{Bf}, K_{BV}	BAVSC power droop coefficients	20, 2	k_{pi}	Converter proportional gain of inner PI loop	0.3
K_V	REVSC voltage droop coefficients	5	k_{ii}	Converter integral gain of inner PI loop	10
K_P	SEVSC power droop coefficient	8	k_{po}	Converter proportional gain of outer PI loop	2
K_f	WFVSC frequency droop coefficient	0.2	k_{io}	Converter integral gain of outer PI loop	40
K_σ	WF power droop coefficient	10	$V_{t,LV}$, $V_{t,rcv}$	Hysteresis comparator thresholds in BAVSC and REVSC	0.9, 0.95
k_q	BAVSC and REVSC reactive current droop coefficient	2	$V_{dc,LV}$, $V_{dc,rcv}$	Hysteresis comparator thresholds in DC chopper control	1.05, 1.03
k_d	BAVSC active current droop coefficient	3	Δf_{db}, $\Delta V_{t,db}$	Frequency and voltage dead-band ranges of the BAVSC	0.001, 0.01

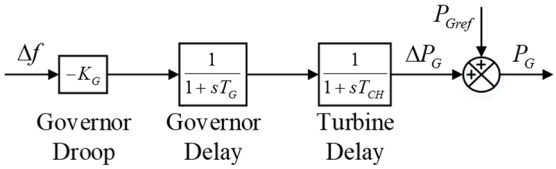

Figure A1. The diagram of the generator governor and turbine.

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