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Capacitor Voltage Balancing Control of MMC Sub-Module Based on Neural Network Prediction

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Abstract: The issue of sub-module (SM) capacitor voltage unbalance is a hot topic in the current research into the modular multilevel converter (MMC). An excellent strategy comprises mitigating the SM capacitor voltage imbalance by adjusting the SM on time. The traditional capacitor voltage balancing control regulates the speed to maintain accuracy. A unique SM capacitor voltage balancing control strategy is presented in this paper and is based on conventional capacitor voltage balance management and neural network prediction. Firstly, the SM capacitor voltage and arm current are speculated by operating the time series forecasting technique in real time, considering the dynamic changes in the SM capacitor voltage and arm current. Secondly, the SM capacitor voltage distinction between the actual and theoretical value is determined, and a deviation's mixed Gaussian distribution is established to estimate its compensation voltage. Thirdly, the SM triggering sequence is anticipated by using the neural network along with the pilot values of the SM capacitor voltage, arm current, and the offset compensation value, and the control is executed. Finally, a three-phase, six-leg, eight-module, nine-level MMC model is built to verify the feasibility of the suggested approach.

Keywords: capacitor voltage balance; time series prediction; Gaussian distribution; neural network



Citation: Xi, Q.; Tian, Y.; Fan, Y. Capacitor Voltage Balancing Control of MMC Sub-Module Based on Neural Network Prediction. *Electronics* **2024**, *13*, 795. <https://doi.org/10.3390/electronics13040795>

Academic Editor: Fabian Khateb

Received: 31 December 2023

Revised: 11 February 2024

Accepted: 14 February 2024

Published: 18 February 2024



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1. Introduction

The modular multilevel converter (MMC) represents the most recent iteration of voltage source converters. When operated, the converter's active and reactive power, voltage, and current can be modified independently, providing minimal loss and high-quality output voltage waveforms [1–4]. However, due to the diverse capacitor values of each sub-module (SM), the SM capacitor voltage deviates from the theoretical voltage during the inverter process, resulting in the SM capacitor voltage imbalance, leading to upper- and lower-bridge voltage fluctuations, increasing the circulating current between the bridges and reducing the DC voltage utilization.

As a result, a switching function model was used to analyze the coupling relationship between the SM electrical quantities [5] and the steady-state characteristics of the SM electrical quantities and design the main circuit's parameters. Meanwhile, according to the MMC structure, the bridge arm's instantaneous power equation was established [6] and revealed the existence of the second-harmonic component in the circulating current. According to the components of the circulating current, a generalized controller-based circulating current suppression strategy [7,8], reactive circulating current injection [9], is proposed, which incorporates the CPS-PWM modulation method to achieve the SM output voltage balancing, but increases the SM's switching frequency and loss. A guiding factor [10] and a balancing regulation index [11] are introduced to achieve a flexible trade-off between switching frequency and capacitor voltage balancing. At the same time, the disadvantages of the CPS-PWM modulation method are fully demonstrated and the use of carrier cascading is proposed, but the rotation period of the carriers will have an extremely important effect on the control. In addition, when carrier modulation is used, it is necessary to establish an independent capacitor voltage control circuit for each SM, which increases

the cost of the control link. Moreover, the extraction of the circulation component will directly affect the SM capacitor voltage balancing control, which improves the complexity of the control link.

The modulation method using nearest level approximation [12,13] is proposed to accomplish balanced control of SM capacitor voltages by conducting bubble sort [14], base sort [15], group sort [16], and subsumption sort [17] on the capacitor voltages, which reduces the effect of the output due to capacitor parameter differences. However, as the SM number increases, the computer's performance is required to be higher. It is not conducive to rapidly adjusting active and reactive power, voltage, and current.

All the above capacitor voltage balancing control strategies need to use specialized sensors, leading to a cost increase for capacitor voltage balancing control. For this purpose, Kalman filtering [18], state observer [19], and the online estimation of arm currents [20] are implemented to predict the arm currents. In addition, SM capacitor voltage balancing has been achieved by changing the SM topology, for instance, by adding diodes between neighboring SMs to form a self-homogenizing circuit [21–23]. The dynamic balancing of SM capacitor voltages is achieved by introducing flying capacitor multilevel (FCML) converters between adjacent SMs [24]. However, this increases the complexity of the SM topology and is not conducive to later expansion. Further, the SM capacitor voltage output interval was partitioned using a field-programmable gate array (FPGA) to achieve SM capacitor voltage dynamic balancing [25,26], improving its balancing control speed. Nevertheless, the interval division and the number setting of intervals will seriously affect the balancing control effect. If SMs were placed in the same output interval, the capacitor voltage balancing control would not be any better. The active and reactive power, voltage, and current could not be precisely controlled.

In practical engineering, it is necessary to regulate the speed at the cost when utilizing the above methods to satisfy the control accuracy. For this reason, using the traditional capacitor voltage balancing control strategy, the SM capacitor voltage, turn-on sequence, and arm current are regarded as the initial data. The MMC input and output parameters' fluctuation interval is divided into smaller segments. The SM capacitor voltage and arm current will evolve when the input and output parameters change. Consequently, the primary database is updated and supplemented. An SM capacitor voltage balancing control strategy based on neural network forecasting is proposed. Firstly, the SM capacitor voltage and arm current trends and periodicity are analyzed and tested. The time series method is used to predict the SM capacitor voltage and arm current in real time. Secondly, the SM capacitor voltage discrepancy between the actual and theoretical value is estimated, and its mean and variance are generated. We observe the deviation distribution, construct a mixed Gaussian distribution of the voltage offset, and evaluate the compensation value of the voltage offset. Thirdly, taking into account the historical data for the SM capacitor voltage and conduction sequence, the neural network is trained. Considering the predicted SM capacitor voltage, arm current, and deflection compensation value, the SM conduction sequence is predicted and the control is completed. Finally, a simulation model is developed to verify the feasibility of the proposed scheme.

2. Theoretical Analysis

During MMC operation, the SM capacitor parameters are not identical, which constitutes a primary factor in the SM output voltage imbalance. The SM capacitor voltage imbalance is a natural occurrence because of the disparity between the predicted time and the actual on-state time calculated via the modulation.

2.1. SM Capacitor Value Differences

MMC's basic unit is SM. Its standard structures include the half-bridge type and full-bridge type. In engineering, a half-bridge SM is commonly employed, consisting of two insulated gate bipolar transistors (IGBTs) and a capacitor, as demonstrated in Figure 1.

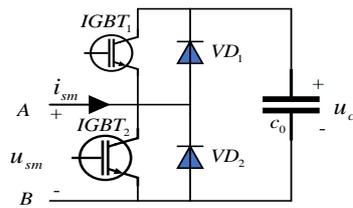


Figure 1. Basic structure of half-bridge SM.

$IGBT_1$ and $IGBT_2$ determine the SM capacitor C_0 charge or discharge. Assuming that i_{sm} is active from A to B and vice versa, if the potential of A is higher than that of B, then u_{sm} is active and vice versa. The values ‘1’ and ‘0’ indicate $IGBT$ conduction and shutdown, respectively. Then, the relationship between the on–off of $IGBT_1$ and $IGBT_2$, and the state of the SM capacitor C_0 is shown in Table 1.

Table 1. Relationship between the on–off of $IGBT_1$ and $IGBT_2$ and the state of the SM capacitor C_0 .

$IGBT_1$	$IGBT_2$	i_{sm}	SM Status	C_0	u_c
0	0	+	input	charge	u_{sm}
0	0	–	remove	bypass	0
1	0	+	input	charge	u_{sm}
1	0	–	input	discharge	$-u_{sm}$
0	1	+	remove	bypass	0
0	1	–	remove	bypass	0
1	1	+	remove	bypass	0
1	1	–	input	discharge	$-u_{sm}$

From Figure 1, we can see that if the SM initial voltage is u_0 , then the capacitor voltage u_c , instantaneous power p_c , and stored energy W_c meet the following relationship during a charging cycle:

$$u_c = \frac{1}{C_0} \int i_{sm} dt + u_0 \tag{1}$$

$$p_c = i_{sm} u_c \tag{2}$$

$$W_c = \int p_c dt = \int i_{sm} u_c dt \tag{3}$$

During operation, we suppose that the voltage and current are U_{dc} , I_{dc} at the DC side bus. In phase $j(j = a, b, c)$, the upper arm current is i_{jp} ; the number of on-state SMs is n_{pj} ; and the capacitor value, voltage, and stored energy of the i -th conducting SM are C_{pi} , u_{jpi} , and W_{jpi} , respectively. We draw the circuit diagram of phase j , as shown in Figure 2.

From Figure 2, we can see that the upper bridge j -phase capacitor voltage u_{jp} and the stored energy W_{jp} are

$$u_{jp} = \sum_{i=1}^{n_{pj}} u_{jpi} \tag{4}$$

$$W_{jp} = \sum_{i=1}^{n_{pj}} W_{jpi} \tag{5}$$

Similarly, according to Equations (4) and (5), the lower-bridge j -th phase capacitor voltage u_{jn} , and capacitor stored energy W_{jn} are received. If the SM initial voltages are all the same, at the t_i moment, SM_{pi} conducts, and the upper-bridge output voltage is U_i , and its variation is $U_i - U_{i-1}$ and remains constant. Taking a charge cycle of SM_{p1} as an example, the upper bridge j -phase output voltage u_{jp} varies, as shown in Table 2.

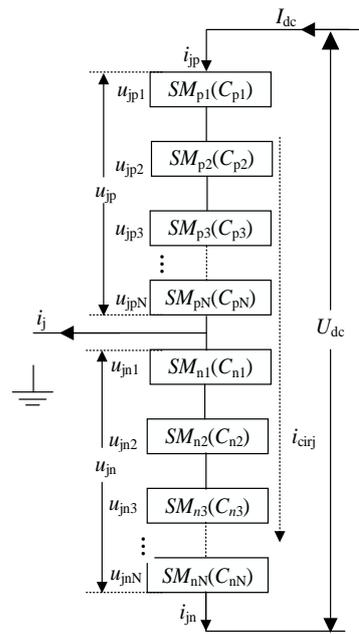


Figure 2. Circuit for phase j .

Table 2. The turn-on relationship between the output voltage u_{jp} and SM in the upper-bridge j -phase.

Time	u_{jp}	Voltage Variation	Upper-Bridge Conductive SM
0	0	0	0
t_1	U_1	U_1	SM_{p1}
t_2	U_2	$U_2 - U_1$	SM_{p1}, SM_{p2}
t_3	U_3	$U_3 - U_2$	$SM_{p1}, SM_{p2}, SM_{p3}$
...
t_{N-1}	U_{N-1}	$U_{N-1} - U_{N-2}$	$SM_{p1}, SM_{p2}, SM_{p3} \dots SM_{pN-1}$
t_N	U_N	$U_N - U_{N-1}$	$SM_{p1}, SM_{p2}, SM_{p3} \dots SM_{pN}$
t_{N+1}	U_{N-1}	$U_N - U_{N-1}$	$SM_{p2}, SM_{p3} \dots SM_{pN-1}, SM_{pN}$

Ideally, the SM capacitor values are equal and SM_{pi} conducts according to Table 2, making the voltage changes $U_i - U_{i-1}$ similar. In practice, due to capacitor production error or degradation, the SM capacitor values are not identical [27]. Suppose SM_{pi} is turned on according to Table 2. In that case, the actual value for the SM_{pi} capacitor voltage deviates from the theoretical value, which causes the difference between the real value of the output voltage u_{jp} and the theoretical value, resulting in the voltage changes $U_i - U_{i-1}$ being dissimilar to the upper-bridge j -phase output voltage u_{jp} , as shown in Figure 3.

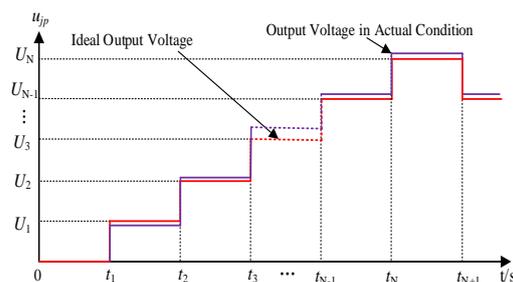


Figure 3. The variation in the output voltage u_{jp} on the j -th phase upper-bridge arm.

Similarly, if the lower-bridge SM capacitor values are not similar, then they cause discrepancies between the actual and theoretical values for the lower-bridge j -phase output voltage u_{jn} .

Combined with Figure 2, ideally, according to Kirchhoff's law:

$$u_{jn} + u_{jp} = U_{dc} \quad (6)$$

$$i_{jp} = i_j + i_{jn} \quad (7)$$

The circulating current i_{cirj} in phase j is

$$i_{cirj} = \frac{1}{2}(i_{jp} + i_{jn}) \quad (8)$$

Combining Equations (7) and (8), i_{jp} and i_{jn} are displayed:

$$i_{jp} = \frac{1}{2}i_j + i_{cirj} \quad (9)$$

$$i_{jn} = -\frac{1}{2}i_j + i_{cirj} \quad (10)$$

The output voltage u_j in phase j is

$$u_j = \frac{1}{2}(u_{jn} - u_{jp}) \quad (11)$$

If the SM capacitor values are not the same, then the actual value u_j deviates from the theoretical value, exacerbating u_j fluctuations.

If U_j is the j -th phase output voltage u_j fundamental voltage rms value on the AC side, then the output voltage modulation index m is

$$m = \frac{\sqrt{2}U_j}{0.5U_{dc}} = \frac{2\sqrt{2}U_j}{U_{dc}} \quad (12)$$

Then, the voltage utilization rate n is

$$n = \frac{\sqrt{6}U_j}{U_{dc}}m \quad (13)$$

In operation, assuming $u_j = \sqrt{2}U_j \sin(\omega t)$, $i_j = \sqrt{2}I_j \sin(\omega t + \varphi)$, then the output instantaneous power p_{out} in phase j is

$$p_{out} = u_j i_j = 2U_j I_j \sin(\omega t) \sin(\omega t + \varphi) \quad (14)$$

In phase j , the interphase circulating current i_{cirj} is

$$i_{cirj} = \frac{p_{out}}{U_{dc}} = \frac{\sqrt{2}m}{4} I_j [\cos \varphi - \cos(2\omega t + \varphi)] \quad (15)$$

Substituting Equation (12) into (15) yields

$$i_{cirj} = \frac{1}{3}I_{dc} - \frac{I_{dc}}{3 \cos \varphi} \cos(2\omega t + \varphi) \quad (16)$$

When the SM capacitor C_i is not equal, meaning that the equivalent capacitance decreases in each bridge, causing I_{dc} to increase, the circulating current i_{cirj} in the j -th phase is shown in Figure 4.

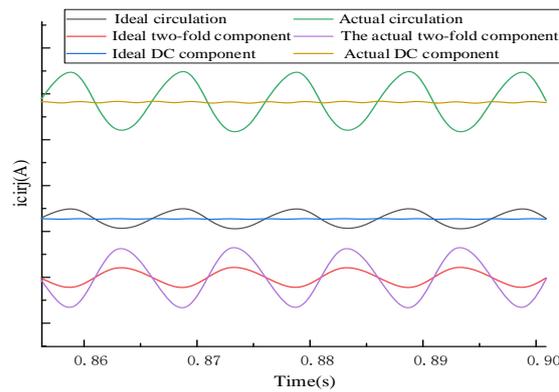


Figure 4. Circulating current i_{cirj} in phase j .

From Figure 4, we can see that the SM capacitor C_i is not the same, causing the circulating current i_{cirj} in the actual case to be larger than in the ideal case, making the output voltage modulation ratio m and the DC voltage utilization n smaller than in the ideal case.

2.2. Modulation Scheme

Currently, there are two main modulation methods for MMC: carrier pulse width and step-wave modulation. The carrier pulse width mainly compares the voltage-modulating waveform generated by the vector control link with the triangular carrier waveform to yield a modulating signal and perform the MMC triggering.

Nearest-level modulation (NLM) is commonly employed as step-wave modulation. According to the MMC’s control target, the voltage-modulated waveform is generated by using the vector control method; the number of SMs to be conducted in the upper and lower bridges is counted in real time so that the output voltage on the AC side comes close to the modulating waveform, which is often applied in flexible DC transmission projects because of its simple design, fast response, and wide range of applications. The NLM modulation diagram is shown in Figure 5.

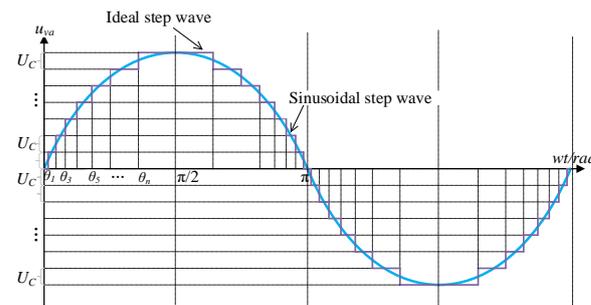


Figure 5. NLM modulation diagram.

From Figure 5, we can see that the step wave varies with the sinusoidal modulated wave and gradually approaches it. Each arm contains N SMs. Each SM has a capacitor value and voltage of C_0 and U_C , respectively. For phase j , the number of conductive SMs in the upper- and lower-bridge arms are n_{pj} and n_{nj} , separately. According to the modulation strategy, the number of conductive SMs n in each bridge meets $0 \leq n \leq N$. Then, n_{pj} , n_{nj} , satisfy the following relation:

$$n_{pj} + n_{nj} = N \tag{17}$$

Combined with Equation (6), the ideal value of the SM capacitor voltage U_C is

$$U_C = \frac{U_{dc}}{n_{pj} + n_{nj}} = \frac{U_{dc}}{N} \tag{18}$$

Whenever the NLM is used, the number of SMs on the upper and lower arms are

$$n_{nj}(t) = \frac{N}{2} + \text{round}\left(\frac{u_{vj}^*(t)}{U_c}\right) \tag{19}$$

$$n_{pj}(t) = \frac{N}{2} - \text{round}\left(\frac{u_{vj}^*(t)}{U_c}\right) \tag{20}$$

$u_{vj}^*(t)$ denotes the ideal modulating wave in the j -th phase at t time.

The SM capacitor voltage is positively related to its stored energy according to the bridge SM connection. We define the discharge rate K_i of the $SM_i (i = 1, 2, 3 \dots)$ as

$$K_i = \left| \frac{U_{1i} - U_{0i}}{t_{1i} - t_{0i}} \right| \tag{21}$$

U_{1i} and U_{0i} represent the $SM_i (i = 1, 2, 3 \dots)$ capacitor voltage U_i after conduction and before the on-time, respectively; t_{1i} and t_{0i} indicate the $SM_i (i = 1, 2, 3 \dots)$ after the on-time and the time before conduction, separately. For example, an MMC requires $SM_i (i = 1, 2, 3 \dots N)$ to conduct at t_0 moment, and the SM voltage is U_0 before it is on. According to the modulation principle of the NLM, the on-time is Δt . Then, ideally, the $SM_i (i = 1, 2, 3 \dots N)$ discharge diagram is shown in Figure 6.

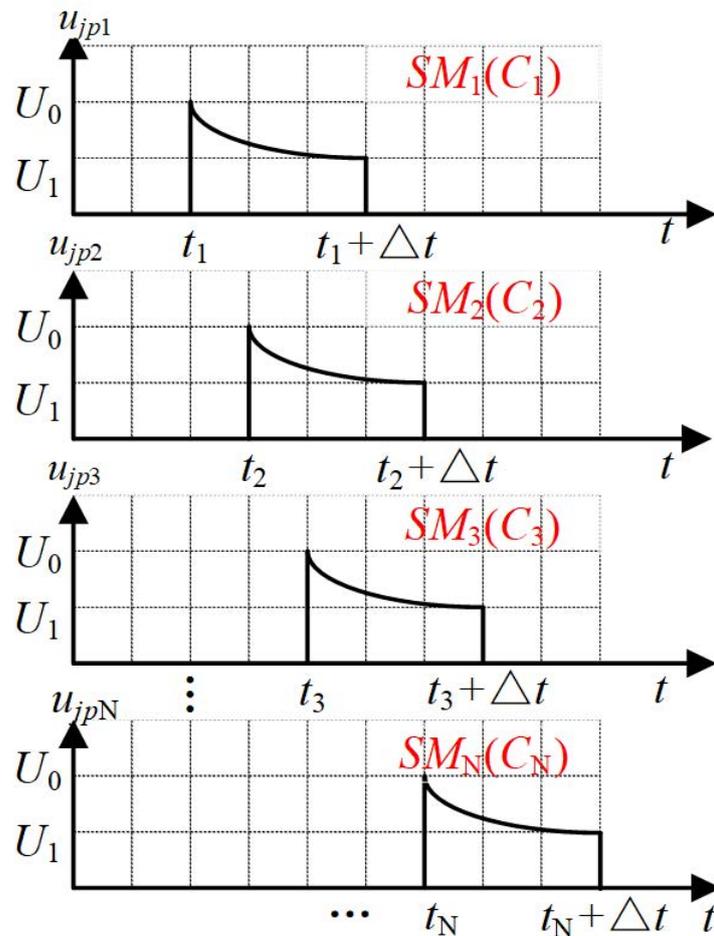


Figure 6. Ideally, the $SM_i (i = 1, 2, 3 \dots N)$ discharges schematically.

As seen in Figure 6, ideally, $C_1 = C_2 = C_3 = \dots = C_N$ causes the $SM_i (i = 1, 2, 3 \dots N)$ to have a matching discharge rate to K . After modulation, the $SM_i (i = 1, 2, 3 \dots N)$ still maintains equal capacitor voltage, the same discharge power, and balanced stored energy.

However, in actual engineering, the SM capacitor values are not exactly alike; for example, $C_1 \neq C_2 \neq C_3 = \dots = C_N$. At this time, according to the theoretical on-time Δt , the actual $SM_i(i = 1, 2, 3 \dots N)$ discharge schematic is shown in Figure 7.

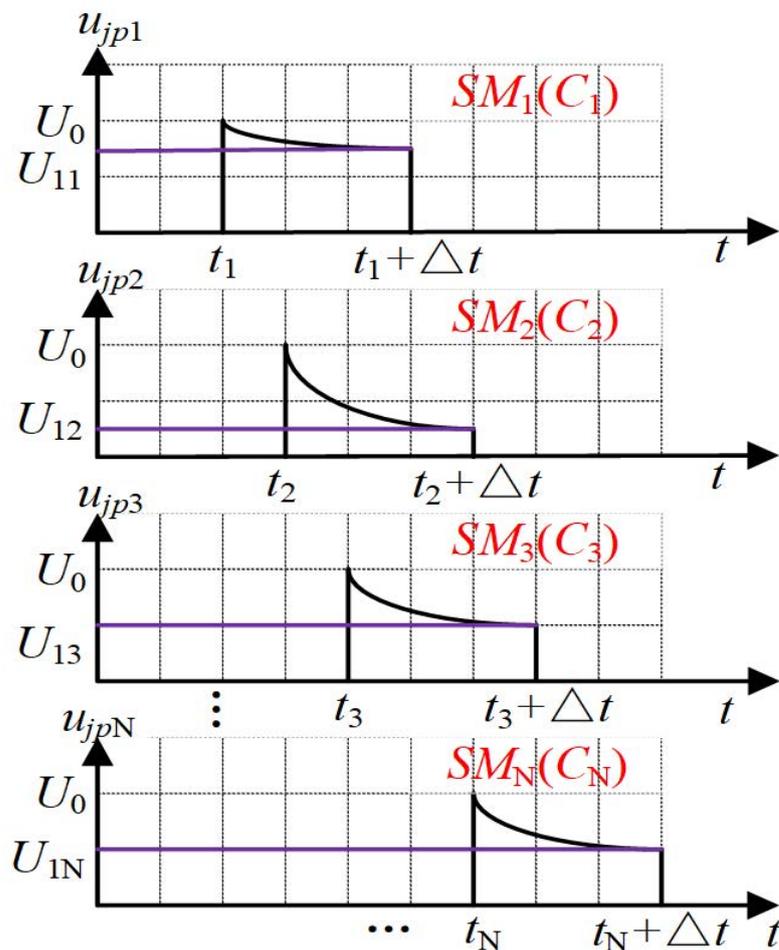


Figure 7. The $SM_i(i = 1, 2, 3 \dots N)$ discharge schematic diagram for the actual case.

Comparing Figures 6 and 7, $C_1 \neq C_2 \neq C_3 = \dots = C_N$ causes the $SM_i(i = 1, 2, 3 \dots N)$ discharge rate $K_1 < K_3 = \dots < K_N < K_2$ in practice. If the $SM_i(i = 1, 2, 3 \dots N)$ is discharged according to the theoretically figured on-time Δt , making the $SM_i(i = 1, 2, 3 \dots N)$ capacitor voltage $U_{1i}(i = 1, 2, 3 \dots N)$, then the discharging power P_{1i} and the stored energy W_{1i} are not exactly alike after the on-time, triggering the SM_2 to over-discharge and vibrate. Similarly, if the $SM_i(i = 1, 2, 3 \dots N)$ is charged according to the theoretically reckoned on-time, it will induce some SMs to store energy excessively.

In engineering, the SM capacitor values $C_1 \neq C_2 \neq C_3 \neq \dots \neq C_N$ prompt the $SM_i(i = 1, 2, 3 \dots N)$ to charge and discharge at entirely different rates K_i . The $SM_i(i = 1, 2, 3 \dots N)$ on-time theoretical time Δt_{1i} differs from the conduction Δt_i calculated by the NLM modulation strategy. After modulation, the SM capacitor voltage deviates from the theoretical value, resulting in unequal energy stored in the different SM capacitors, inducing some SMs to be overcharged and discharged, and reducing the SMs' service life.

3. Traditional SM Capacitor Voltage Balancing Control

In engineering applications, the NLM modulation strategy requires the collaboration of SM capacitor voltage sequencing to decline the bridge SM capacitor voltage imbalance. The specific control process is shown in Figure 8.

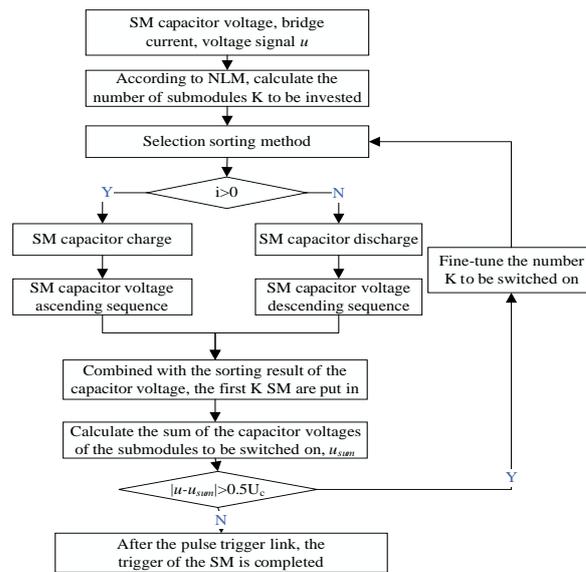


Figure 8. Traditional capacitor voltage balancing control.

The number of arm SMs, to-be-conducted SMs, and sequencing times are all interconnected, as demonstrated in Figure 9.

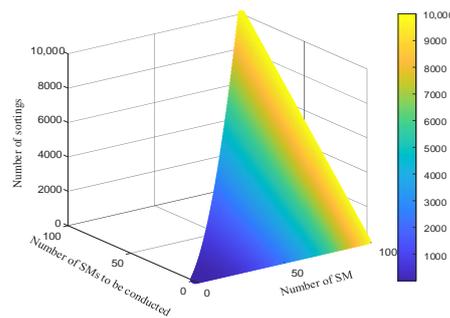


Figure 9. Relationship between the number of bridge SMs, to-be-conducted SMs, and ordering counts.

From Figures 8 and 9, it can be seen that the number of sequencing times is positively correlated with that of bridge SMs and to-be-conducted SMs.

4. Presentation Methodology

Upon investigation, it was discovered that each bridge in the ± 500 kV Yanqing converter station of the Zhangbei Flexible HVDC Transmission Project contains 264 SMs [28,29]. During operation, relying on multiple sensors to gather the output voltage and bridge current from each SM in real time is essential. Furthermore, the complexity of voltage balancing control is evidently increased by employing the traditional sorting algorithm, highlighting the higher requirements for the controller’s performance. If we suppose that the predictive method is used to derive every SM capacitor voltage and bridge current, then, by doing so, the sensor’s measurement delay and number can be shortened, and the system’s cost can be decreased. The deviation between the actual and theoretical values of capacitor voltage is estimated, a mixed Gaussian distribution with voltage deviation is constructed, and the predicted voltage is compensated to reduce the capacitor voltage deviation. The neural network is utilized to predict the SM triggering sequence and complete the activation to enhance the SM capacitor voltage balancing control speed.

4.1. Time Series Prediction

The time series method is introduced to predict the SM capacitor voltage and arm current. The forecasting model changes with MMC’s operating status variation. When the

MMC operates steadily, the SM capacitor voltage and arm current are periodic, and the auto-regressive (AR) model is invoked. Conversely, the auto-regressive integrated moving average (ARIMA) model is required. The estimation procedure for the SM capacitor voltage is shown in Figure 10.

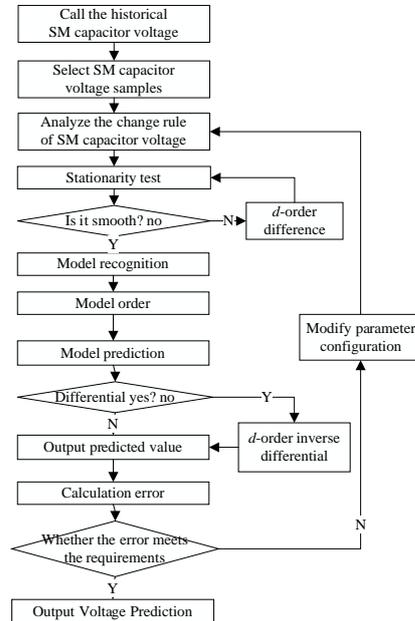


Figure 10. Prediction process for SM capacitor voltage.

As shown in Figure 10, when the time series prediction method is exploited, it is crucial to ensure that the SM capacitor voltage and arm current are stable. The time series $u_c(t)$ is generated from the SM capacitor voltage’s historical record value, and the smoothness test is performed. If the steadiness is not satisfied, then a new sequence $u_{c1}(t)$ is formed to meet the stability requirement by implementing d -order differences. Assuming the period $T = 0.02$ (s), the time series $u_{c1}(t)$ is examined to ascertain whether it conforms to the following equation:

$$u_{c1}(t) = u_{c1}(t - Tk)(k = 1, 2, 3 \dots) \tag{22}$$

If the time series $u_{c1}(t)$ satisfies Equation (22), the MMC is operating steadily. The AR model is invited to determine its order by combining the Akaike information criterion (AIC) and the Bayes information criterion (BIC). The specific AIC and BIC criteria are as follows:

$$AIC(k) = 2k - 2\ln(L) \tag{23}$$

$$BIC(k) = k\ln(n) - 2\ln(L) \tag{24}$$

Here, k is the number of parameters or the order of the model; n is the number of samples; and L is the likelihood function of the sample composition.

If we suppose the sampling time $T_1 = 0.000002$ (s), then the SM capacitor voltage predicted value $u_{c1}(t + T_1)$ is

$$u_{c1}(t + T_1) = \sum_{i=1}^n k_i u_{c1}(t + T_1 - iT) \tag{25}$$

In Equation (23), k_i satisfies the following relationship:

$$\sum_{i=1}^n k_i = 1 \tag{26}$$

If the time series $u_{c1}(t)$ does not satisfy Equation (22), then an ARIMA model is established, which means that MMC is working in an unstable state. Then, the order p and q are determined, respectively, by the autocorrelation function (ACF) and partial autocorrelation function (PACF). According to the auto-regressive moving average (ARMA) model, the prediction of the stationary sequence $u_{c1}(t + T_1)$ is completed:

$$u(t + T_1) = \varphi_0 + \sum_{i=1}^p \varphi_i u_{c1}(t - iT_1) \tag{27}$$

$$l(t + T_1) = \varepsilon(t) + \sum_{i=1}^q \theta_i \varepsilon(t - iT_1) \tag{28}$$

$$u_{c1}(t + T_1) = u(t + T_1) + l(t + T_1) \tag{29}$$

Here, φ_i is an autoregressive coefficient; θ_i is a moving average coefficient; and $\varepsilon(t_i)$ is a random disturbance in this term.

Finally, the SM capacitor voltage $u_c(t + T_1)$ is found via the d -order inverse difference of the stationary sequence $u_{c1}(t + T_1)$. The arm current $i(t + T_1)$ can be obtained utilizing the aforementioned method. We define the prediction error h as

$$h = \frac{|pr - tr|}{tr} \times 100\% \tag{30}$$

Here, pr and tr represent the predicted and actual values, respectively.

According to Equation (30), the SM capacitor voltage and arm current prediction inaccuracy are revealed.

4.2. Constructing Mixed Gaussian Distributions

In actual operation, the SM capacitor parameters are not the same, making the SM charging and discharging rates differ, resulting in a deviation between the virtual and theoretical values for the capacitor voltage and causing an imbalance in the SM stored energy. Therefore, assessing the capacitor voltage error is necessary to establish a mixed Gaussian deviation distribution and estimate the deviation compensation value. The construction process for the mixed Gaussian distribution is shown in Figure 11.

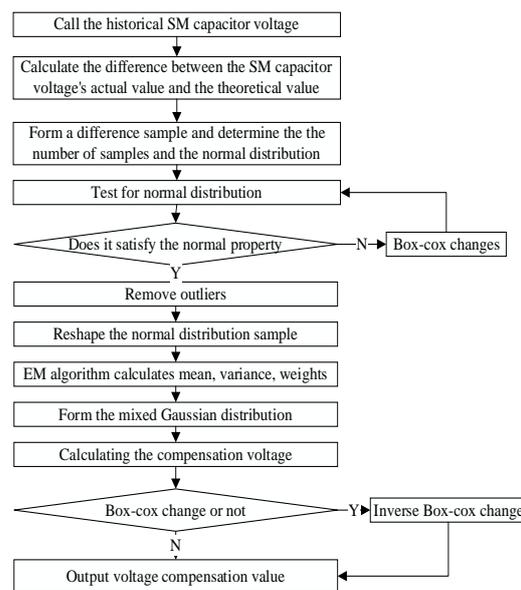


Figure 11. Construction of the mixed Gaussian distribution for the SM capacitor voltage deviation.

From Figure 11, it can be seen that, firstly, it is vital to perform a standard distribution test (Jarque-Bera test, jbstest) [30] on SM capacitor voltage deviation samples, compute the skewness and kurtosis of this offset, and fabricate the JB statistic:

$$skewness = E \left[\left(\frac{X - \mu}{\sigma} \right)^3 \right] \tag{31}$$

$$kurtosis = E \left[\left(\frac{X - \mu}{\sigma} \right)^4 \right] \tag{32}$$

$$JB = \frac{n}{6} \left[S^2 + \frac{(K - 3)^2}{4} \right] \tag{33}$$

According to Equations (31)–(33), the corresponding probability (p) is produced and compared with the set significance level (α) if $p > \alpha$, indicating that the deviation satisfies the normal distribution. Conversely, it is necessary to use the Box–Cox transformation to contend the normal distribution. The specific transformation rules are as follows:

$$y(\lambda) = \begin{cases} \frac{x^\lambda - 1}{\lambda}, \lambda \neq 0 \\ \ln x, \lambda = 0 \end{cases} \tag{34}$$

Here, represents the variation parameter. If the error $x < 0$, then it is important to add the deviation x to the constant c and continue Equation (34).

Secondly, the outliers are eliminated based on the significance level (α), and the Gaussian samples are reshaped by combining the calculated means so that the number of samples in each Gaussian distribution is the same. Thirdly, each Gaussian distribution’s mean and variance and their corresponding weights are received by using the expectation–maximization algorithm (EM) to form the mixing Gaussian distribution at the i -th moment, as shown in Figure 12. Finally, the compensated value of the SM capacitor voltage deviation is determined by employing the mixed Gaussian distribution.

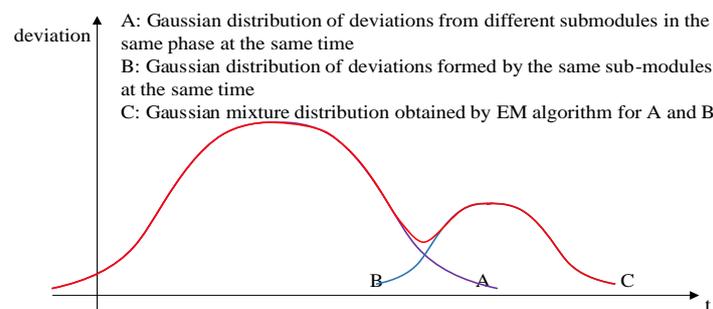


Figure 12. Mixed Gaussian distribution at i moment.

4.3. SM Trigger Sequence Prediction

Figure 9 shows that the traditional voltage balance control strategy largely depends on the sorting results for SM capacitor voltage. The time consumption of traditional voltage balancing control increases as the number of SMs grows, resulting in an apparent enlargement in the complexity of the sorting algorithm. When the neural network is applied in the SM capacitor voltage balance control link, it can not only achieve the goal of predicting the SM triggering sequence but also raise the MMC’s response speed. Its model is shown in Figure 13, below.

In Figure 13, $X_i(k - a)$ ($a = 1, 2, 3, \dots, m$) and $Y_i(k)$ denote the a -th input and the k -th output from the i -th sample, respectively. In the neural network, $X_i, W_{nm}^{(1)}, W_n^{(2)}, Y_i$ are represented as shown in Table 3, below.

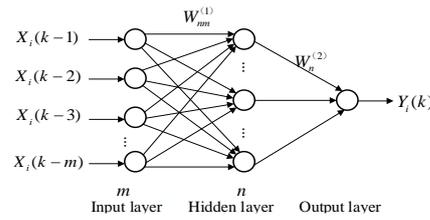


Figure 13. The model of the neural network.

Table 3. Different letter sizes in neural networks and their meanings.

Matrix	Size (Rows × Columns)	Connotation
X_i	$m \times 1$	The i -th input sample
$W_{nm}^{(1)}$	$n \times m$	Input layer to hidden layer weights
$W_n^{(2)}$	$n \times 1$	Weighting of hidden layers to output layers
Y_i	$k \times 1$	Output generated by the neural network for the i -th sample

It is assumed that the actual output and the computed output of forward propagation from the i -th training sample are Q_i and Y_i , respectively. Then, the error e_1 is

$$e_1 = Q_i - Y_i \tag{35}$$

The relationship between the calculation error e_1 and the setting error e_{ref} is

$$e_{ref} > |e_1| \tag{36}$$

If Equation (36) holds, it means that the neural network training meets the requirements. Therefore, the threshold B_1 of the neural network hidden layer neurons, the weight W_1 from the input layer to the hidden layer, the threshold B_2 of the output layer neurons, and the weight W_2 from the hidden layer to the output layer are saved. Conversely, back-propagation is performed, and B_1 , W_1 , B_2 , and W_2 are updated using the learning factor α . The specific update rules are

$$W_1 = W_{1_{t-1}} + \alpha \left((1 - b_1) (e_1' W_2)' \right) X_i' \tag{37}$$

$$B_1 = B_{1_{t-1}} + \alpha b_1 (1 - b_1) (e_1' W_{2_{t-1}})' \tag{38}$$

$$W_2 = W_{2_{t-1}} + \alpha e_1 b_1' \tag{39}$$

$$B_2 = B_{2_{t-1}} + \alpha e_1 \tag{40}$$

Here, $W_{1_{t-1}}$, $B_{1_{t-1}}$, $W_{2_{t-1}}$, and $B_{2_{t-1}}$ represent W_1 , B_1 , W_2 , and B_2 , respectively, at the previous moment. b_1 indicates the hidden layer output of the neural network, and its value is

$$b_1 = \frac{1}{1 + e^{-(W_1 X_i + B_1)}} \tag{41}$$

When the neural network is used to estimate the SM trigger sequence, firstly, a timetable named “SM capacitor voltage—conduction sequence” is built based on the SM conduction sequence history; secondly, the neural network is operated to train the timetable, so that the accepted conduction sequence can be close to the actual SM conduction order. Finally, a “multiple-input–single-output” anticipating model is generated and merged with the latest collected SM capacitor voltages to complete the SM conduction sequence prediction; the specific flow is shown in Figure 14.

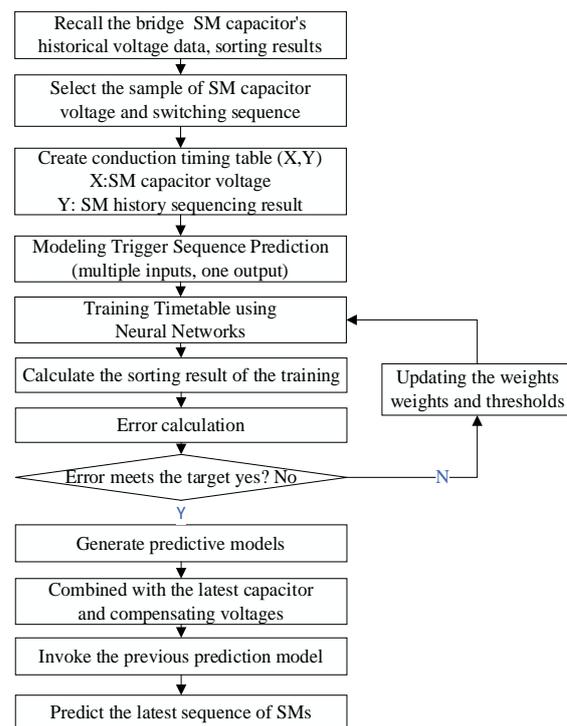


Figure 14. Neural network predicts the SM's conduction sequence.

Figure 14 shows a strong correlation between the selected SM conduction sequence samples and the neural network's forecasting precision. Depending on whether the training sample N fluctuates, the prediction method is further separated into fixed data sample prediction, fixed timescale prediction, and variable timescale prediction.

5. Simulation Results

Firstly, the MMC model with three phases, six bridges, and eight SMs is built in Matlab/Simulink. Together with the MMC control target, the NLM modulation strategy is used to perform the SM capacitor voltage balancing control by combining the bubbling method.

Secondly, the SM capacitor voltage, arm current, and conductance sequence are recorded in real time under the traditional voltage balancing control strategy.

Thirdly, time series prediction, grey prediction, Gaussian prediction, exponential smoothing, and other approaches are exploited to predict the SM capacitor voltage and arm current. The above methods' forecasting precision and time delay are measured and compared.

Finally, the mixed Gaussian distribution of the voltage deviation is produced, and its compensation value is computed. The SM trigger sequence is determined and completed by manipulating the neural network. The feasibility of the prediction method is verified via simulation.

Taking the passive inverter as an example, when the MMC is operating in the inactive inverter state, the parameters of the MMC are configured, as shown in Table 4, below.

Table 4. Parameter configuration of MMC working in the passive inverter state.

Parameter	Symbol	Unit	Numerical Value
Number of SMs per bridge	n	Individual	8
Size of each SM capacitor	C_n	μF	0.11
Bridge reactor size	L_n	mH	0.08
Output resistance	R	Ω	5000
Output inductance	L	H	1×10^{-5}
Initial input voltage	U_{dc0}	kV	6.52

Table 4. Cont.

Parameter	Symbol	Unit	Numerical Value
Input voltage after change	U_{dc1}	kV	8
Output phase voltage amplitude before change	u_{a0}	kV	2.85
Output phase voltage amplitude after change	u_{a1}	kV	3.5

5.1. Voltage and Current Prediction

When the MMC operating parameters are not changed, the SM capacitor voltage variation curve, the arm current variation curve, and their prediction curve are as shown in Figure 15.

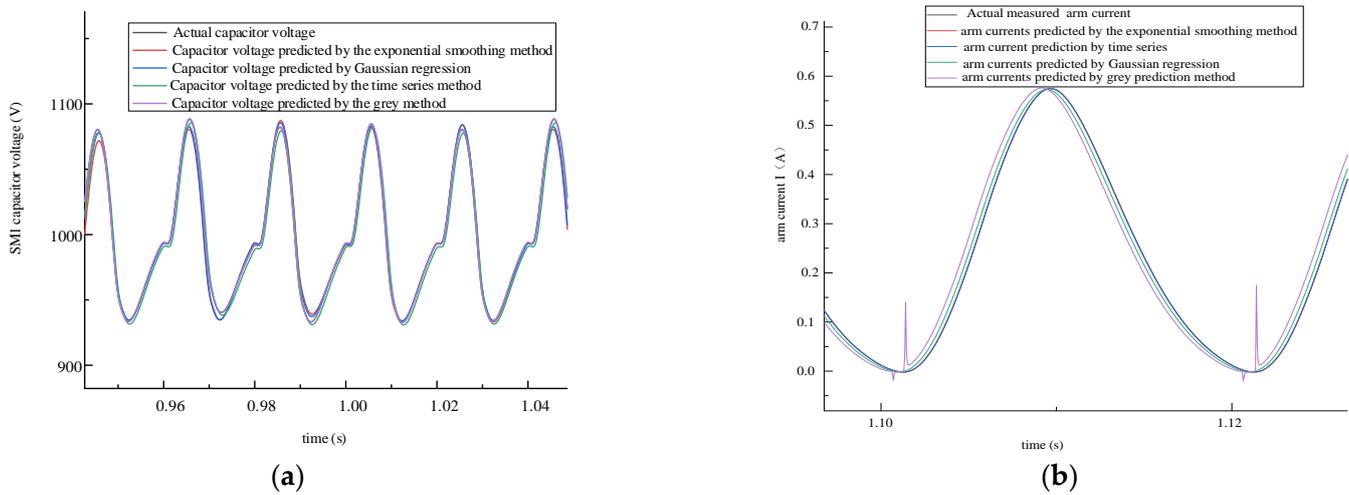


Figure 15. SM capacitor voltage, arm current variation curve, and their prediction curve. (a) SM capacitor voltage variation curve. (b) Arm current variation curve.

When the MMC operating parameters are changed, the SM capacitor voltage variation curve and its prediction curve are as shown in Figure 16.

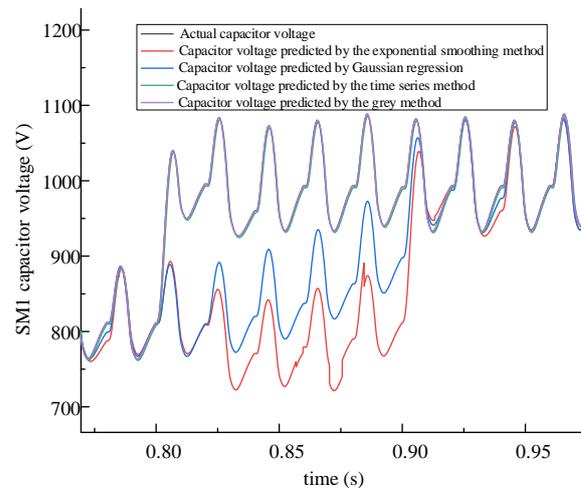


Figure 16. SM capacitor voltage variation curve and its prediction curve.

Combined with Equation (28), different methods' prediction delay and accuracy are evaluated, respectively, as shown in Table 5.

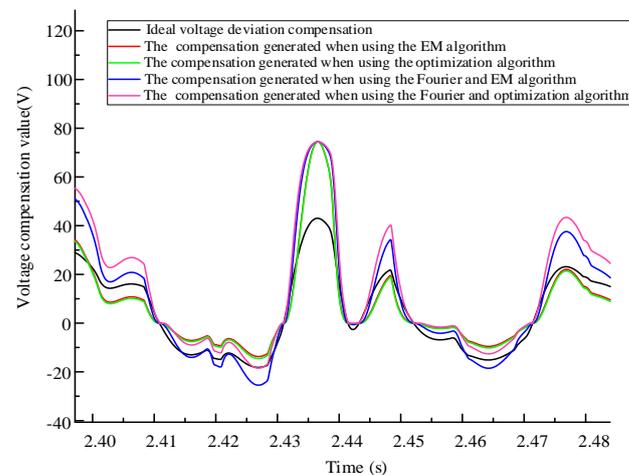
Table 5. Prediction delay and error of different methods.

Access Method		Time Delay (ms)	Error
Measurement devices	Hall sensor	0.01	1.0%
	PCB sensor	0.015	0.2%
	Analog-to-digital converter	/	0.2%
	Voltage controlled oscillator	/	0.2%
Predictions	Time series prediction	0.0001	0.19%
	Grey prediction	8	0.02%
	Gaussian predictions	80	0.5%
	Exponential smoothing prediction	0.0015	0.7%

According to the standard, the devices' measurement accuracy reaches 0.2 grade [31,32]. The PCB sensor is frequently employed to convey real-time voltage and current in the power system [29]. Two methods are reported in the literature to collect the SM capacitor voltage: the analog-to-digital converter and voltage-controlled oscillator [33]. Comparing Table 5, when the time series prediction tool is utilized, its time delay is much lower than the measurement delay of the PCB sensor. Meanwhile, the time series estimation approach meets practical engineering requirements.

5.2. Constructing Mixed Gaussian Distributions for Voltage Deviations

Under the conditions in Table 4, the offset voltage is formed and its compensation value is counted separately, as shown in Figure 17, below.

**Figure 17.** SM capacitor voltage deviation compensation values with different methods.

As shown in Figure 17, when the mixed Gaussian distribution of voltage offset is fabricated using the EM algorithm and the sampling frequency, its received compensation voltage amount is closest to the ideal voltage deviation compensation amount. Then, the deviation compensation effect is as shown in Figure 18.

5.3. SM Trigger Sequence Prediction

When the neural network is manipulated to predict the SM trigger sequence, its prediction accuracy and speed are easily influenced by the number of hidden layer neurons and the training samples when the training, validation, and test sets meet different proportions, as shown in Table 6.

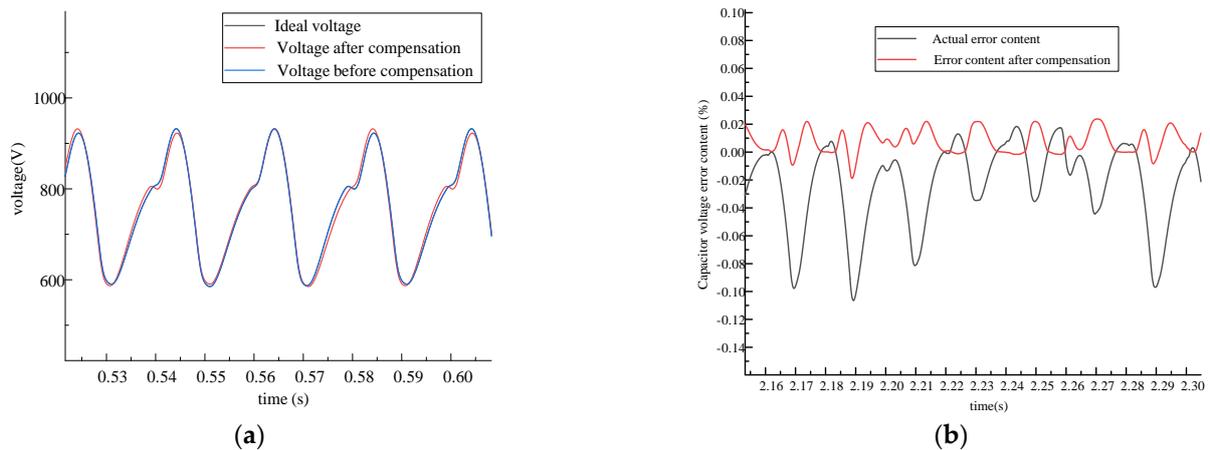


Figure 18. Before and after compensation, the SM capacitor voltage compensation effect and its error comparison. (a) SM capacitor voltage compensation effect. (b) Error content before and after compensation.

Table 6. Different proportions of the training, validation, and test sets.

Different Proportions	Training Set	Test Set	Validation Set
A	70%	15%	15%
B	80%	10%	10%
C	80%	15%	5%
D	90%	5%	5%

A bar graph represents the training set’s accuracy, and a line graph reflects the test set’s accuracy. At this point, the relationship between the accuracy (%) of its training set and the hidden layer neuron number of the neural network varies, as shown in Figure 19, below.

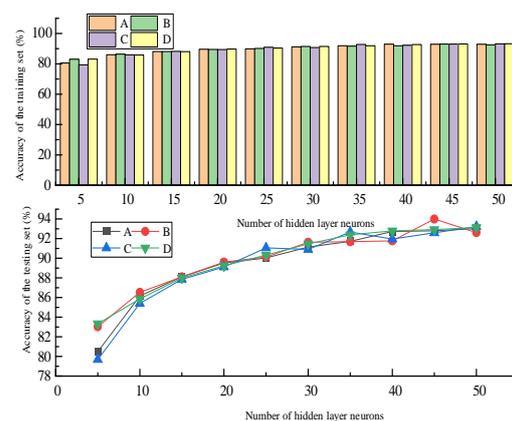


Figure 19. Relationship between the accuracy (%) of the training set and the number of neurons in the neural network’s hidden layer on different scales.

Figure 19 indicates that the neural network forecast accuracy will fluctuate drastically when the training, validation, and test sets encounter different proportions. In particular, when the training, validation, and test sets are 90%, 5%, and 5%, respectively, there is an excellent linear relationship between the neural network prediction accuracy and the number of neurons in the hidden layer. When the number of hidden layer neurons is greater than 40, the accuracy of the training, validation, and test sets gradually slows down. Meanwhile, its mean-square-error variation is shown in Figure 20, below.

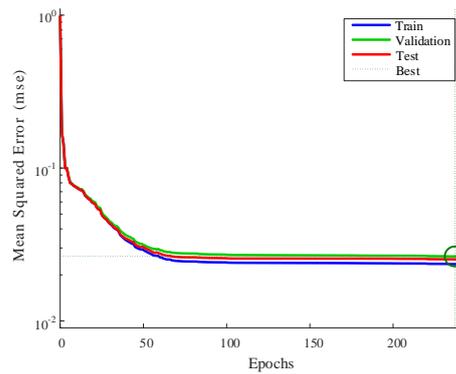


Figure 20. Variation in the mean square error.

It can be seen from Figure 20 that with an increasing number of iterations, the mean square error of the training set gradually decreases. At 237 iterations, the mean square error is the smallest. Therefore, in this prediction mode, the number of hidden layer neurons and iterations is 40 and 300, respectively.

When the neural network is employed to predict the SM conduction sequence, the parameter configuration of the neural network is as shown in Table 7, below.

Table 7. Parameter configuration of the neural network.

Parameters	Input	Implicit Layers	Output	Input	Implicit Neurons	Output	Iterations	Error	Activation Function
Size	8	1	1	1	40	1	300	1	Sigmoid

In addition, the prediction method also exerts an essential impact on the forecast accuracy and speed of the neural network. When the neural network uses the fitting approach for estimation, the SM trigger sequence is shown in Figure 21, below.

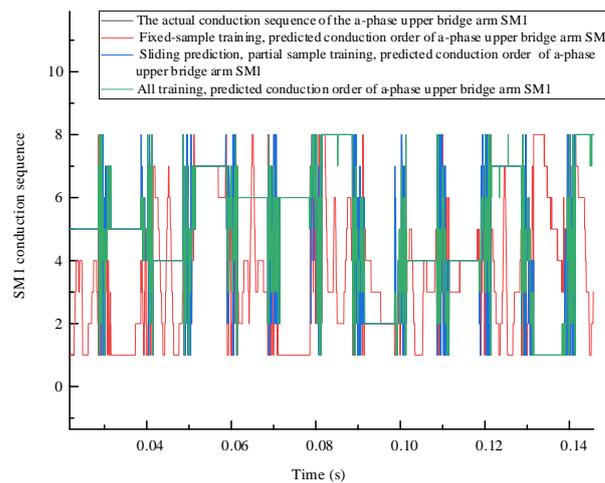


Figure 21. Neural network predicting the conduction order of SM via fitting under different sample training options.

When the neural network uses the classification approach for prediction, the SM trigger sequence is shown in Figure 22, below.

Combining Figures 21 and 22, the neural network forecast accuracy is assessed for various training samples using different methods to predict the SM conduction order, as shown in Table 8.

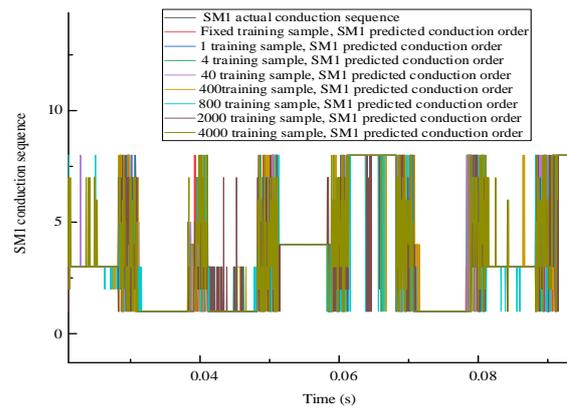


Figure 22. Neural network predicting the conduction order of SM via classification under different sample training options.

Table 8. Prediction accuracy and speed of SM trigger sequence.

Prediction Methodology		Sample Space	Iterations	Control Link Steps	Prediction Accuracy	
Classification prediction	Fixed data sample	/	0	13	83.53%	
	Variable data samples (random initialization)	The sample scale is 1	1	1	31	85.63%
		The sample scale is 4	4	3	157	83.75%
		The sample scale is 40	40	9	3685	82.58%
		The sample scale is 400	400	21	84,181	81.98%
		The sample scale is 800	800	30	240,253	82.02%
		The sample scale is 2000	2000	40	800,333	79.26%
		The sample scale is 4000	4000	56	2,240,461	80.38%
	Variable data samples (fixed initialization)	The sample scale is 1	1	1	31	85.65%
		The sample scale is 4	4	3	157	83.69%
		The sample scale is 40	40	6	2461	82.60%
		The sample scale is 400	400	7	28,069	82.22%
		The sample scale is 800	800	8	64,077	82.13%
		The sample scale is 2000	2000	10	200,093	79.06%
Fitting prediction	Fixed data sample	/	0	13	43.34%	
	Fixed timescale	4000	45	1,800,373	60.56%	
	Variable timescale	/	/	/	80.71%	

As seen in Table 8, the neural network estimation speed is closely related to the training samples. The smaller the scale of the samples, the fewer iterations in the training session, and the faster predictions are made. Fixed initialization under the same sample scale significantly improves the neural network forecast speed.

In practical engineering, firstly, the fixed data samples are selected to train the neural network; secondly, the trained neural network is fine-tuned with the variable data samples to generate a suitable model; and, finally, the prediction of the SM conduction sequence is accomplished by merging the latest SM capacitor voltage. At this time, the output voltage u_j of the harmonic content is as shown in Table 9, below.

Table 9. Harmonic content of u_j before and after prediction.

	Ideal	Pre-Modulation	Traditional Method	Forecast Methodology
Harmonic content (THD)	6.68%	10.13%	7.38%	8.89%

From Table 9, it can be seen that the neural network prediction method satisfies the accuracy of control requirements. If we imagine that the number of SMs in each bridge and hidden layer in the neural network are m and n , separately, then, as a result, the time complexity of the neural network and the sorting algorithm are $O(2mn + m + n)$ and $O(m^2)$, respectively. When $m - \frac{n}{m} - 2n \geq 1$ is satisfied, the forecast time delay of the neural network will be less than that of the bubble sort.

6. Conclusions

The reasons for SM capacitor voltage imbalance are examined in this paper from two perspectives: the SM capacitor values and the modulation mechanism. The adverse impacts of SM capacitor voltage imbalance are explored in detail, such as boosting the circulating current, relaxing the usage of the DC voltage, and giving rise to overheating and vibration in specific SMs.

The time series prediction technique is implemented based on historical values to forecast the SM capacitor voltage and arm current in real time. The mixed Gaussian distribution of the capacitor voltage offset is developed, and the compensation voltage is calculated. The usual sorting method is used to produce the trigger sequences, regarded as a sample to train the neural network. Then, the prediction of the SM trigger sequence and the completion of the control are achieved by uniting the anticipated values for the SM capacitor voltage, the arm current, and the compensation value for voltage deviation.

The SM capacitor voltage balancing control strategy based on neural network prediction is verified via Matlab/Simulink simulation. It improves the speed while satisfying the accuracy and provides an idea for the subsequent intelligent control of the capacitor voltage balance.

Author Contributions: Writing—original draft, Q.X.; Writing—review & editing, Y.T.; Funding acquisition, Y.F. All authors have read and agreed to the published version of the manuscript.

Funding: This work was supported in part by the National Key Research and Development Program of China (2021YFB1507000).

Data Availability Statement: Data will be made available on request.

Conflicts of Interest: The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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