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System of Surface Defect Monitoring Based on a Distributed Crack Sensor

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Received: 22 August 2017; Accepted: 9 October 2017; Published: 11 October 2017

Abstract: In this paper, we propose a method for monitoring surface defects like cracks in highly loaded structures. This method is based on the ability of surface cracks to open under the influence of external loads, thus causing the appearance of stresses and tears in the sensitive element—thin films that were deposited on the surface of the test object. We developed a system for monitoring surface defects based on a distributed crack sensor, the functional scheme of the sensor and its design, the structural scheme and algorithm of the system operation, and its model as a VHDL (VHSIC (Very high speed integrated circuits) Hardware Description Language)-description.

Keywords: sensor; surface defect monitoring; surface crack

1. Introduction

The monitoring of defects occurring through the operation of highly loaded structures is important for the economy and for people's safety. The sheathing of aircraft, sea vessels, bridge supports, structural elements of construction equipment, drilling rigs, etc., undergo periodic and static loading during operation. As a result, fatigue cracks appear in the material of these structures. This can lead to the destruction of the structure [1–3].

Over the past decade, a number of new methods and devices for nondestructive testing have been developed. These aids are characterized by ease of automation, autonomy, and the ability to monitor while the monitored object is in its operation mode [4–10].

This work is focused on the development of a method for detecting surface defects such as cracks, and a defect monitoring system that makes it possible to realize this method. In [11], we proposed to use the fact that, under the influence of external loads, surface cracks are opened and, if a thin film is deposited onto the surface, this film will also undergo stresses, and therefore can be torn. Only the case when stresses normal to the crack walls are applied to a surface-cracked object is studied. This case is also known as a tensile or opening mode. Such impacts can lead to further rapid growth of the crack, since the vertices of the crack in this case raise the stress, and the material in these areas is therefore subjected to increased loads. Situations when the object undergoes torsional or bending deformations were not considered.

The authors developed a model of a layered structure in which a thin metal film was deposited on a dielectric polymer material located above a surface crack [11]. This model indicated that tensile stresses create a high level of stress in a thin metal film over a crack (as a result of modeling an aluminum plate with a 50 μm depth crack and coated with 50 μm thick polyimide film and 30 μm thick copper film, 12–13.5 GPa stress appeared in the copper film material above the crack) and can lead to its rupture. In the reference data, the authors did not find values for the tensile strength of copper exceeding 450 MPa.

and passkeys PK, the lines are alternately connected (and, for broken lines, connecting their segments one by one) to the V_{DD} power supply and the load resistor (Figure 1a).

The integrity of the conductors is monitored by voltage levels at the outputs U_i^- , U_i^+ and U_j . Low voltage levels at these outputs indicate a break in the line or segment, and high levels indicate its integrity.

We developed the algorithm for the operation of the surface defect monitoring system. Its block diagram is shown in Figures 2 and 3.

A full cycle of checking conductors for integrity is implemented using four system modes (k—mode number). In the first mode, the integrity of the conductors of the first layer with indices $i = 1, 2, \dots, I$ is checking. Multiplexers from MUX^{i+1} to MUX^{i+1} connect all i -th lines to the supply voltage V_{DD} in parallel using the control signal P_i , and the keys from PK^{i-1} to PK^{i-1} and from PK^{i+1} to PK^{i+1} alternately include each i -th line in the circuit. If the line is damaged, a low voltage level is registered on the U_i^- pin and a logical '0' is written to the memory cell corresponding to the number of the damaged line in random access memory (RAM) MEM1 with one-dimensional addressing. Accordingly, the number of cells in memory MEM1 is equal to the number of lines I .

In the second mode, the lines with indices $j = 1, 2, \dots, J$ are similarly checked. At a low voltage level at the output U_j , '0' is written to the memory cell corresponding to the number of the line currently being checked in the RAM MEM2 with one-dimensional addressing. The number of cells in memory MEM2 is equal to the number of j -th lines.

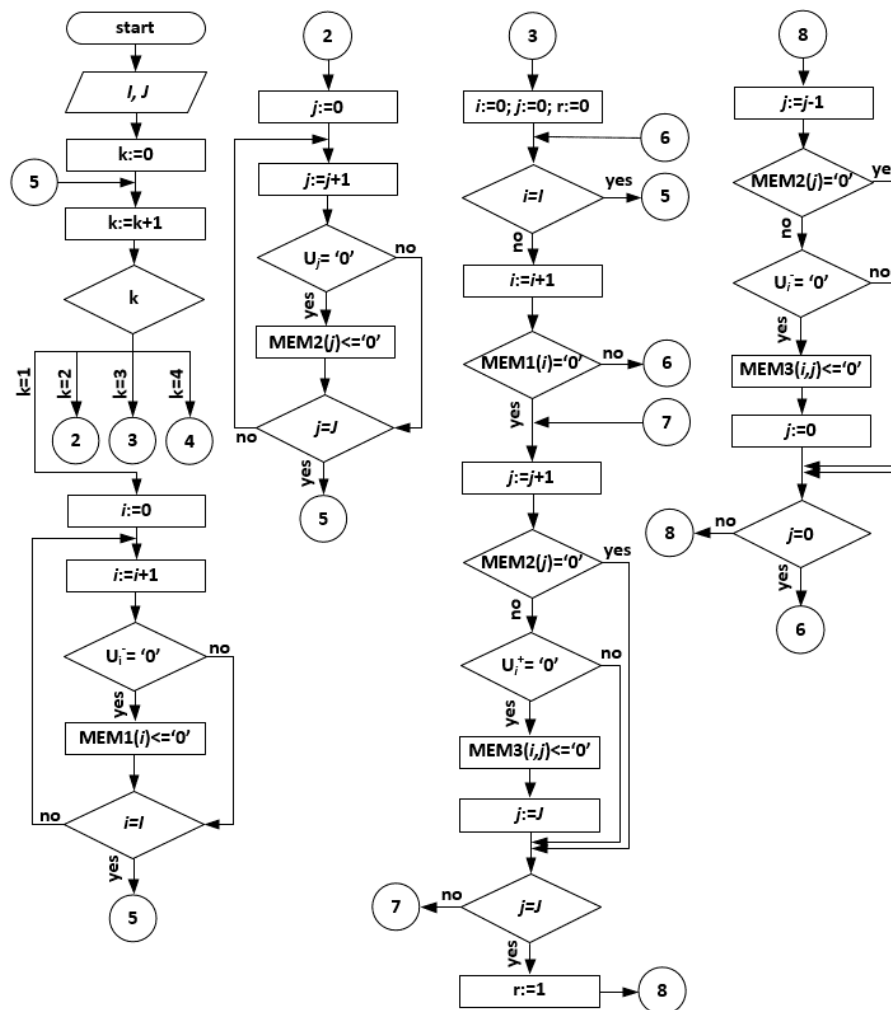


Figure 2. Operation algorithm of the surface defect monitoring system. Part I.

In the third and fourth modes, all segments of defective i -th and j -th lines are checked, respectively. This is done to clarify the location of the defect.

In the third mode, the voltage V_{DD} is applied to the first defective i -th line in order of increasing number through the multiplexer MUX^{i+i} and the key PK^{j+i} corresponding to the first right defect-free j -th line, and the voltage at the terminal U_i^+ is checked. If the signal passes (high voltage level on U_i^+), this segment is considered to be defect-free, and the power voltage V_{DD} is connected to the previous defect-free j -th line through the key PK^{j+i} . If a low voltage level at the U_i^+ pin is registered, the segment under investigation is considered damaged. In this case, '0' is written to the memory MEM3 with two-dimensional addressing at the address corresponding to the segment index. Further, the segments belonging to this i -th line are checked in reverse order by including the key PK^{i-i} corresponding to the defective i -th line and the key PK^{j+j} corresponding to the first left defect-free j -th line, and then the sorting of j -th lines is carried out in order of increasing number. The damage of the segment is checked based on the presence of a low voltage level at the output U_i^- .

After checking all defective i -lines, the segments of defective j -lines are checked in the fourth mode in the same way, and the verification cycle is completed.

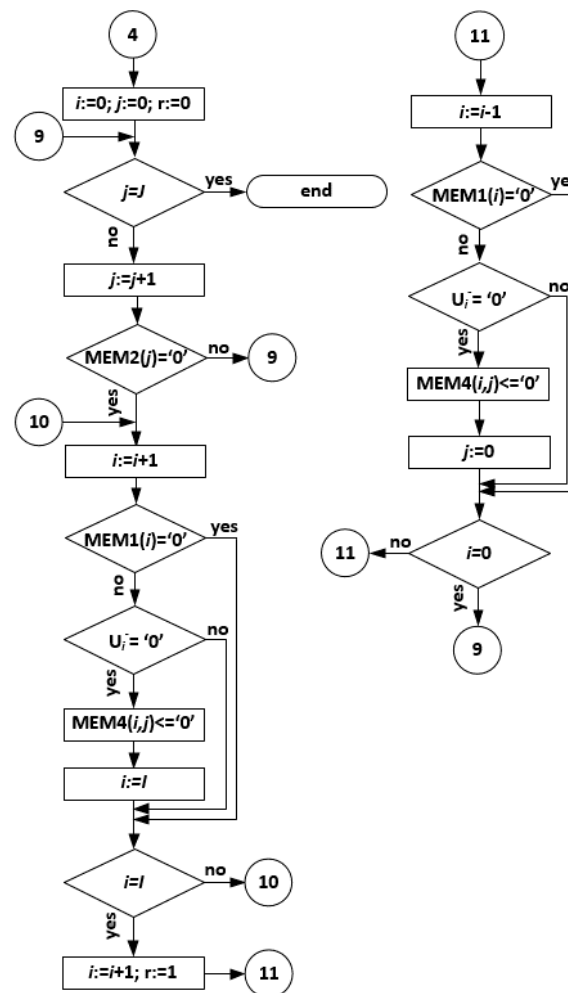


Figure 3. Operation algorithm of the surface defect monitoring system. Part II.

This operation algorithm is implemented as a finite-state machine, the graph of which is shown in Figure 4.

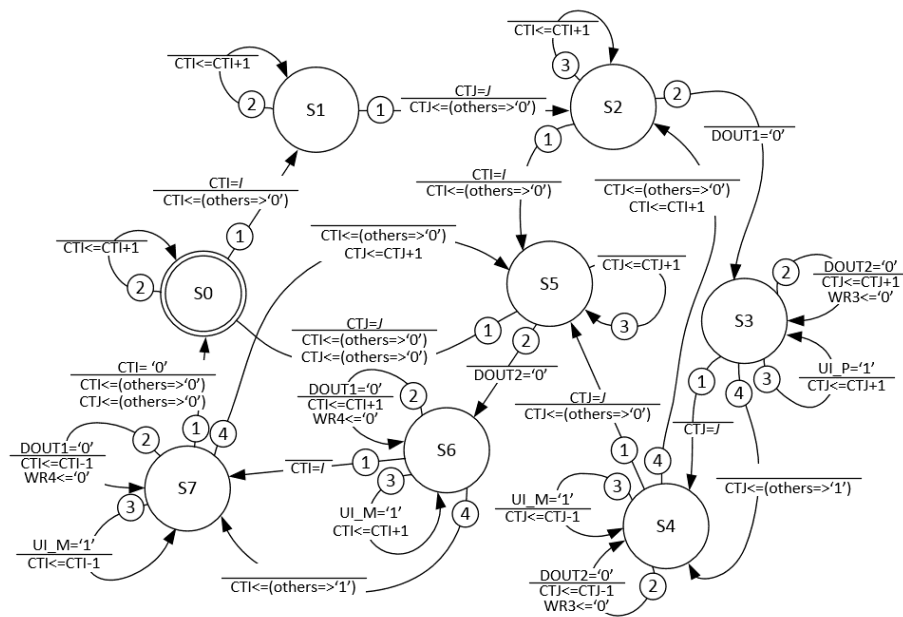


Figure 4. The finite-state machine graph, managing the work of the surface defect monitoring system.

The states of the finite-state machine are given in Table 1. The finite-state machine can be in one of the eight states S0–S7.

Table 1. The states of the finite-state machine.

S	k	WR1	WR2	WR3	WR4	DIN3	SI_M	SI_P	SJ_M	SJ_P	P_I	P_J
S0	1	1	0	0	0	0	1	1	0	0	1	0
S1	2	0	1	0	0	0	0	0	1	1	0	0
S2	3	0	0	0	0	0	0	0	0	0	0	0
S3	3	0	0	1	0	1	0	1	0	1	0	0
S4	3	0	0	1	0	0	1	0	0	1	0	0
S5	4	0	0	0	0	0	0	0	0	0	0	0
S6	4	0	0	0	1	0	1	0	0	1	0	0
S7	4	0	0	0	1	0	1	0	1	0	0	1

Signal designations in Table 1 correspond to Figure 4. Signals WR1 and WR2, taking the value ‘1’, allow the writing of a bit to the cells of memory MEM1 and MEM2, respectively. Signals WR3 and WR4, taking the value ‘1’, allow the writing of a bit to the cells of RAM MEM3 and MEM4, which stores information about defective segments of the i -th and j -th lines. The DIN3 signal determines the connection of the MEM3 and MEM4 data input lines to the U_i^+ or U_i^- lines, in accordance with the current checking order of the segments of the defective i -th line. Signals SI_M, SI_P, SJ_M and SJ_P control semiconductor switches PK in accordance with the current operating mode of the system. The signal P_i controls multiplexers MUX^{i+1} and determines the connection of the i -th lines to the power supply V_{DD} or to the load resistor R_i^+ . The signal P_j controls the multiplexers MUX^{j+1} and determines the connection of j -th lines to the supply V_{DD} or to the load resistor R_j .

The states S0 and S1 of the finite-state machine correspond to the first and second mode k of the system operation algorithm shown in Figures 2 and 3. In the state S2, the RAM MEM1 is checked, and if there are cells in the memory MEM1 where the value ‘0’ is stored, the first (in order of increasing number) i -th line is selected, at the address of which the value ‘0’ is stored in the memory cell. If there are no zeros in MEM1, the finite-state machine goes to state S5. In the state S3, all segments of the defective i -th line are examined from right to left; in state S4, from left to right. In the state S5, as in S2, the RAM MEM2 is checked, and if there are cells where the value ‘0’ is stored, the first (in order of

increasing number) j -th line is selected, at the address of which the value '0' is stored in the memory cell. If there are no damaged lines among the j -lines, the transition to the initial state S_0 is carried out. In the state S_6 , all segments of the j -th damaged line are checked from the bottom up; in the state S_7 , from the top down (this orientation corresponds to Figure 1a). After checking all the segments of the damaged j -lines, the transition to the initial state S_0 follows.

The developed structural scheme of the surface defect monitoring system is shown in Figure 5.

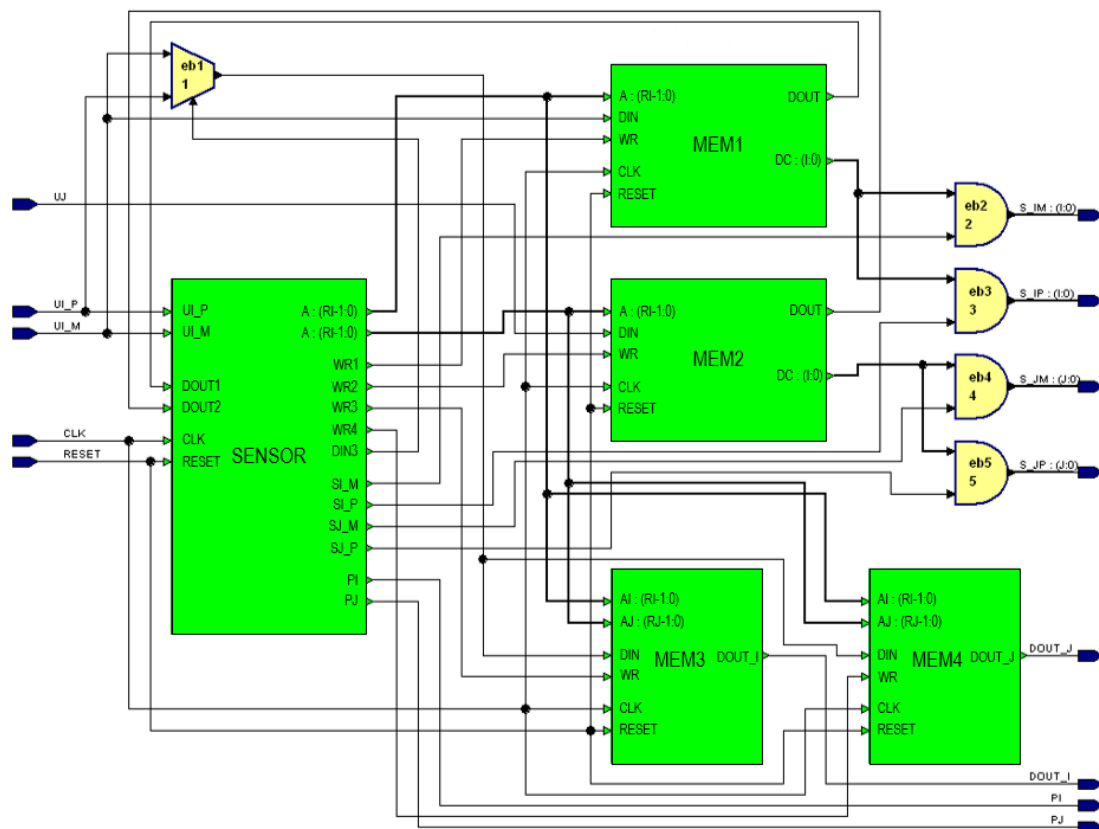


Figure 5. The structural scheme of the surface defect monitoring system.

The system consists of a control block SENSOR and memory blocks MEM1, MEM2, MEM3 and MEM4. The control block is a clocked finite-state machine, the graph of which is shown in Figure 4. Memory blocks MEM1 and MEM2—with one-dimensional addressing—consist of single-digit cells, the number of which is I and J , respectively. Memory blocks MEM3 and MEM4—with two-dimensional addressing—consist of single-digit cells, the number of which is $I \times J$. Two memory blocks are used for each memory block MEM3 and MEM4, since the total number of segments is $2(I \times J)$. At the time the system is turned on, the RESET signal, assuming a value of '1', initiates the recording of logical '1' into all the cells of the memory blocks MEM1, MEM2, MEM3 and MEM4.

Thus, by the end of the finite-state machine cycle, the results of checking the integrity of the segments of thin-film conducting lines are in the memory blocks MEM3 and MEM4. Then, the information from the outputs DOUT_I and DOUT_J goes to the computer for further processing.

3. Results

In this paper, we considered a system for monitoring surface defects based on a distributed crack sensor. This system detects disruptions in thin conductive films deposited on the surface of a test object. This can help us to detect the occurrence of surface cracks. These results apply only to cases of the first mode of deformation, or opening crack mode. The possibility of rupturing a thin conducting

film had been considered previously by the authors [11]. In this paper, the functional scheme for the proposed distributed crack sensor, its design, structural scheme and algorithm of the system operation, and its model as a VHDL-description were developed.

Acknowledgments: This study was supported by “Development programs of the Southern Federal University until 2021” (project VnGr-07/2017-10).

Author Contributions: Boris G. Konoplev, Eugeny A. Ryndin and Alina S. Isaeva developed the design of the distributed crack sensor, Eugeny A. Ryndin developed the structural scheme of the system operation and its model as a VHDL-description, Alina S. Isaeva and Mark A. Denisenko developed the algorithm of the system operation. Alina S. Isaeva wrote the paper.

Conflicts of Interest: The authors declare no conflict of interest.

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