electronics

MDPI

Article

Optimization of Line-Tunneling Type L-Shaped Tunnel Field-Effect-Transistor for Steep Subthreshold Slope

Faraz Najam and Yun Seop Yu *

Department of Electrical, Electronic and Control Engineering and IITC, Hankyong National University, Anseong 17579, Korea; faraznajam@hknu.ac.kr

* Correspondence: ysyu@hknu.ac.kr; Tel.: +81-31-670-5293

Received: 12 October 2018; Accepted: 22 October 2018; Published: 24 October 2018

Abstract: The L-shaped tunneling field-effect-transistor (LTFET) has been recently introduced to overcome the thermal subthreshold limit of conventional metal-oxide-semiconductor field-effect-transistors (MOSFET). In this work, the shortcomings of the LTFET was investigated. It was found that the corner effect present in the LTFET effectively degrades its subthreshold slope. To avoid the corner effect, a new type of device with dual material gates is presented. The new device, termed the dual-gate (DG) LTEFT (DG-LTFET), avoids the corner effect and results in a significantly improved subthreshold slope of less than 10 mV/dec, and an improved ON/OFF current ratio over the LTFET. The DG-LTFET was evaluated for different device parameters and bench-marked against the LTFET. This work presents the optimum configuration of the DG-LTFET in terms of device dimensions and doping levels to determine the best subthreshold, ON current, and ambipolar performance.

Keywords: band-to-band tunneling; L-shaped tunnel field-effect-transistor; double-gate tunnel field-effect-transistor; corner-effect

1. Introduction

Tunnel field-effect-transistors (TFETs) are being actively pursued as a potential replacement to conventional metal-oxide-semiconductor (MOS) technology [1]. TFETs offer a sub-thermal subthreshold slope (SS) but suffer from limited ON current I_{ON} performance [2]. To overcome the limit, different types of line tunneling type TFETs have been introduced, including L-shaped [3] (LTFETs), U-shaped [4] (UTFETs), and Z-shaped [5] TFETs (ZTFETs). Among them, only the LTFET has been experimentally demonstrated [3].

It was found using device simulations that the 2D corner effect [6] present in LTFETs degrades its subthreshold performance. In order to remove SS degradation due to the kink effect induced by the source corner, the fully depleted rounded corner with a gradual doping profile was used [6]. The LTFET still achieves a sub-thermal SS, but as shown in this work there is room for significant improvement in the subthreshold performance of LTFETs. To achieve this improvement, a new device based on the original LTFET is introduced. The new device uses a dual-gate (DG) structure and is termed the DG-LTFET. The two gates (gate1 and gate2) have different workfunctions and different heights. The DG-LTFET was thoroughly evaluated for different device parameters, including the source region height, gate1 and gate2 heights, gate1 and gate2 workfunctions, channel thickness, and drain doping levels. Optimum dimensions and drain doping level were determined for the DG-LTFET. Section 2 briefly discusses the corner-effect problem of the LTFET. Section 3 introduces the DG-LTFET and compares its results with the LTFET. Section 4 presents the conclusion.

2. The LTFET: The Corner Effect

Figure 1 shows a schematic for LTFET. The p^+ (10^{20} cm^{-3}) doped source region overlaps the gate with the n^- (10^{12} cm^{-3}) channel sandwiched in between them. This sandwiched channel region is termed as $R_{nonoffset}$. There is also a part of the channel termed R_{offset} in which there is an offset present between the source and the gate, as indicted in Figure 1. The following parameters were used for all devices considered in this work unless otherwise specified: source height (H_s) = 40 nm, oxide thickness (t_{ox}) = 2 nm, length of $R_{nonoffset}$ (T_j) = 5 nm, channel length (L_{ch}) = 50 nm, height of R_{offset} (H_{offset}) = 10 nm, height of $R_{nonoffset}$ ($H_{nonoffset}$) = H_s, gate height (H_{g1}) = H_s + (H_{offset} − t_{ox}) = 48 nm, dielectric permittivity ε_{ox} = 25, metal gate workfunction W_{rk_LTFET} = 4.72 eV, and drain doping (N_d) = 10^{20} cm^{-3}.

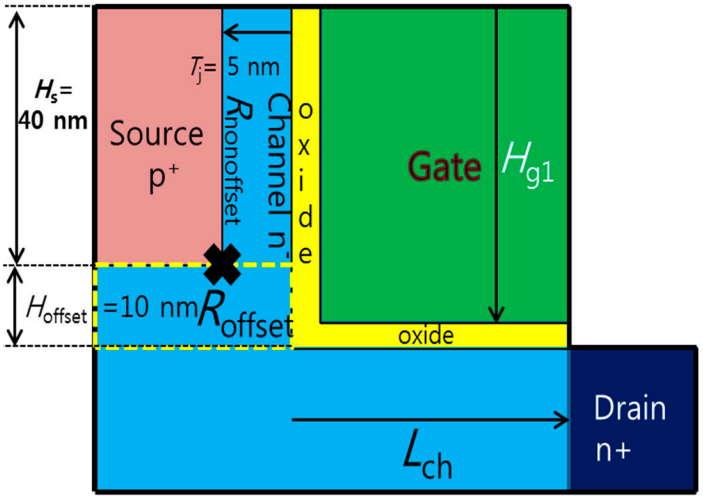


Figure 1. Schematic of the L-shaped tunneling field-effect-transistor (LTFET).

Sentaurus technology-computer-aided-design tool (TCAD) was used as the simulator [7]. The following models were used in the simulation: the dynamic nonlocal band-to-band-tunneling (BTBT) model, Fermi statistics, and the constant mobility model. The dynamic nonlocal BTBT model calculates BTBT in both lateral and 1D directions. Crystal orientation is assumed to be <100> in all devices. A constant electron effective tunneling mass of 0.19 m_o was used in all simulations [8]. All simulations were performed at a drain source bias V_{ds} = 0.1 V unless otherwise specified.

For analysis to follow, drain-source current (I_{ds}) versus gate-source bias (V_{gs}) characteristics of the LTFET are shown in Figure 2a. There is a direct overlap between gate and source in $R_{nonoffset}$, and the electric field in $R_{nonoffset}$ is in the 1D direction. In R_{offset}, however, the electric field from the gate converges around the sharp source corner marked by an **X** in Figure 1. This increases the potential in R_{offset} as compared to $R_{nonoffset}$ for any given bias (until potential saturates due to electron inversion). Figure 2b shows the surface potential at V_{gs} = 0 V. It can be seen that, because the electric field converges around the sharp source corner [6], the potential in R_{offset} has increased. Since the potential is higher in R_{offset} as compared to $R_{nonoffset}$, the threshold voltage for BTBT in R_{offset} ($V_{th\_Roffset}$) is lower than the threshold voltage for BTBT in $R_{nonoffset}$ ($V_{th\_Rnonoffset}$).

Figure 3a,b show the tunneling rate (G_{tun}) contour plot and G_{tun}, respectively, at V_{gs} = 0.21 V which is the bias needed to generate I_{ds} = 10^{-13} A (from Figure 2a). It is obvious from Figure 3 that the BTBT only takes place in R_{offset}, whereas $R_{nonoffset}$ is completely switched off. Figure 4a shows G_{tun} at several V_{gs} values. From Figure 4a, $V_{th\_Roffset}$ and $V_{th\_Rnonoffset}$ can be found to be around V_{gs} = 0.17 V and 0.24 V, respectively. Figure 4b shows the G_{tun} contour plot at V_{gs} = $V_{th\_Rnonoffset}$ = 0.24 V. Figure 4a shows that G_{tun} in $R_{nonoffset}$ just after it turns on, is always higher and has a much larger BTBT area (in the y direction) as compared to R_{offset}. Thus, whenever $R_{nonoffset}$ turns on, it dominates over R_{offset}. The reason why G_{tun} is higher in $R_{nonoffset}$ is simply because the BTBT paths in R_{offset} are laterally

oriented or 2D from source to the surface in R_{offset}, whereas the BTBT paths in $R_{nonoffset}$ are 1D. The 2D BTBT paths being naturally longer than the 1D paths result in a lower G_{tun} in R_{offset}.

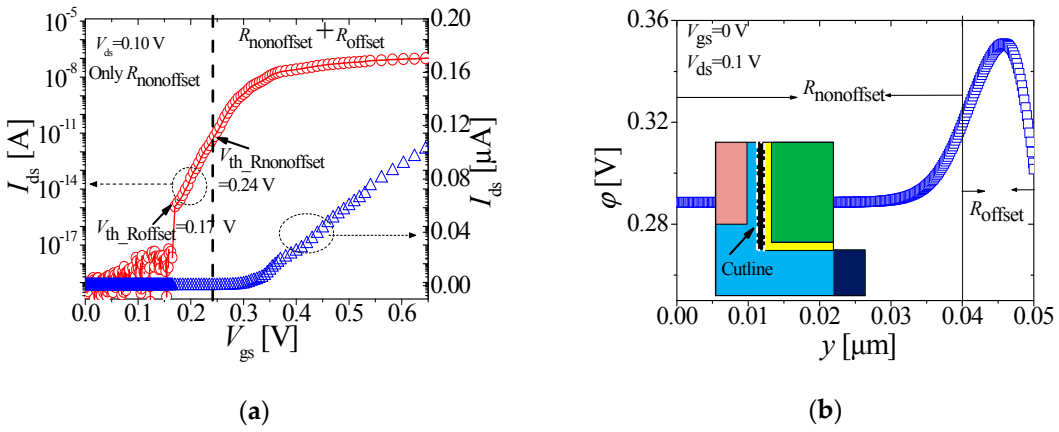


Figure 2. (**a**) I_{ds}-V_{gs} transfer characteristics of the LTFET. $V_{th\_Rnonoffset}$ = 0.24 V and $V_{th\_Roffset}$ = 0.17 V. (**b**) Potential along the cutline shown in the inset at V_{gs} = 0 V. Potential is higher in R_{offset}.

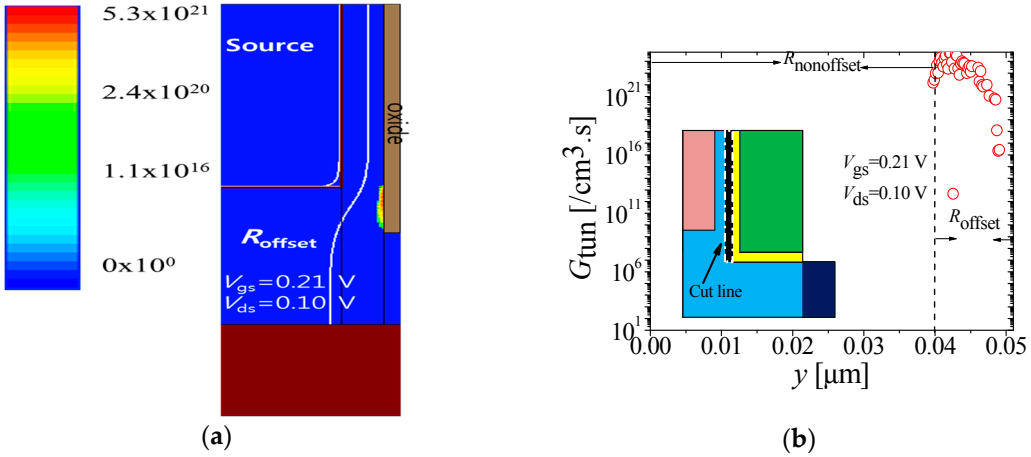
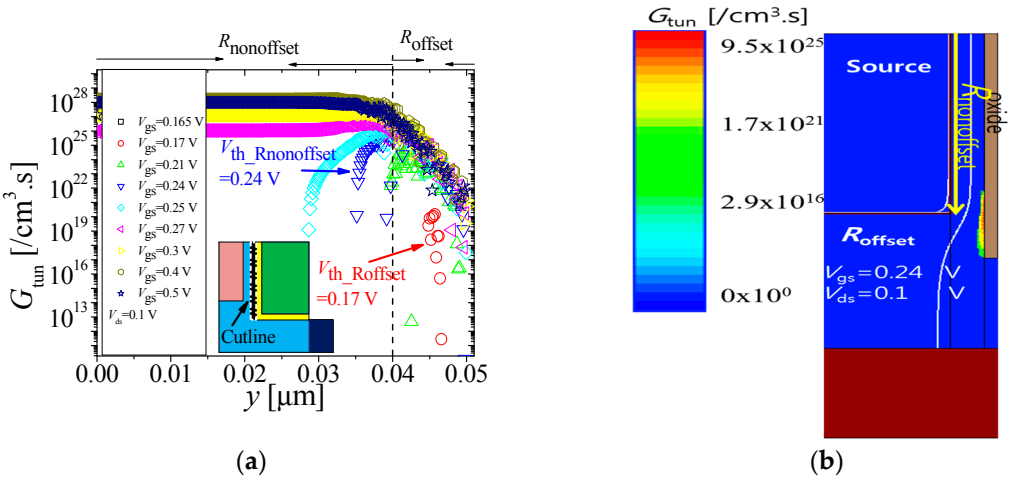


Figure 3. (**a**) G_{tun} contour plot at V_{gs} = 0.21 V, which is the bias needed to generate I_{ds} = 10^{-13} A and (**b**) G_{tun} extracted from (**a**).

From Figure 4a, it can be observed that, for a large part of the subthreshold region (V_{gs} < 0.24 V), only R_{offset} with the longer 2D BTBT paths and lower G_{tun} is contributing to the BTBT current and the more efficient $R_{nonoffset}$ makes no contribution to the current. In other words, the LTFET underperforms in the subthreshold region. If $R_{nonoffset}$ could be forced to turn on at a lower bias than R_{offset}, which is the condition $V_{th\_Rnonoffset}$ < $V_{th\_Roffset}$, $R_{nonoffset}$ will turn on in the subthreshold region, and with the condition G_{tun} in $R_{nonoffset}$ > G_{tun} in R_{offset}, demonstrated in Figure 4a, a significant improvement in SS could be expected.

In other words, the $R_{nonoffset}$ could be regarded as a parasitic region with a parasitic, fringing capacitance originating from the bottom of the gate to the sharp source corner. Since the potential is different in this area (Figure 2b), the capacitance associated with this region is different from the $R_{nonoffset}$ region. If $V_{th\_Rnonoffset}$ < $V_{th\_Roffset}$ could be achieved, as is demonstrated below, the effect of this parasitic capacitance could be practically eliminated, and this is the purpose of the device proposed below. Since drain is not in close proximity to R_{offset}/$R_{nonoffset}$, where the BTBT current is generated, gate-drain capacitance fringing capacitance is not expected to influence the potential and BTBT significantly at high frequency.



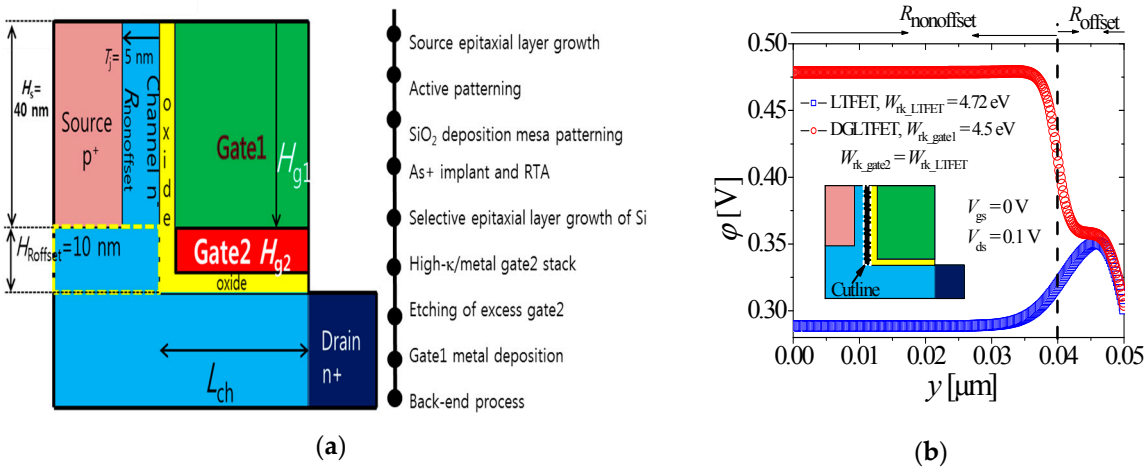
(**a**) (**b**)

Figure 4. (**a**) G_{tun} at different V_{gs}. (**a**) $V_{th\_Rnonoffset}$ = 0.24 V and $V_{th\_Roffset}$ = 0.17 V. (**b**) G_{tun} contour plot at V_{gs} = $V_{th\_Rnonoverlap}$ = 0.24 V. In (**b**), yellow arrow indicates the height of $R_{nonoffset}$.

3. DG-LTFET

3.1. The DG-LTFET: Basic Device Physics

In order to achieve the condition $V_{th\_Rnonoffset} < V_{th\_Roffset}$, the DG-LTFET is presented in Figure 5a. DG-LTFET uses dual material gates denoted by gate1 and gate2, each with a different workfunction ($W_{rk\_gate1/2}$) and height ($H_{g1/2}$). $H_{g1} = H_{nonoffset} = H_s$ = 40 nm, H_{offset} = 10 nm, $H_{g2} = H_{nonoffset} - H_{g1} + (H_{offset} - t_{ox})$ = 8 nm, and T_j = 5 nm. W_{rk_gate1} is always lower than W_{rk_gate2}. W_{rk_gate2} is fixed at W_{rk_LTFET} = 4.72 eV for all DG-LTFET considered in this work. The DG-LTFET process-flow is indicated in Figure 5a. The process-flow is based on the LTFET process-flow [3]. The DG-LTFET process-flow follows the LTFET process-flow until the chemical vapor deposition (CVD) of gate2 (similar to the gate deposition in the LTFET). After this, two additional steps are required. The device is masked to protect the gate oxide and channel areas, and gate2 is selectively etched according to the desired height. Gate1 is then deposited in the recess created by gate2-etching by a low-temperature atomic layer deposition process. Similar dual-material gate structures have been extensively reported in the literature including [9–11].



(**a**) (**b**)

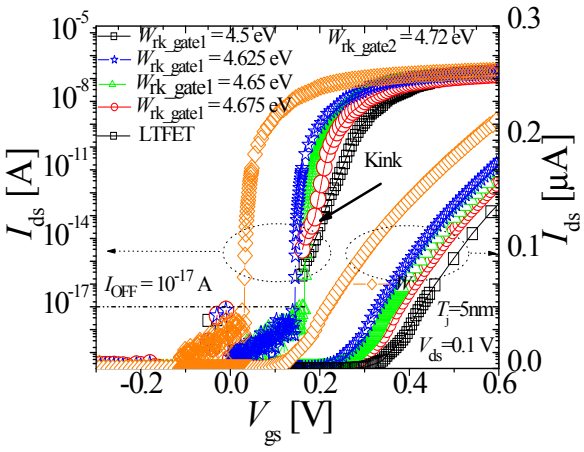
Figure 5. (**a**) Schematic of DG-LTFET with process-flow indicated alongside and (**b**) V_{fb} of DG-LTFET (red symbols) compared with that of the LTFET (blue symbols). In the DG-LTFET, W_{rk_gate1} = 4.5 eV and W_{rk_gate2} = W_{rk_LTFET} = 4.72 eV were used.

Lower W_{rk_gate1} results in an increased flatband voltage [12] (V_{fb}) in $R_{nonoffset}$ as compared to R_{offset}. Figure 5b shows V_{fb} of DG-LTFET (red symbols) with W_{rk_gate1} = 4.5 eV and W_{rk_gate2} = W_{rk_LTFET}. Also shown for the reference is V_{fb} of the LTFET (blue symbols). Expectedly, the DG-LTFET potential increases in $R_{nonoffset}$. The potential does not change abruptly from gate1 to gate2 because of the presence of 2D effects around the source corner. Electric field from the bottom of gate2 converges around the source corner. Around the middle of R_{offset}, equilibrium is established between the two gates and DG-LTFET potential overlaps LTFET potential since W_{rk_gate2} = W_{rk_LTFET}. With W_{rk_gate1} < W_{rk_gate2}, the increased potential in $R_{nonoffset}$ reduces $V_{th\_Rnonoffset}$. If $W_{rk\_gate1/2}$ are appropriately tuned with W_{rk_gate1} < W_{rk_gate2}, the condition $V_{th\_Rnonoffset}$ < $V_{th\_Roffset}$ = 0.17 V can be achieved. Because W_{rk_gate2} = W_{rk_LTFET} = 4.72 eV, $V_{th\_Roffset}$ (in the DG-LTFET) is equal to $V_{th\_Roffset}$ (in the LTFET).

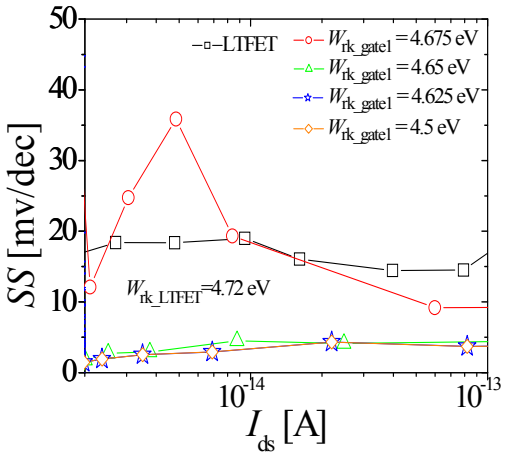
Figure 6a–c show I_{ds}-V_{gs} characteristics at different W_{rk_gate1}, SS, and I_{ON}/I_{OFF} of the DG-LTFET with constant W_{rk_gate2} = W_{rk_LTFET} = 4.72 eV for all DG-LTFET, respectively. Also shown for the reference is the I_{ds}-V_{gs} characteristics of the LTFET (black squares). I_{ON} is extracted at V_{gs} = 0.7 V, and I_{OFF} is defined as I_{ds} = 10^{-17} A. With W_{rk_gate1} = 4.675 eV (red circles), the $V_{th\_Rnonoffset}$ is reduced to 0.189 V. Compared with the LTFET, $R_{nonoffset}$ now turns on earlier in the subthreshold region, along with R_{offset}. Since the BTBT is more efficient in $R_{nonoffset}$ (Figure 4a) as compared to R_{offset}, I_{ds} increases more rapidly within the subthreshold region.

Hence, just at the transition point, where $R_{nonoffset}$ turns on (V_{gs} ~0.189), a kink appears in the I_{ds}-V_{gs} curve. With W_{rk_gate1} = 4.65 eV (green triangles), $V_{th\_Rnonoffset}$ is reduced to V_{gs} = 0.167 V and the condition $V_{th\_Rnonoffset}$ < $V_{th\_Roffset}$ is achieved, and DG-LTFET exhibits a remarkable SS with values less than 10 mV/dec as seen in Figure 6b. With W_{rk_gate1} = 4.625 eV (blue stars), $V_{th\_Rnonoffset}$ reduces further to 0.1448 V, which is < $V_{th\_Roffset}$. If $V_{th\_Rnonoffset}$ < $V_{th\_Roffset}$ is established, then any increase in $V_{th\_Roffset} - V_{th\_Rnonoffset}$ simply shifts the I_{ds}-V_{gs} to the left without any change in SS as shown by the blue stars (W_{rk_gate1} = 4.625 eV) and orange diamonds (W_{rk_gate1} = 4.5 eV) in Figure 6a,b, respectively. An improvement of ~16% is observed in the I_{ON}/I_{OFF} of the DG-LTFET (with W_{rk_gate1} = 4.625 eV) over the LTFET.

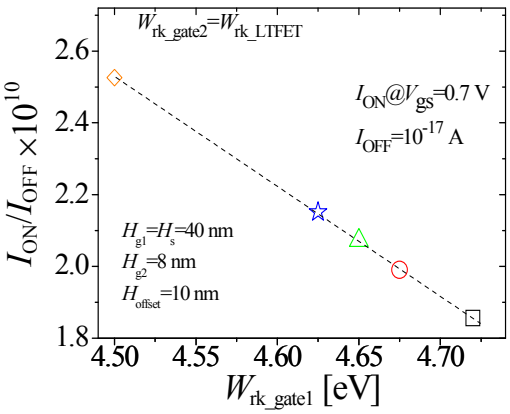
Figure 7a shows the G_{tun} contour plot of DG-LTFET at a V_{gs} (= 0.172 V) bias needed to achieve an equivalent I_{ds} of 10^{-13} A in DG-LTFET with W_{rk_gate1} = 4.65 eV. Figure 7b shows the contour plot extracted from Figure 7a. For reference, Figure 7b also shows that G_{tun} needed to generate an equivalent amount of I_{ds} in the LTFET (at a V_{gs} bias of 0.21 V, Figure 3b). As can be seen in Figure 7b, the LTFET needs contribution only from R_{offset}, but generating the same amount of I_{ds} DG-LTFET depends heavily on $R_{nonoffset}$ with some contribution from R_{offset}. Because G_{tun} in $R_{nonoffset}$ is more efficient (Figure 4a), as the V_{gs} bias increases, G_{tun} increases exponentially in a much larger area in $R_{nonoffset}$, which results in the DG-LTFET exhibiting a much steeper subthreshold swing, while the LTFET continues to depend only on the inefficient BTBT in R_{offset} until around $V_{th\_Rnonoffset}$ = 0.24 V.



(**a**)



(**b**)



(**c**)

Figure 6. (**a**) I_{ds}-V_{gs} characteristics of DG-LTFET with different W_{rk_gate1}s and fixed W_{rk_gate2} = W_{rk_LTFET}. Also shown are I_{ds}-V_{gs} characteristics of the LTFET (black squares). (**b**) SS extracted from I_{ds}-V_{gs} characteristics in Figure 8a. (**c**) I_{ON}/I_{OFF} ratio extracted from I_{ds}-V_{gs} characteristics in Figure 8a. Red circles: W_{rk_gate1} = 4.675 eV; green triangles: W_{rk_gate1} = 4.65 eV; blue stars: W_{rk_gate1} = 4.625 eV; orange diamonds: W_{rk_gate1} = 4.5 eV.

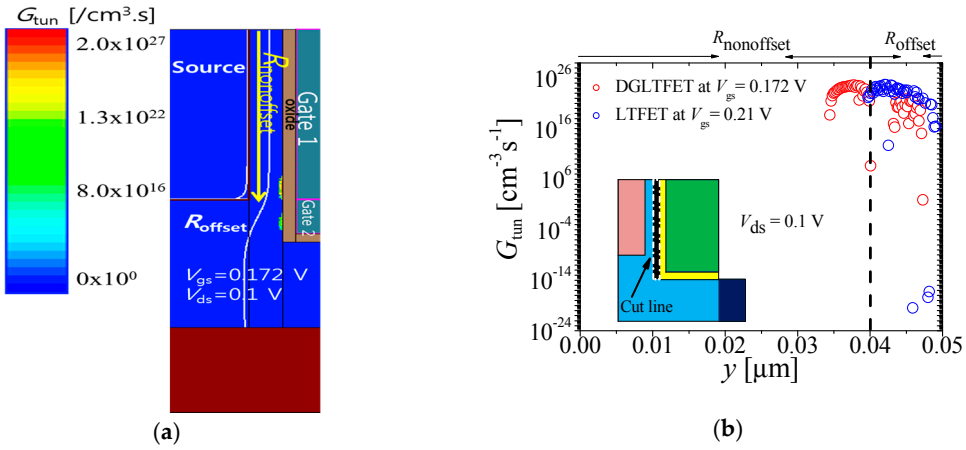


Figure 7. (**a**) G_{tun} contour plot of DG-LTFET at V_{gs} = 0.172 V, which is needed to generate $I_{ds} = 10^{-13}$ A and (**b**) G_{tun} extracted from (**a**) (red symbols). Also shown for reference is G_{tun} (blue symbols) of the LTFET at a V_{gs} bias needed to generate $I_{ds} = 10^{-13}$ A. In (**a**), yellow arrow indicates the height of $R_{nonoffset}$.

3.2. Device Optimization

To optimize device performance, the impact of variations in key parameters including $H_{g1/2}$, H_s/T_j, and N_d was investigated. To investigate the impact of $H_{g1/2}$ values, I_{ds}-V_{gs} characteristics for the DG-LTFET at different H_{g1} and H_{g2} = $H_{nonoffset}$ − H_{g1} + (H_{offset} − t_{ox}) with fixed W_{rk_gate1} = 4.5 eV and W_{rk_gate2} = W_{rk_LTFET}, H_s = $H_{nonoffset}$ = 40 nm, H_{offset} = 10 nm, and T_j = 5 nm is presented in Figure 8. It can be seen that I_{ds} is independent of $H_{g1/2}$.

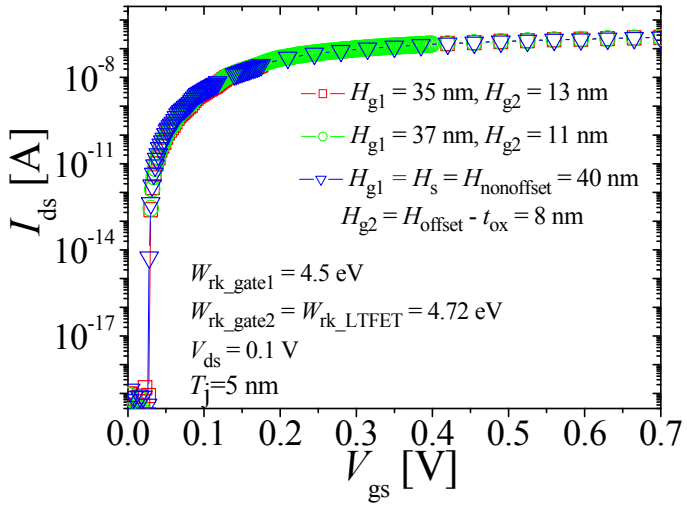
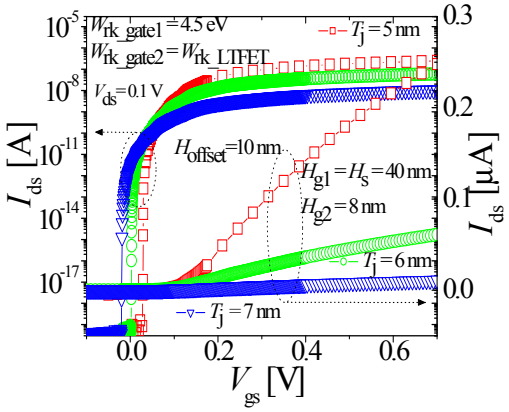
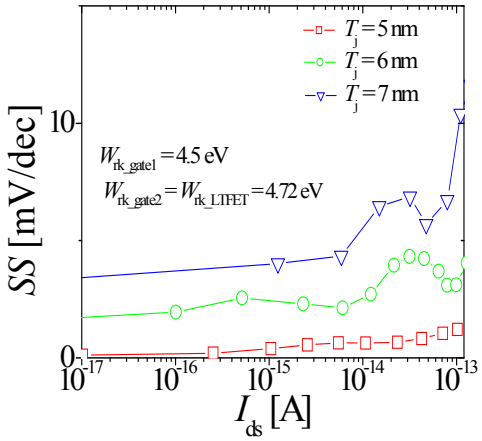


Figure 8. I_{ds}-V_{gs} characteristics for several $H_{g1/2}$s with $W_{rk\_gate1/2}$ = 4.5 eV and W_{rk_gate2} = W_{rk_LTFET}. Red squares, green circles, and blue triangles: H_{g1} = 35, 37, and 40 nm, respectively.

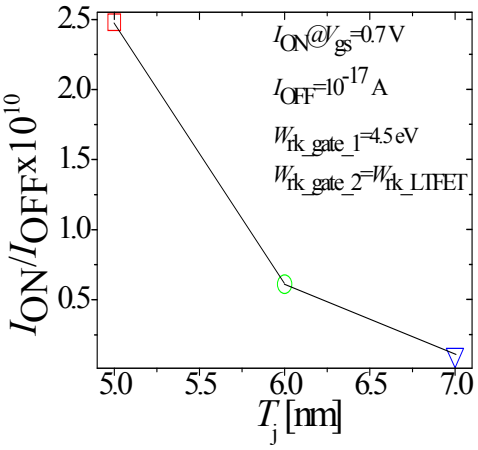
Next, to investigate the effect of T_j on device performance, I_{ds}-V_{gs} characteristics, SS, and I_{ON}/I_{OFF} of DG-LTFET are presented for different T_j with fixed W_{rk_gate1} = 4.5 eV and W_{rk_gate2} = W_{rk_LTFET}, H_{g1} = $H_{nonoffset}$ = 40 nm, H_{offset} = 10 nm, and H_{g2} = $H_{nonoffset}$ − H_{g1} + (H_{offset} − t_{ox}) = 8 nm in Figure 9a–c, respectively. It was found that the increasing T_j results in a degradation of the I_{ON}/I_{OFF} ratio. It is simply because of the increase in BTBT path length with the increase in T_j. The T_j of 5 nm was found to be optimum in this work as any further reduction will bring significant quantum confinement effect into play, which is well known to degrade device performance [4,5,13–15].



(**a**)



(**b**)

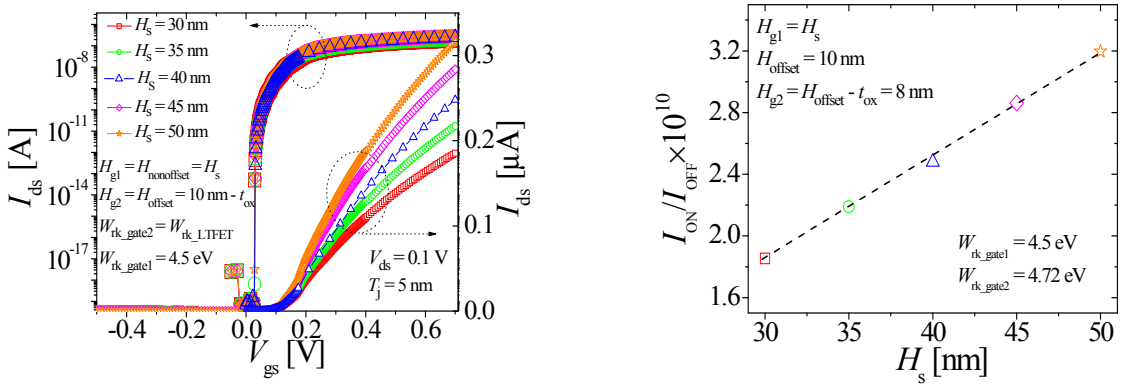


(**c**)

Figure 9. (**a**) I_{ds}-V_{gs} characteristics of the DG-LTFET with different T_j and fixed W_{rk_gate1} = 4.5 eV, W_{rk_gate2} = W_{rk_LTFET}, and H_{g1} = H_s = $H_{nonoffset}$ = 40 nm, H_{g2} = H_{offset} (10 nm) − t_{ox} = 8 nm. (**b**) The SS of I_{ds}-V_{gs} shown in Figure 8a. (**c**) I_{ON}/I_{OFF} ratio of I_{ds}-V_{gs} characteristics shown in Figure 8a. Red squares, green circles, and blue triangles: T_j = 5, 6 and 7 nm, respectively.

Next, the impact of varying H_s was investigated. I_{ds}-V_{gs} characteristics of the DG-LTFET for several H_s with fixed W_{rk_gate1} = 4.5 eV and W_{rk_gate2} = W_{rk_LTFET}, H_{g1} = H_s = $H_{nonoffset}$, H_{g2} = $H_{nonoffset}$ − H_{g1} + (H_{offset} − t_{ox}) = 8 nm, and T_j = 5 nm is presented in Figure 10. By maintaining H_{g1} = H_s, H_{offset} = 10 nm, and H_{g2} = 8 nm, the electric field vector distribution within the DG-LTFET remains the same as H_s is varied, and the BTBT area simply scales with H_s. An increase (decrease) in the BTBT area with H_s simply results in an increased (decreased) I_{ON}/I_{OFF} ratio as shown in Figure 10b with no change in SS, as evident from Figure 10a.

Finally, the ambipolar current of the DG-LTFET is discussed. Ambipolar I_{ds} of TFET depends on the drain-channel junction. In the DG-LTFET, the drain-channel junction is controlled by gate2 with W_{rk_gate2} = W_{rk_LTFET}. With the same workfunction, the electrostatics of the drain-channel junction in the DG-LTFET is exactly the same as that in the LTFET. Figure 11a shows ambipolar I_{ds} of the DG-LTFET compared with the LTFET. Any change in W_{rk_gate1} in the DG-LTFET does not affect the drain-channel junction. The same argument applies for any other design parameter variation in DG-LTFET including H_s, $H_{g1/2}$, and T_j; that is, as long as the electrostatics of the drain-channel junction remains unaffected, the DG-LTFET will exhibit an equivalent ambipolar I_{ds} as the LTFET. Further, the impact of N_d on ambipolar I_{ds} was considered. Different N_d values were considered for a DG-LTFET with W_{rk_gate1} = 4.5 eV and W_{rk_gate2} = W_{rk_LTFET}, H_{g1} = $H_{nonoffset}$ = 40 nm, H_{g2} = H_{offset} − t_{ox} = 8 nm, and T_j = 5 nm, and the results are shown in Figure 11b. A drain doping level of 10^{18} cm^{-3} was found to suppress ambipolar I_{ds} appreciably without affecting the I_{ON}.



(**a**) (**b**)

Figure 10. I_{ds}-V_{gs} characteristics of DG-LTFET with different H_s, fixed W_{rk_gate1} = 4.5 eV, W_{rk_gate2} = W_{rk_LTFET}, and H_{g1} = H_s = $H_{nonoffset}$, H_{g2} = H_{offset} (=10 nm) − t_{ox} = 8 nm. (**b**) An I_{ON}/I_{OFF} ratio of I_{ds}-V_{gs} characteristics shown in (**a**). Red squares, green circles, blue triangles, magenta diamonds, and orange stars: H_s = 30, 35, 40, 45, and 50 nm, respectively.

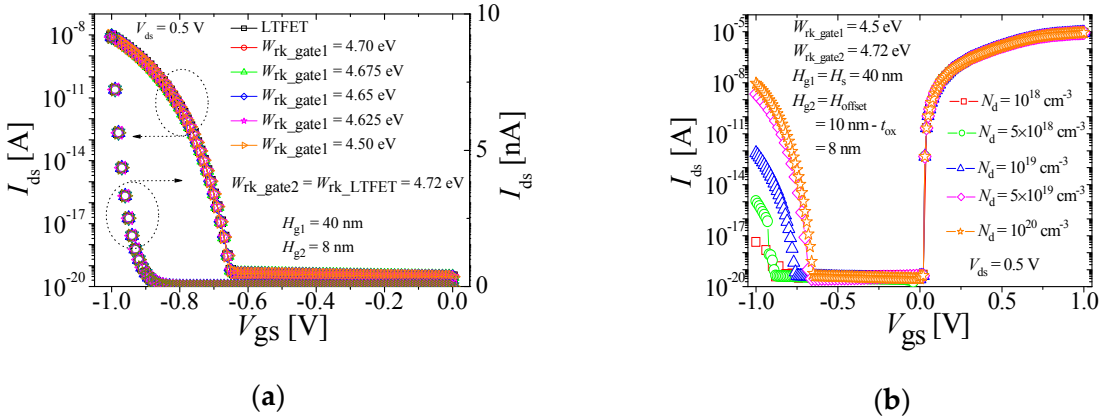


Figure 11. (**a**) I_{ds}-V_{gs} characteristics of DG-LTFET at V_{ds} = 0.5 V with different W_{rk_gate1} and W_{rk_gate2} = W_{rk_LTFET}, H_{g1} = H_{offset} = 10 nm, H_{g2} = 8 nm, T_j = 5 nm and N_d = 10^{20} cm^{-3}. Red circles, green triangles, blue diamonds, magenta stars, and orange right triangles: W_{rk_gate1} = 4.7, 4.675, 4.65, 4.625, and 4.5 eV. (**b**) DG-LTFET I_{ds} with different N_d. N_d = 10^{18} cm^{-3} demonstrates almost negligible ambipolar I_{ds}. Red squares, green circles, blue triangles, magenta diamonds, and orange stars: N_d = 10^{18}, 5 × 10^{18}, 10^{19}, 5 × 10^{19}, and 10^{20} cm^{-3}.

4. Conclusions

The device physics of the LTFET was investigated. It was found that a large part of the subthreshold region is dominated by the parasitic, lateral, 2D BTBT from the source to R_{offset} with a lower G_{tun}. The more efficient 1D BTBT from the source to $R_{nonoffset}$, with a higher G_{tun} takes place at a higher bias in the subthreshold region. In other words, the condition, that is, $V_{th\_Rnonoffset} > V_{th\_Roffset}$, exists in the LTFET. With $R_{nonoffset}$ not conducting the device does not utilize its channel fully during the subthreshold region. A new type of device based on the LTFET was introduced in this work. The device uses a dual gate structure with $W_{rk\_gate1} < W_{rk\_gate2}$. This increases the potential in $R_{nonoffset}$ and lowers $V_{th\_Rnonoffset}$. The DG-LTFET reverses the threshold condition of the LTFET, that is, it lowers $V_{th\_Rnonoffset}$ and makes it $<V_{th\_Roffset}$. $R_{nonoffset}$ with higher G_{tun} turns on earlier than R_{offset} in the subthreshold region in the DG-LTFET and the device exhibits an SS of less than 10 mV/dec. It was found that W_{rk_gate1} in the DG-LTFET needs to be sufficiently less than W_{rk_gate2} to achieve the sub 10 mv/dec SS. It was found that I_{ds} and SS are independent of $H_{g1/2}$. The DG-LTFET was further evaluated for different device dimensions including T_j and H_s while maintaining the electric field vector distribution equivalent. I_{ds} decreases with an increase in T_j and scales with H_s. The N_d value of 10^{18} cm^{-3} was found to appreciably reduce ambipolar I_{ds}. With the results presented in this work, the DG-LTFET could be considered as a viable potential replacement to conventional MOSFET and 3D integrations [16].

Author Contributions: Conceptualization, F.N. and Y.S.Y.; methodology, F.N. and Y.S.Y.; investigation, F.N. and Y.S.Y.; data curation, F.N.; writing—original draft preparation, F.N.; writing—review and editing, F.N., and Y.S.Y.; supervision, Y.S.Y.; project administration, Y.S.Y.; funding acquisition, Y.S.Y.

Funding: This research was funded by Ministry of Trade, Industry & Energy (MOTIE), project number 10054888 and Korea Semiconductor Research Consortium (KSRC) support program for the development of future semiconductor devices.

Acknowledgments: This work was supported by IDEC (EDA tool).

Conflicts of Interest: The authors declare no conflict of interest. The funders had no role in the design of the study; in the collection, analyses, or interpretation of data; in the writing of the manuscript; or in the decision to publish the results.

References

1. Avci, U.E.; Morris, D.H. Tunnel field-effect transistors. *IEEE J. Electron. Devices Soc.* **2015**, *3*, 88–95. [CrossRef]
2. Ionescu, A.M.; Riel, H. Tunnel field-effect transistors as energy efficient electronic switches. *Nature* **2011**, *479*, 329–337. [CrossRef] [PubMed]
3. Kim, S.W.; Kim, J.H.; Liu, T.K.; Choi, W.Y.; Park, B. Demonstration of L-shaped tunnel field-effect transistors. *IEEE Trans. Electron. Devices* **2016**, *63*, 1774–1778. [CrossRef]
4. Yang, Z. Tunnel field-effect transistor with an L-shaped gate. *IEEE Electron. Device Lett.* **2016**, *4*, 839–842. [CrossRef]
5. Imenabadi, R.M.; Saremi, M.; Vandenberghe, W.G. A novel PNPN-like Z-shaped tunnel field-effect transistor with improved ambipolar behavior and RF performance. *IEEE. Trans. Electron. Devices* **2017**, *64*, 4752–4758. [CrossRef]
6. Kim, S.W.; Choi, W.Y.; Sun, M.C.; Park, B.G. Investigation on the corner effect of L-shaped tunneling field-effect transistors and their fabrication method. *J. Nanosci. Nanotechnol.* **2016**, *9*, 6376–6381. [CrossRef]
7. *Sentaurus User Manual*; Version L-2016.03 March; Synopsys, Inc.: Mountain View, CA, USA, 2016.
8. Kao, K.H.; Verhulst, A.S.; Vandenberghe, W.G.; Soree, B.; Groeseneken, G.; Meyer, K.D. Direct and indirect band-to-band-tunneling in germanium-based TFETs. *IEEE Trans. Electron. Devices* **2012**, *59*, 292–301. [CrossRef]
9. Saxena, R.S.; Kumar, M.J. Dual-material gate technique for enhanced transconductance and breakdown voltage of trench power MOSFETs. *IEEE. Trans. Electron. Devices* **2009**, *56*, 517–522. [CrossRef]
10. Long, W.; Ou, H.; Kuo, J.-M.; Chin, K.K. Dual-material gate (DMG) Field Effect Transistor. *IEEE. Trans. Electron. Devices* **1999**, *46*, 865–870. [CrossRef]
11. Polishchuk, I.; Ranade, P.; King, T.-J.; Hu, C. Dual work function metal gate CMOS technology using metal interdiffusion. *IEEE Electron. Device Lett.* **2001**, *9*, 444–446. [CrossRef]
12. Sze, S.M.; Kwok, K.N. *Physics of Semiconductor Devices*, 3rd ed.; John Wiley & Sons: Hoboken, NJ, USA, 2006; ISBN 9780471143239.
13. Walke, A.M.; Verhulst, A.S.; Vandooren, A.; Verreck, D.; Simeon, E.; Rao, V.R.; Groeseneken, G.; Collaert, N.; Thean, A.V.Y. Part I: Impact of field-induced quantum confinement on subthreshold swing behavior of line TFETs. *IEEE Trans. Electron. Devices* **2013**, *60*, 4057–4064. [CrossRef]
14. Padilla, J.L.; Gamiz, F.; Godoy, A. A simple approach to quantum confinement in tunneling field-effect transistors. *IEEE Electron. Device Lett.* **2012**, *33*, 1342–1344. [CrossRef]
15. Padilla, J.L.; Alper, C.; Gamiz, F.; Ionescu, A.M. Assessment of field-induced quantum confinement in heterogate germanium electron-hole bilayer tunnel-field transistor. *Appl. Phys. Lett.* **2014**, *105*, 082108. [CrossRef]
16. Lim, S.K. Bringing 3D ICs to Aerospace: Needs for Design Tools and Methodologies. *J. Inf. Commun. Converg. Eng.* **2017**, *15*, 117–122. [CrossRef]