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Implementation of a Single-Phase SST for the Interface between a 13.2 kV MVAC Network and a 750 V Bipolar DC Distribution

Hyeok-Jin Yun [1,2], Dong-Keun Jeong [1,2], Ho-Sung Kim [2], Myoungho Kim [2], Ju-Won Baek [2], Ju-Yong Kim [3] and Hee-Je Kim [1,*]

1 Department of Electrical Engineering, Pusan National University, Busan 46241, Korea; yhj3409@naver.com (H.-J.Y.); jeongdk0731@nate.com (D.-K.J.)
2 Power Conversion and Control Research Center, HVDC Research Division, KERI, Changwon 51543, Korea; khsgt@keri.re.kr (H.-S.K.); mhkim@keri.re.kr (M.K.); jwbaek@keri.re.kr (J.-W.B.)
3 Smart Power Distribution Lab, Power Distribution ICT Group, Daejeon 305-760, KEPCO, Korea; juyong@kepco.co.kr
* Correspondence: heeje@pusan.ac.kr; Tel.: +82-51-510-2364

Received: 12 April 2018; Accepted: 30 April 2018; Published: 4 May 2018

Abstract: This paper presents the implementation of a single-phase solid-state transformer (SST) for the interface between a 13.2 kV medium voltage alternative current (MVAC) network and a 750 V bipolar DC distribution. The SST has ten cascaded subunits in consideration of the device rating and modulation index (MI). Each subunit consists of an AC/DC stage and a DC/DC stage with a high frequency isolated transformer (HFIT). The AC/DC stage consists of cascaded H-bridges (CHBs) to cope with the MVAC. The DC/DC stage employs a triple active bridge (TAB) converter for bipolar DC distribution. Topology analysis and controller design for this specific structure are discussed. In addition, the insulation of HFIT used in DC/DC converters is also discussed. A simple balancing controller at the AC/DC stage and a current sharing controller at the DC/DC stage are used to prevent DC-link voltage unbalance caused by the cascaded structure. The discussions are validated using a 150 kW single-phase 21-level SST prototype at the laboratory level.

Keywords: balancing controller; CHB; DAB; SST

1. Introduction

In recent decades, DC distribution has received increased attention for many applications because it is considered advantageous and superior to AC distribution in some cases, such as interfacing between renewable energy sources and DC loads, lower line losses, and so on [1–5]. There are two types of DC distribution systems: unipolar distribution and bipolar distribution. This paper focuses on the bipolar system due to its prominent advantages. The bipolar DC system can provide different voltage levels to loads, which allows connecting high- and low-power devices at a suited voltage level. In addition, this concept reduces the voltage level with respect to ground, which makes the distribution system safer for users [6]. To construct a bipolar DC distribution system with these many advantages, there is a need for additional power conversion devices that can be connected to an already existing AC grid.

The SST based on power electronics is a popular scheme to access to the AC grid and DC distribution system. It decreases the size of the system and provides instantaneous voltage regulation, bidirectional power flow, voltage sag and reactive power compensations, harmonic reduction, and so on [7–10].

Many researchers have developed some prototypes to implement SSTs. For example, Ref. [11] introduced a 7.2 kV 20 kVA single-phase SST prototype with customized 6.5 kV 25 A dual insulated

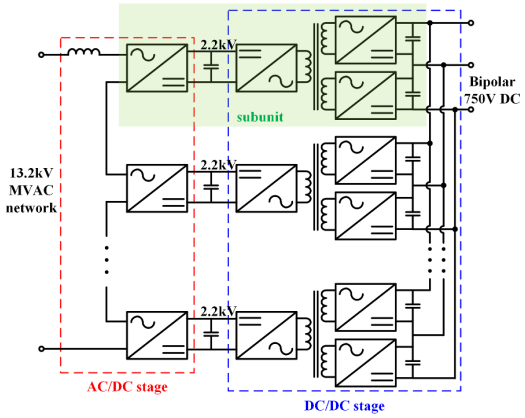
gate bipolar transistor (IGBT) packages for high-voltage and low-current application, and Ref. [12] presented a 3.3 kV 300 kVA back-to-back three-phase SST prototype for universal and flexible power management. In Ref. [13], a 15 kV 1.2 MVA single-phase SST prototype was designed for a railway grid. These prototypes have different structures depending on the purpose of use. In other words, the SST prototypes were designed to be suitable for specific applications.

This paper introduces a single-phase 150 kW prototype of an SST for the connection between a 13.2 kV MVAC grid and a bipolar 750 V DC distribution system. This SST prototype consists of an AC/DC stage and a DC/DC stage. The AC/DC stage employs the CHB rectifiers and is responsible for power factor control, voltage regulation, and the voltage balancing of DC-links. The DC/DC stage employs a specially designed TAB converter for connecting to the bipolar DC distribution system. In addition, it is responsible for voltage control, and current sharing in parallel-connected outputs. This paper also discusses the insulation of the HFIT used in the TAB converter.

The rest of this paper is organized as follows: the overall structure of the SST system used in this paper is briefly introduced in Section 2. Section 3 provides the details about the controller of AC/DC stage for the voltage balancing of DC-links. In Section 4, the DC/DC stage is analyzed including the characteristics of the topology, modeling, and controller design. In Section 5, the HFIT design for high-voltage insulation is discussed. The simulations and experimental results using a 150 kW SST prototype are presented in Sections 6 and 7, respectively. Finally, the conclusions are provided in Section 8.

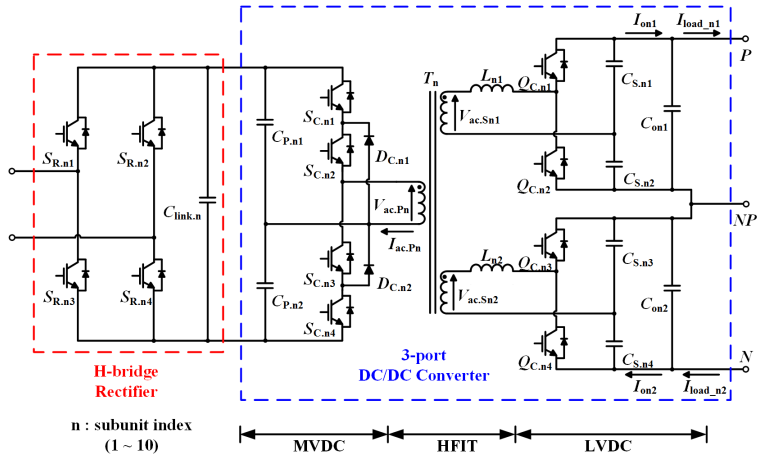
2. Structure of the SST Prototype

The upstream grid is a 13.2 kV single-phase MVAC network, but the loads work under the 750 V bipolar DC distribution system. To meet this requirement, the SST prototype is assembled by several subunits that are connected in a cascaded structure (as shown in Figure 1a). Figure 1b shows one subunit consisting of one H-bridge rectifier and one TAB converter. The AC/DC stage is realized using an interfacing inductor and several CHB rectifiers to support the 13.2 kV MVAC. The DC/DC stage consists of three parts, which, organized from left to right, are the medium voltage direct current (MVDC), HFIT, and low voltage direct current (LVDC). On the MVDC side, a neutral point clamped (NPC) circuit is employed to handle a DC-link voltage higher than the rating of semiconductor devices. The NPC generates a 3-level voltage to the HFIT, where the voltage applied to the semiconductor devices is half of the DC-link. In addition, for application to bipolar DC distribution, the HFIT coupled with three windings and the LVDC side is configured as a multi-terminal in which two half-bridge circuits are connected in series. The outputs of the DC/DC stage are connected in parallel, and each subunit has to be rated for only a fraction of the full power.



(**a**)

Figure 1. *Cont.*



(**b**)

Figure 1. Structure of the SST prototype system: (**a**) simplified structure of the overall SST prototype system; (**b**) detailed structure of one subunit.

The voltage of the DC-link is controlled to 2.2 kV in consideration of the topology and the rating of the semiconductor device. In this case, a minimum of ten modules are needed to take into account the line voltage [14], the second harmonic ripple in the DC-link voltages, and the margin reserved for the control strategy [15].

3. A Simple and Practical Voltage Balancing Controller for CHB

One of the main problems that arises when the AC/DC rectifier stage is configured as CHBs in a SST system is the voltage imbalance between DC-links. This imbalance can be caused by unbalanced load conditions, mismatch of the active and passive components, or the floating structure of the high voltage DC-links [16–19]. This imbalance also increases the stress of the semiconductor device and causes over-voltage or over-current problems that can lead to the collapse of the entire system. The imbalance issue particularly worsens when the SST operates under no load or light load conditions because a small power difference is a significant percentage of the real power and will result in a large voltage imbalance.

To avoid this imbalance problem, an adequate control strategy should be needed to adjust the amount of active power transferred to the individual DC-links. There are several references including control strategies to solve the voltage imbalance of DC-links. In Ref. [20], based on a single-phase d–q control, a voltage balancing controller that adjusts the individual modulation signals is proposed to balance the DC-links. Ref. [21] presented an individual voltage balancing strategy for single-phase STATCOM devices that is based on the CHB multi-level topology. This balancing technique achieves control and balance of the individual DC-links, maintaining among them an equal distribution of the reactive power provided by the H-bridges. In Ref. [22], a voltage balancing controller in the d–q coordinate is proposed to reduce the coupling effect between the voltage balancing controller and the original system controller for the single phase CHB multi-level topology. However, these conventional methods require additional balancing controllers as many as the number of CHB modules. Therefore, as the number of modules increases, the computation time of the additional balancing controllers increases.

In this paper, a simple and practical voltage balancing controller for DC-links is proposed. The proposed balancing controller does not require additional sensors, and no additional control loops required for module expansion. The entire control block diagram for an AC/DC stage is shown in Figure 2. The controller is divided into three parts. The first part is the voltage error compensator for total DC-links. This voltage error compensator is responsible for rectifying MVAC to MVDC. In this process, the voltage error compensator only controls the voltage of the total DC-links, so an additional controller is required for voltage balancing between individual DC-links. The second part is

the balancing controller for DC-links. The balancing controller monitors the voltage of all DC-links and sorts them in order of magnitude. Through this sorting process, the maximum voltage and the minimum voltage are obtained. A compensation value proportional to the difference between these two values is generated for DC-link balancing, as shown in the following equations:

$$I^*_{\mathrm{AC\_max\_mag}} = I^*_{\mathrm{AC\_mag}} - K_{\mathrm{p}} \cdot (V_{\mathrm{O\_max}} - V_{\mathrm{O\_min}}), \tag{1}$$

$$I^*_{\mathrm{AC\_min\_mag}} = I^*_{\mathrm{AC\_mag}} + K_{\mathrm{p}} \cdot (V_{\mathrm{O\_max}} - V_{\mathrm{O\_min}}). \tag{2}$$

According to the Figure 2 and Equations (1) to (2), the balancing controller transfers more active power to the DC-link with minimum voltage and less active power to the DC-link with maximum voltage. The voltage deviation of the individual DC-links gradually converges to zero over the processes of voltage sorting, detection of maximum and minimum values, and compensation of active power. The last part is the current error compensator. The current error compensator is responsible for power factor control between the grid voltage and current. The proportional-resonant (PR) controller is used to improve the total harmonic distortion (THD) of the single-phase current and to reduce the steady state error [23]. Finally, the AC current reference values from the current error compensator were applied to the CHB by the phase shift pulse width modulation (PSPWM) scheme for ease of expansion and implementation [24].

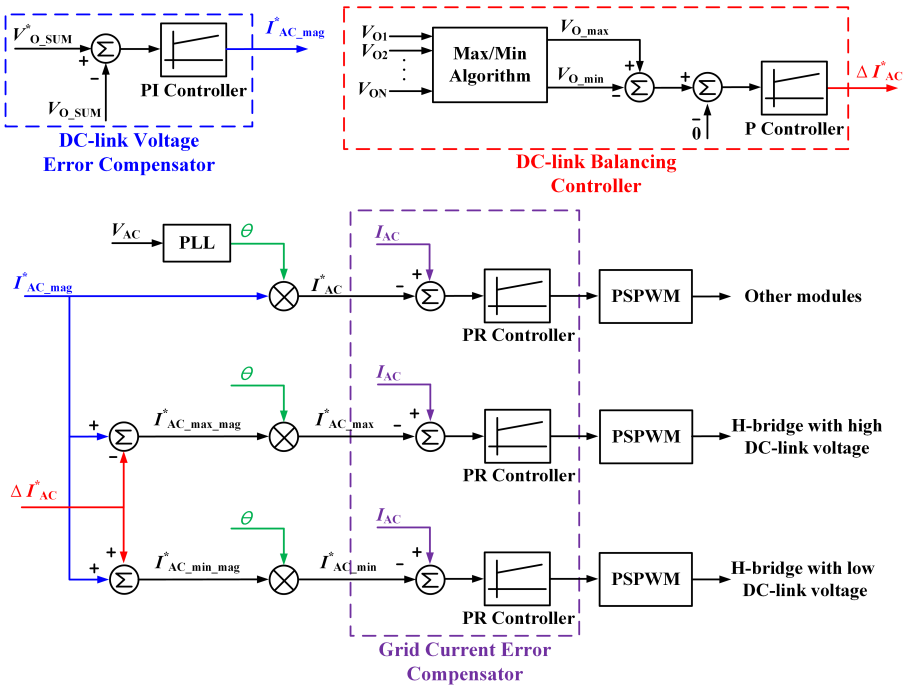


Figure 2. The entire control block diagram for AC/DC stage.

4. Analysis of the TAB Converter

The dual active bridge (DAB) converter has been widely used because of its various advantages such as high power density, bidirectional power flow, galvanic isolation, and so on [25,26]. Most DAB converters consist of half-bridge or full-bridge circuits, which produce 2-level square waves across the HFIT. These 2-level DAB converters are usually cascaded for medium and high voltage applications [27,28]. In this structure, the individual voltage of DC-links cannot be higher than the voltage rating of the switching devices used in the 2-level DAB converters. Therefore, there is a disadvantage in that the number of required subunits increases due to the voltage rating of the switching devices when 2-level DAB converters are cascaded in an SST system.

The 3-level DAB converters can overcome this voltage constraint of semiconductor switches to a great extent. Power converters synthesizing more than two voltage levels, such as NPC, and flying capacitor converter (FCC), are traditionally known as 3-level converters. The FCC has a disadvantage in that a complicated switching scheme is required to keep the flying capacitor voltage charged at the appropriate constant level [29]. On the other hand, NPC has an advantage in that all of the switching devices in a leg withstand only half of the individual DC-link voltage using simple switching scheme. Therefore, in this paper, a 3-level NPC circuit is employed on the primary side of the DC/DC converter.

The loads of this DC/DC converter should work under a bipolar DC distribution system. To simply meet this requirement, two 2-port DC/DC converters can be connected in parallel to the individual DC-link. However, this structure has the disadvantage of increasing the number of HFITs and converters. In addition, when a power transfer occurs between the two bipolar DC outputs, the losses are increased because the circulating power is transmitted through two primary circuits. Therefore, the TAB converter using a three windings coupled transformer is advantageous for bipolar DC distribution. Studies have been conducted to expand to a TAB converter using 2-level DAB converters [30,31].

However, unlike the conventional 2-level TAB, the TAB converter used in this paper is configured as follows: a 3-level NPC circuit on the primary side, a three windings coupled transformer, and a secondary side is configured as a multi-terminal in which two half-bridge circuits are connected in series (as shown in Figure 1b). In addition, the outputs of the each TAB converter are connected in parallel, and each subunit has to be rated for only a fraction of the full power.

This section discusses the modeling and controller design procedure of the TAB for this particular structure.

4.1. Modeling of the Three Windings Coupled Transformer

Conceptually, the 2-port DAB converter can be viewed as an interfacing inductor driven at either end by a controlled square-wave voltage source [32]. In the 2-port DAB converter, the interfacing inductance is the sum of the transformer leakage inductance and the external inductance that is needed in order to adjust the output power as well as to extend the zero-voltage switching operation [33]. The interfacing inductor between each port is a dominant parameter as the energy transfer component in the DAB converter [32,33]. Therefore, interfacing inductances between each port should be obtained for the power transfer modeling of the TAB converter.

Theoretically, the extended cantilever model (ECM) for the transformer is convenient in terms of the parameter extraction, since each model parameter can be extracted from a single measurement of an open-circuit voltage or a short-circuit current [34]. For this reason, the ECM is applied for the three windings coupled transformer to extract interfacing inductances between each port, as shown in Figure 3, where L_{W1} is the magnetizing inductance seen from the primary winding, W_1 (L_{ij}, i, j = 0∼2, $i \neq j$) is the leakage inductance between each pair of windings, and n_2 and n_3 are turns ratios and have the same value in this application.

The equivalent circuit of the TAB converter using an extended cantilever is shown in Figure 4, where ($L_{ij}^{'}$, i, j = 0∼2, $i \neq j$) is the leakage inductance between each pair of windings referred to secondary and tertiary sides, the 3-level voltage at its primary NPC circuit is referred to secondary and tertiary sides and it is denoted as V_0. V_1 and V_2 are the square-wave voltage at its secondary and tertiary bridges, respectively, and P_0 is the amount of power transferred from the DC-link to the input port. P_1 and P_2 are the amount of power supplied to each load from the bipolar output ports.

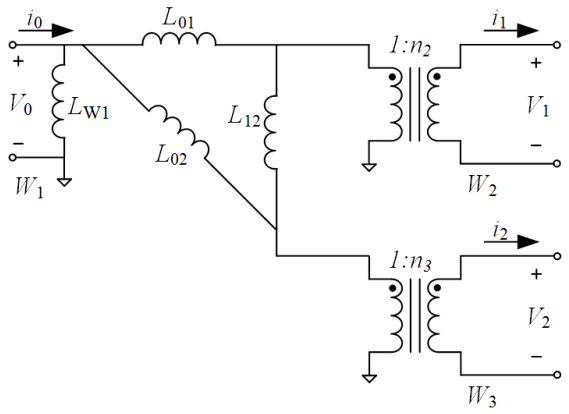


Figure 3. Extended cantilever model for the three windings coupled transformer.

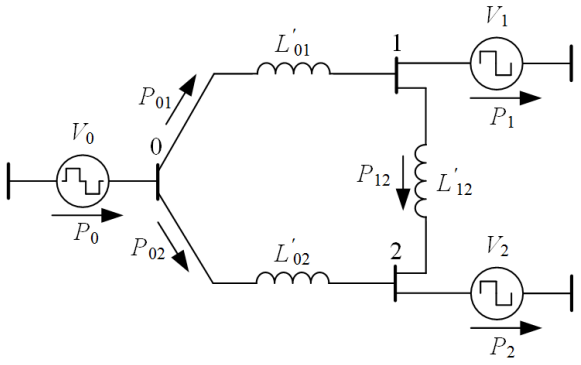


Figure 4. Equivalent circuit for the TAB converter.

4.2. Power Transfer Modeling of the TAB Converter

According to the equivalent circuit shown in Figure 4, it can be seen that the power flow paths between any two of the three ports P_{ij} (the power transferred from port i to port j; i, j = 0∼2, $i \neq j$). P_{01} and P_{02} are the power flow from the primary side to each bipolar output, respectively. They can be represented by the power flowing through the 2-port DAB converter, consisting of a primary NPC leg and a secondary half-bridge leg. Figure 5a,b show the theoretical voltage and current waveforms of this 2-port DAB converter, where $V_{ac.P}$ is the 3-level voltage produced by the primary NPC leg, α is half of the angular distance for zero state, $V_{ac.Sj}$ is the 2-level voltage produced by the secondary or tertiary half-bridge leg, ϕ_{0j} is the phase-shift angle between the active bridges, and V_{L0j} and I_{L0j} are the voltage and current of the interfacing inductor between port 0 and port j, respectively. I_{oj} is the current of the each bipolar output.

The switching scheme for the 2-port DAB converter with a 3-level NPC topology was presented in Refs. [35,36]. Based on the value of ϕ_{0j}, there may be two cases such as Case I: $0 \leq \phi_{0j} \leq \alpha$, Case II: $\alpha < \phi_{0j} \leq \pi/2$. Referring to Figure 5, the power equations for two cases can be obtained as follows:

$$\text{Case I}: P_{0j} = \frac{nV_0V_j}{2\omega L'_{0j}}\phi_{0j} \cdot (1 - \frac{2\alpha}{\pi}), \tag{3}$$

$$\text{Case II}: P_{0j} = \frac{nV_0V_j}{2\omega L'_{0j}} \cdot (\phi_{0j} - \frac{\phi_{0j}^2}{\pi} - \frac{\alpha^2}{\pi}), (j = 1, 2), \tag{4}$$

where ω is the switching angular frequency.

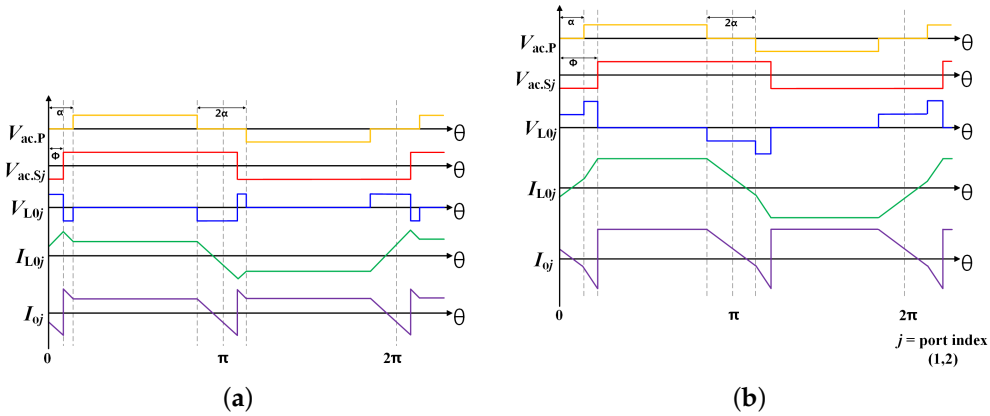


Figure 5. Theoretical waveforms of the 2-port DC/DC converter: (**a**) Case I ($0 \leq \phi_{0j} \leq \alpha$); (**b**) Case II ($\alpha < \phi_{0j} \leq \pi/2$).

According to Equations (3) and (4), the smaller the value of α, the more power can be transferred to the load. Therefore, α should theoretically have the minimum value for freewheeling. This means that the 2-port DAB converter with a 3-level NPC topology works in Case I over a very short interval in practice. In addition, the amount of power calculated by Equations (3) and (4) are almost the same under light load conditions. Considering the above statements, the power equation of the 2-port DAB converter with a 3-level NPC topology may be considered as the generalized equation and can be rewritten as follows:

$$\begin{aligned} P_{0j} \simeq \frac{nV_0V_j}{2\omega L'_{0j}} \cdot (\phi_{0j} - \frac{\phi_{0j}^2}{\pi}), \\ (j = 1, 2), \\ (0 \leq \phi_{0j} \leq \tfrac{\pi}{2}). \end{aligned} \tag{5}$$

Equation (5) is equivalent to the equation of a 2-level half-bridge DAB converter because the α term that generates the zero-state in the NPC leg is removed. Therefore, P_{12}, which is another power flow between two bipolar DC outputs, can also be obtained from Equation (5). As a result, in the TAB converter, the amount of power between any two of the three ports can be obtained from Equation (5). To reduce computing burden, (5) can be simplified as follows through the fundamental approximation in Ref. [32]:

$$\begin{aligned} P_{ij} \simeq \frac{4V_iV_j}{\pi^2\omega L'_{ij}} \cdot \phi_{ij}, \\ (i, j = 0 \sim 2, i \neq j), \\ (0 \leq \phi_{ij} \leq \tfrac{\pi}{2}). \end{aligned} \tag{6}$$

According to (6), the amount of power flowing through port 1 and port 2 are calculated as follows, respectively:

$$P_1 = P_{01} + P_{21} = (\frac{4V_0V_1}{\pi^2\omega L'_{01}} + \frac{4V_1V_2}{\pi^2\omega L'_{12}}) \cdot \phi_{01} - \frac{4V_1V_2}{\pi^2\omega L'_{12}} \cdot \phi_{02}, \tag{7}$$

$$P_2 = P_{02} + P_{12} = -\frac{4V_1V_2}{\pi^2\omega L'_{12}} \cdot \phi_{01} + (\frac{4V_0V_2}{\pi^2\omega L'_{02}} + \frac{4V_1V_2}{\pi^2\omega L'_{12}}) \cdot \phi_{02}. \tag{8}$$

Equations (7) and (8) can be rewritten in matrix form as follows:

$$\vec{P} = \vec{G} \cdot \vec{\phi}, \vec{P} = \begin{pmatrix} p_1 \\ p_2 \end{pmatrix}, \vec{\phi} = \begin{pmatrix} \phi_{01} \\ \phi_{02} \end{pmatrix}, \vec{G} = \begin{pmatrix} g_{11} & g_{12} \\ g_{21} & g_{22} \end{pmatrix}, \tag{9}$$

where $\vec{G}$ is the transfer function matrix that describes the system parameters.

As shown in (9), the TAB converter is a two-input and two-output (TITO) system. The TITO system is characterized by significant interactions between their inputs and outputs. Because of these interactions, a control action in one loop gets transmitted to the other loop as a disturbance. Therefore, decoupling techniques are required to eliminate or minimize the interaction. The simplified decoupling technique is most widely used in practice because of its robustness and simple decoupling network for TITO systems [37]. Figure 6 shows the control block diagram with simplified decoupling. The decoupler transfer function matrix $\vec{D}$ and the decoupled transfer function matrix $\vec{T}$ can be given as in (10) and (11), respectively:

$$\vec{D} = \vec{G}^{-1} \cdot \vec{T} = \begin{pmatrix} 1 & -\frac{g_{12}}{g_{11}} \\ -\frac{g_{21}}{g_{22}} & 1 \end{pmatrix}, \tag{10}$$

$$\vec{T} = \begin{pmatrix} g_{11} - \frac{g_{12}g_{21}}{g_{22}} & 0 \\ 0 & g_{22} - \frac{g_{12}g_{21}}{g_{11}} \end{pmatrix}. \tag{11}$$

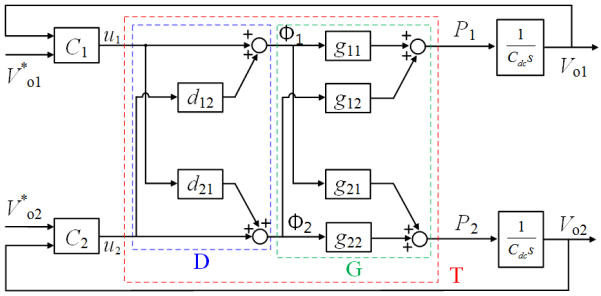


Figure 6. Control block diagram with simplified decoupling.

4.3. Controller Design

After applying the simplified decoupling, the decoupled controller is represented by two single-input and single-output (SISO) controllers as shown in Figure 7. Two SISO controllers hold each bipolar DC output voltage at a set point by automatically adjusting control signals as follows. The reference voltage and the measured voltage are given as inputs to the comparator, from which an error signal is passed as input to the integral proportional (IP) controller. The use of the IP controller enhances the system dynamic response and reduces undesirable peak overshoot compared to the proportional integral (PI) controller [38]. The IP controller generates the control signal based on the error signal. The output of the IP controller sets the output current of the converter required to keep the output capacitor voltage at the appropriate constant level. In addition, a load current feedforward is added into the controller to improve the dynamic response against the load changes [39].

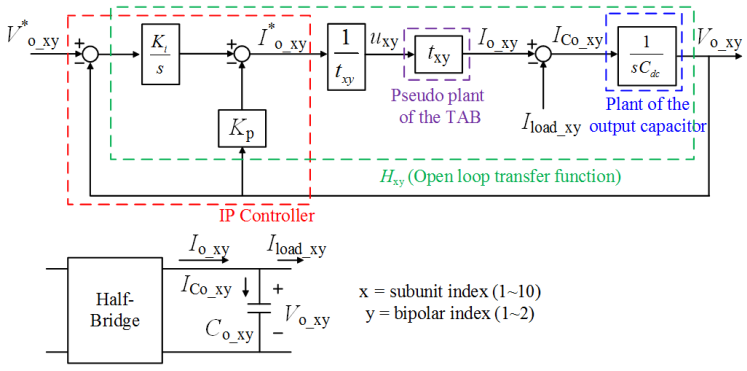


Figure 7. Block diagram of the voltage controller converted to SISO system.

Using the formula of the IP controller and the mathematical relationship between the voltage and current of the capacitor, the closed-loop transfer function is given by:

$$H(s) = \frac{V_{oj}}{V_{oj}^*} = \frac{\frac{K_i}{C_{oj}}}{s^2 + \frac{K_p}{C_{oj}}s + \frac{K_i}{C_{oj}}}, \tag{12}$$

where C_{oj} is the output capacitance, K_p and K_i, all non-negative, denote the coefficients for the proportional and integral terms, respectively. To order the closed-loop system, it is necessary to choose the coefficients K_p and K_i.

The transfer function of a second-order system in standard form is given by:

$$F(s) = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}. \tag{13}$$

By comparing (12) and (13), the resulting IP controller parameters are obtained by:

$$\begin{aligned} K_p &= 2\zeta\omega_n^2 C_{oj}, \\ K_i &= C_{oj}\omega_n^2, \end{aligned} \tag{14}$$

where ζ is the damping factor and ω_n is the natural frequency.

The outputs of the DC/DC stage are connected in parallel, and each subunit has to be rated for only a fraction of the full power. The primary goal of these parallel-connected converters is to share the load current among the constituent converters. Improper load sharing can lead to the converter overloading and overheating, which decreases the system reliability and can eventually lead to the failure of the overall system [40]. Therefore, a robust control technique that ensures synchronizing and proper load sharing is essential to ensure the stability and reliability of the system. Figure 8 shows the control block diagram of the current-sharing controller based on the outer loop regulation (OLR) mode studied in Ref. [41]. The OLR mode uses the current-sharing error signal to adjust the voltage reference of the outer voltage loop until equal load current distribution is achieved. The current data of each module is transmitted via the CAN protocol, and the average current value can be calculated based on this information. The current-sharing error signal is processed through the average current method (ACM), which compares the difference between the average current and the individual current. The key features of the scheme, generally, are that the reference voltage, output voltage feedback, and the voltage compensator of each converter module are independent.

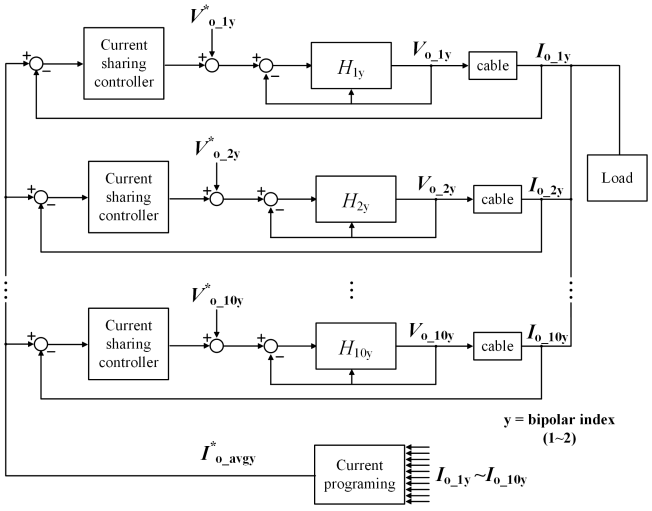


Figure 8. Control block diagram of current sharing controller.

5. Transformer

The primary windings of the HFIT are electrically connected to the 13.2 kV MVAC network, as shown in Figure 1a. In addition, the secondary and tertiary windings of the HFIT are electrically connected to the 750 V bipolar LVDC and are floated with respect to the ground of the MVAC network. In this structure, the minimum requirement of dielectric strength between the primary and other windings is 22 kV, which corresponds to the total DC-link voltage [42]. Similarly, the minimum requirement of dielectric strength between the core and windings is 22 kV. The dielectric strength of the HFIT was selected to be 50 kV, which is about 2.3 the former strength of 22 kV, according to the IEEE standard in Ref. [43].

Figure 9 shows the guard and bobbin structure of the HFIT to ensure the high dielectric strength. The guard provides an electrical insulation between the core and the windings. The bobbin provides an electrical insulation between the windings through the section structure. Both guard and bobbin were made of Teflon material considering processability, low permittivity, and high voltage insulation [44]. The thickness of the insulator was determined by electric field distribution and intensity, which is difficult to calculate due to the nonuniform electric field. Therefore, to determine the thickness of the guard and section layer, the electric field distribution and intensity were simulated via ElecNet as shown in Figure 10. Based on the structure of Figure 9, the thickness of guard and section layer was temporarily set to 5 mm and 50 kV is applied between the primary and other windings. It can be seen that the maximum field strength induced in the guard and section layer was 17 kV/mm, while the dielectric strength of Teflon material is usually 20 kV/mm in vacuum. Therefore, the thickness of the guard and section layer was selected as 5 mm considering margin. In addition, the empty space between the bobbin, guard, and windings was filled with molding fluid to prevent partial discharge and surface discharge. SYLGARD 170 A/B was selected as the molding fluid, considering the thermal conductivity, dielectric strength, viscosity [45].

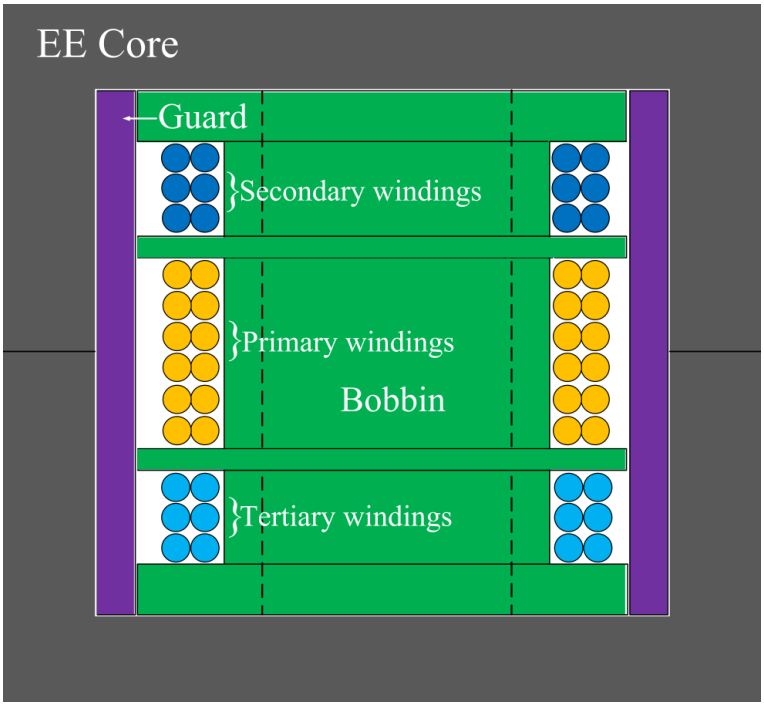


Figure 9. Arrangement of windings and structure of bobbin.

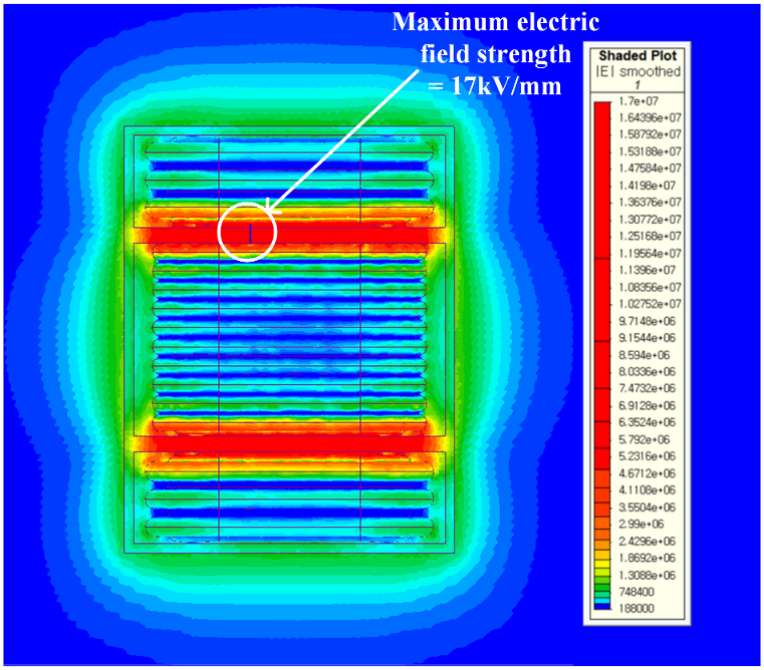


Figure 10. Electric field simulation results of section bobbin structure.

6. Simulation

Figure 11 shows the simulation waveform employed to verify the DC-link voltage balancing capability of the AC/DC stage. Simulation parameters are listed in Table 1. The AC/DC stage was realized using an interfacing inductor and ten CHB rectifiers to support the 13.2 kV MVAC. As mentioned in Section 3, this structure can cause the voltage imbalance between DC-links. The simulation sequence is as follows. Initially, the active power flowing through all of the CHB rectifiers is 150 kW (rated power) and the voltage imbalance is caused by unbalanced load conditions (up to 20%). The voltage of DC-links remains unbalanced because the balancing algorithm is forcedly deactivated until t = 0.4 s. The balancing algorithm is activated at t = 0.4 s, and the voltage of DC-links gradually converges to 2.2 kV. At t = 0.6 s, the load of subunit10 is increases from 13.6 kW to 15.8 kW, and the load of subunit6 is reduced from 16.6 kW to 14.4 kW. At t = 0.8 s, the CHB rectifiers act like an inverter to transfer 150 kW of power from the DC-links to the MVAC. It can be seen that the DC-link voltage is balanced in all sequences after the balancing algorithm is activated.

Figure 12 shows the simulation waveform used to verify the decoupling capability of the DC/DC stage. Simulation parameters are also listed in Table 1. The simulation sequence is as follows. At t = 0.1 s, the voltage reference of port 1 is changed from 720 to 750. At t = 0.14 s, the voltage reference of port 2 is changed from 780 to 750. At t = 0.18 s, the load of port 1 is increased from no load to full load (7.5 kW) in a stepwise manner. At t = 0.22 s, the load of port 2 is also increased from no load to full load (7.5 kW). At t = 0.26 s, full power is injected into the power grid through port 1 (−7.5 kW). At t = 0.3 s, full power is injected into the power grid through port 2 (−7.5 kW). It can be seen that two SISO controllers hold each bipolar DC output voltage at a set point in all sequences. In addition, the results indicate that interactions between their inputs and outputs are well suppressed.

Figure 13 shows the simulation waveform employed to verify the current sharing controller of the DC/DC stage. In the simulation, the number of output parallel-connected TAB converters is limited to two because of the computing burden. At t = 0.06 s, the improper load-sharing is caused by the non-identical voltage sensors (difference up to 2%). Initially, improper load-sharing occurs, but soon all load currents gradually converge to their average value. In addition, at a random timing, the load of each port is increased from no load to full load and full power is injected into the DC-links through

TAB converters. It can be seen that the load sharing is good in all sequences after the current sharing controller is activated.

Table 1. System parameters.

Parameter	Symbol	Value	Unit
Number of subunits		10	
Line inductance	L_{in}	40	mH
DC capacitance in DC-link	C_{link}	370	uF
Rated DC voltage of DC-link	V_{link}	2.2	kV
Switching frequency of the AC/DC stage	$f_{sw.rec}$	1.8	kHz
DC capacitance in LVDC	C_o	1	mF
Rated DC voltage of LVDC	V_o	±750	V
Switching frequency of the DC/DC stage	$f_{sw.conv}$	10	kHz
HFIT turn ratio	n	0.34	
Interfacing inductance between MVDC and LVDC	L_{0j}	140	uH

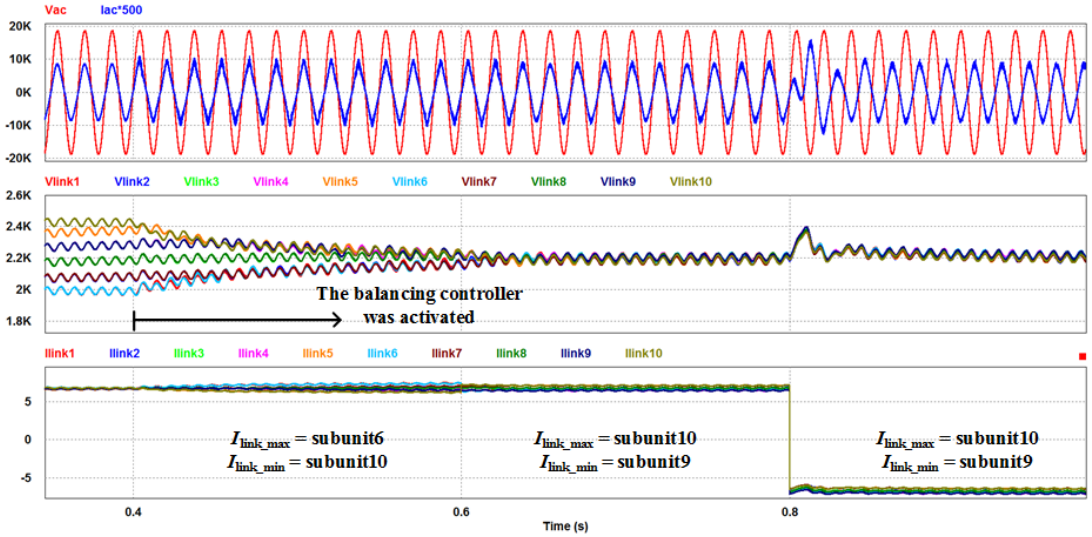


Figure 11. Simulation waveform to verify the voltage balancing capability of the AC/DC stage.

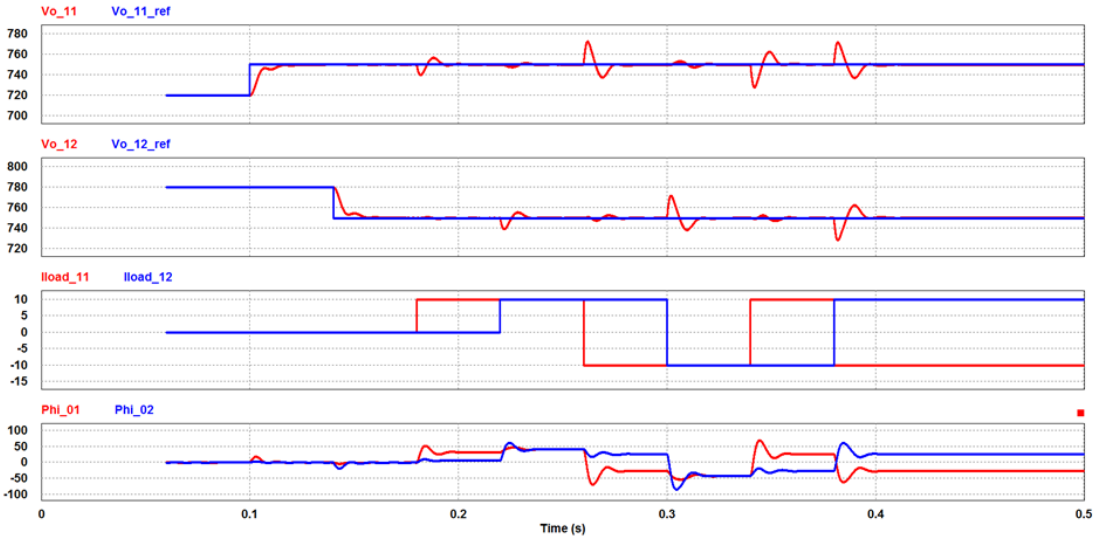


Figure 12. Simulation waveform to verify the decoupling capability of the DC/DC stage.

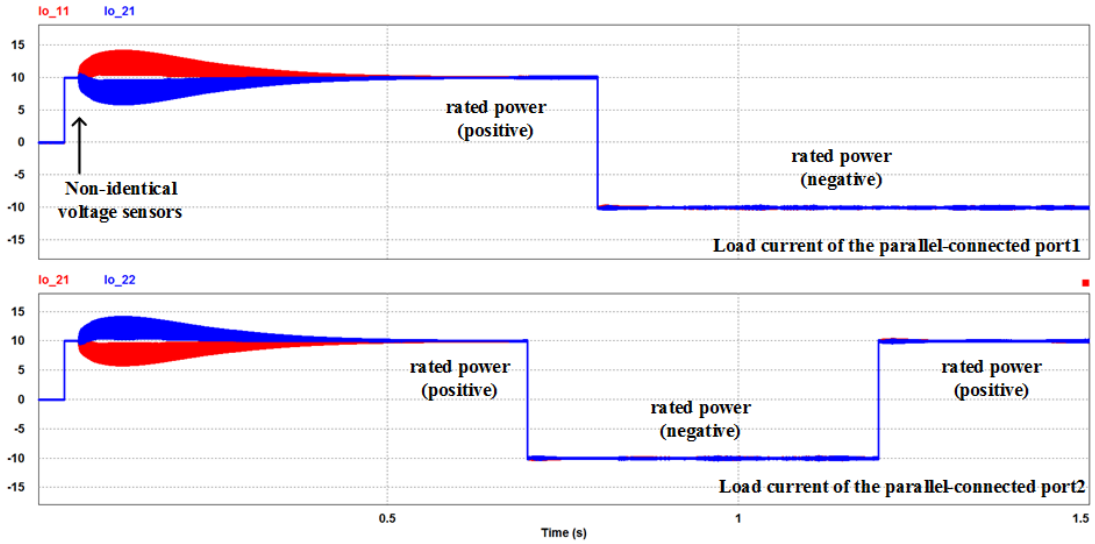


Figure 13. Simulation waveform to verify the current sharing controller.

7. Experiment

In order to test the hardware and software beyond the numerical simulations, a 150 kW single-phase 21-level SST prototype was designed and assembled, and is shown in Figure 14. As mentioned in Section 2, the AC/DC stage was realized using an interfacing inductor and ten CHB rectifiers to support the 13.2 kV MVAC. In the DC/DC stage, for application to bipolar DC distribution, the HFIT coupled with three windings and the LVDC side is configured as a multi-terminal in which two half-bridge circuits are connected in series. The outputs of DC/DC stage are connected in parallel, and ten subunits have to be rated for only a fraction of the full power. The entire operation of the SST system was programmed by DSP and CPLD processors. The AC/DC stage and DC/DC stage have its own DSP and CPLD controllers. The required data between them is shared by CAN protocol. The parameters adopted in both simulation and experiment are the same.

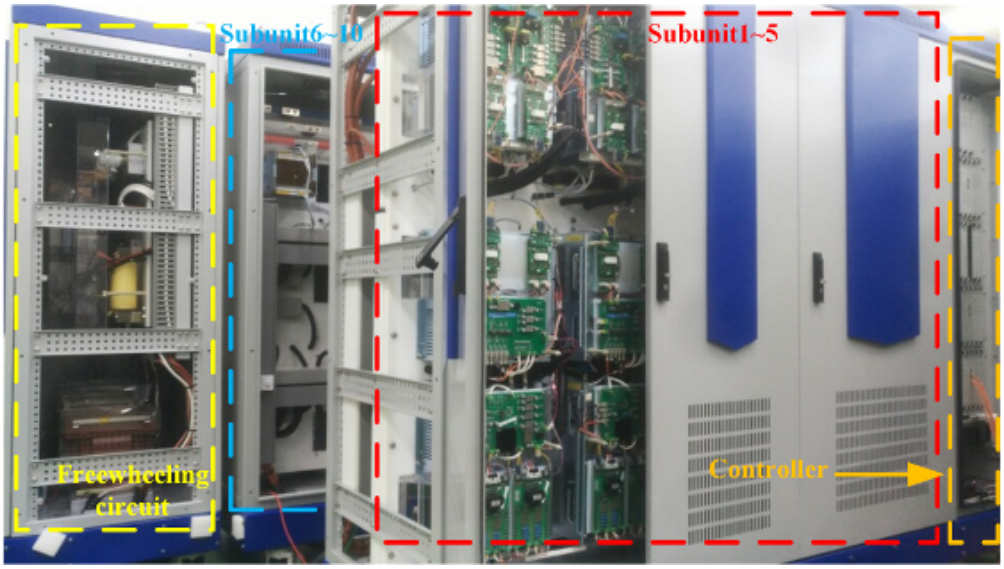


Figure 14. Single-phase 21-level SST prototype.

Figure 15 shows a waveform used to verify the DC-link voltage balancing capability of the AC/DC stage. Due to the limitations of the measuring equipment, only V_{dclink1}~V_{dclink3} was measured by the oscilloscope. The remaining voltage of DC-links was monitored via software such as LabVIEW (Ver 13.0, National Instrument, Austin, TX, USA). It can be seen that the voltage of DC-links was initially unbalanced due to finite tolerances in the power stage and control parameters when the balancing controller was deactivated. However, the voltage of DC-links started converging to set point after the balancing controller was activated. This indicates that the balancing controller works properly.

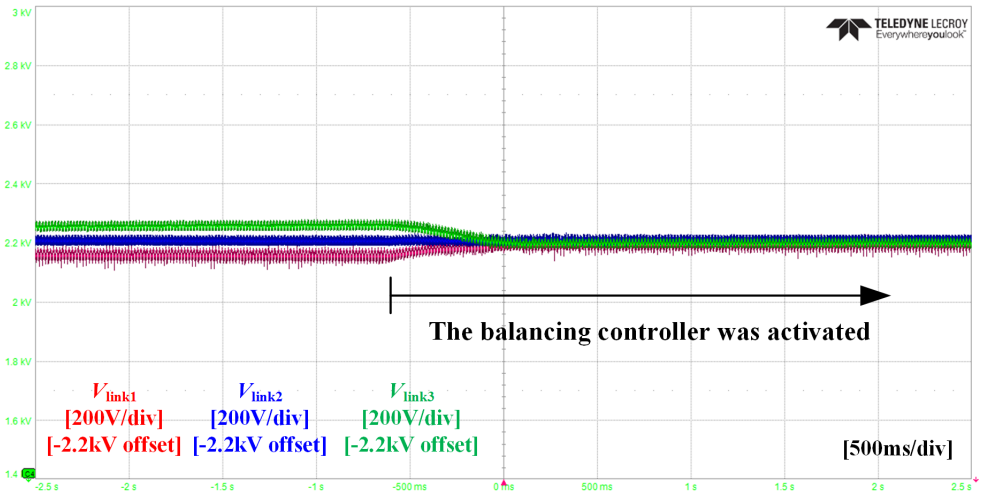


Figure 15. DC-link voltage waveform when balancing controller is activated.

The steady-state waveform of a TAB converter in several load conditions are depicted as follows. Figure 16a shows a waveform when the TAB converter is operating under no load conditions. Figure 16b shows a waveform when the amount of power transferred from port 1 to load is 7.5 kW, while port 2 has no load. Figure 16c shows a waveform when the amount of power transferred from port 2 to load is 7.5 kW, while port 1 has no load. Figure 16d shows a waveform when the amount of power transferred from each port to load is 7.5 kW (total 15 kW, rated power of one subunit). The TAB converter holds each bipolar DC output voltage at a set point in several load conditions. In addition, the experimental voltage and current waveforms have a close match with the aforementioned analysis in Section 4.

Figure 17 shows a waveform used to verify the decoupling capability of the TAB converter. The loads of each port are changed in a stepwise manner at a random timing. Due to the limitation of the load device, the load that is changed stepwise on each port is limited to a maximum of 20 kW. It can be seen that the result indicates that interaction between each port is well suppressed.

The paralleling experiment performed to verify the current-sharing controller of the DC/DC stage is as follows. The number of output parallel-connected TAB converters was ten. However, there are two limitations to measure the waveforms at the laboratory level. First, only the output currents of five subunits are measured in the oscilloscope due to the limitations of the measuring equipment. The remaining output currents were monitored via software such as LabVIEW. Second, due to the limitation of the load device, the amount of power transferred from the ten subunits to loads was limited to 50 kW, which corresponds to 1/3 of the rated power. The rated operation of the SST prototype will be verified later through a field test. Figure 18a,b show the current waveforms of the bipolar DC/DC output stage (denoted as $I_{\text{o\_1}y}$, $I_{\text{o\_2}y}$, y is the subunit index, y = 1~5). It can be seen that all output currents remain balanced under various load conditions.

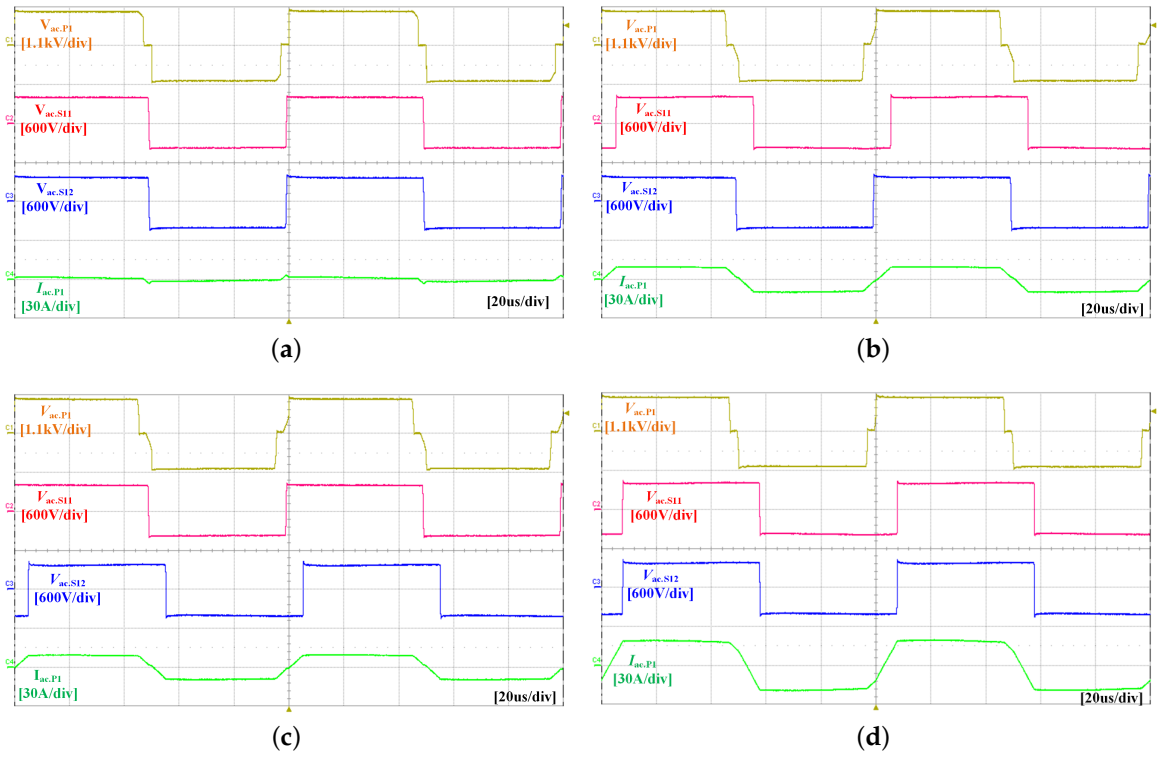


Figure 16. Steady-state waveform of a TAB converter: (**a**) under the no load condition; (**b**) when the amount of power transferred from port 1 to load is 7.5 kW; (**c**) when the amount of power transferred from port 2 to load is 7.5 kW; (**d**) when the amount of power transferred from each port to load is 7.5 kW.

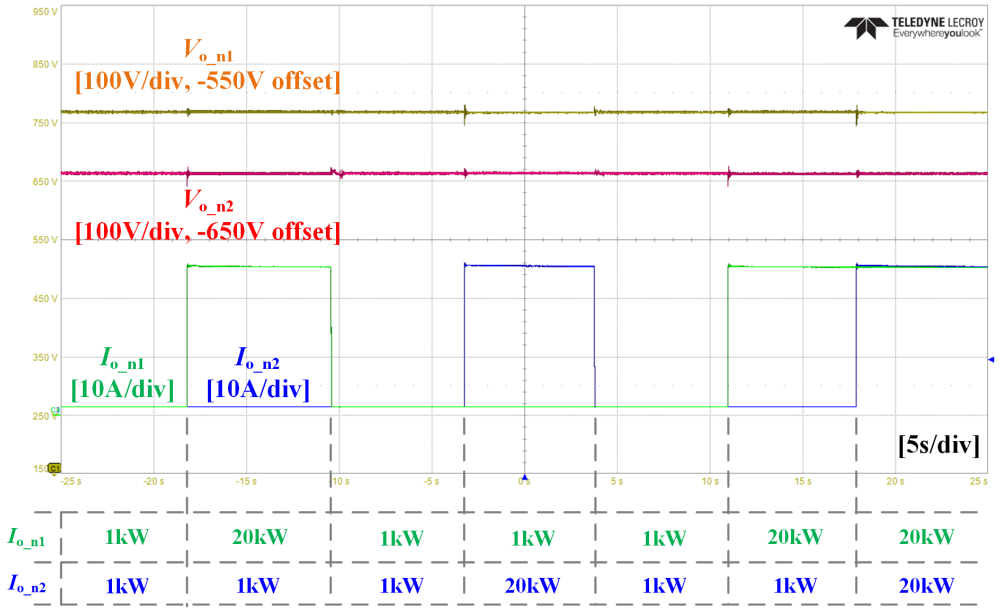


Figure 17. The decoupling waveform of the TAB converter when the loads of each port are changed at a random timing (n is the subunit index, n = 1∼10).

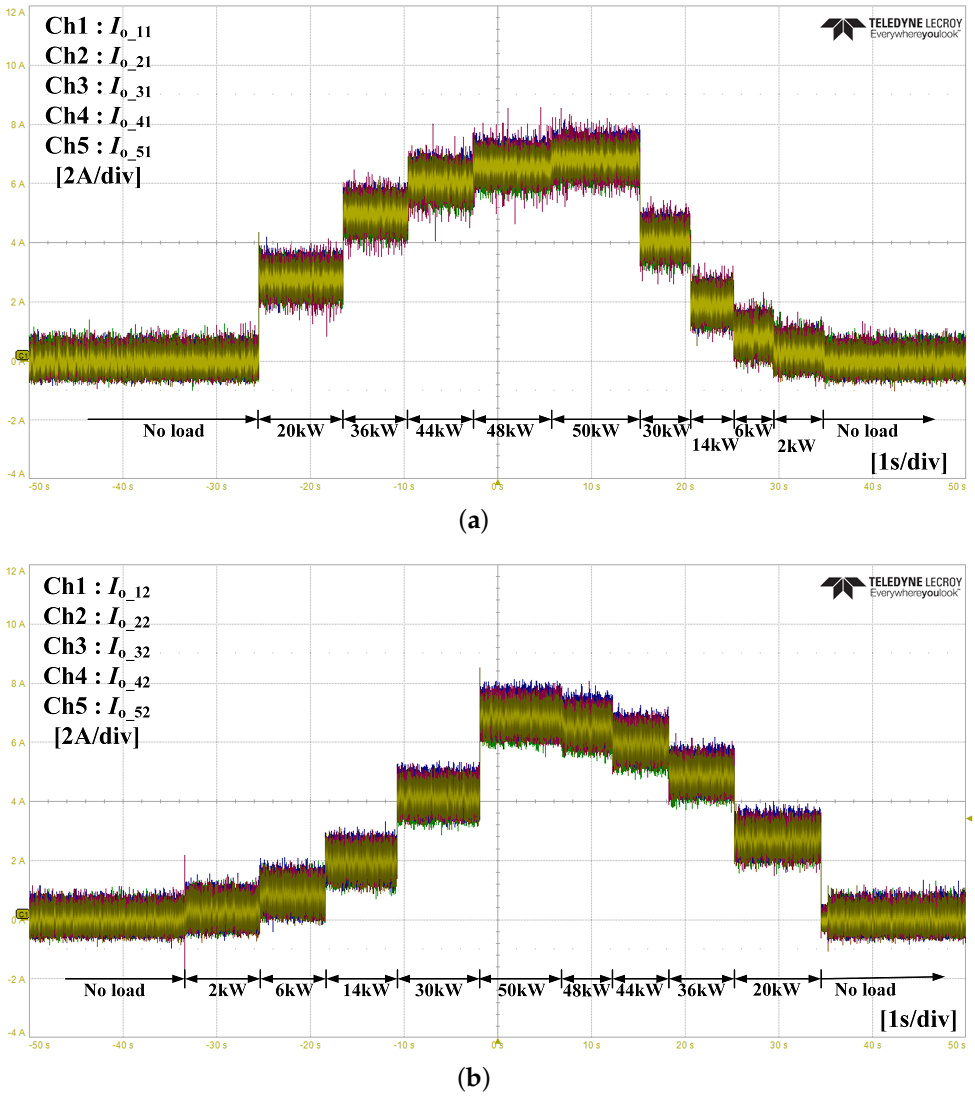


Figure 18. Current sharing waveforms: (**a**) output currents corresponding to Port 1; (**b**) output currents corresponding to Port 2.

8. Conclusions

This paper presents the implementation of a single-phase 150 kW prototype of an SST for application between a 13.2 kV MVAC network and a 750 V bipolar DC distribution. The prototype of the SST has ten cascaded subunits in consideration of the device rating and MI. Each subunit consists of an AC/DC stage and a DC/DC stage. In the AC/DC stage, a simple balancing controller is provided to prevent the voltage imbalance of DC-links due to the cascade structure. In the DC/DC stage, a simplified decoupling technique is provided to suppress the interaction between bipolar DC outputs. A paralleling scheme to ensure proper load sharing is provided for the parallel-connected DC/DC stage. In addition, the design of the HFIT to ensure high dielectric strength is discussed. All algorithms were validated through simulations and experiments.

Author Contributions: All the authors gave equal contributions in writing and revising the paper.

Acknowledgments: This research was supported by the KEPCO research institute.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Agelidis, V.G.; Demetriades, G.D.; Flourentzou, N. Recent Advances in High-Voltage Direct-Current Power Transmission Systems. In Proceedings of the 2006 IEEE International Conference on Industrial Technology, Mumbai, India, 15–17 December 2006; pp. 206–213.
2. Blaabjerg, F.; Ma, K. Future on Power Electronics for Wind Turbine Systems. *IEEE J. Emerg. Sel. Top. Power Electron.* **2013**, *1*, 139–152. [CrossRef]
3. Kouro, S.; Malinowski, M.; Gopakumar, K.; Pou, J.; Franquelo, L.G.; Wu, B.; Rodriguez, J.; Perez, M.A.; Leon, J.I. Recent Advances and Industrial Applications of Multilevel Converters. *IEEE Trans. Ind. Electron.* **2010**, *57*, 2553–2580. [CrossRef]
4. Flourentzou, N.; Agelidis, V.G.; Demetriades, G.D. VSC-Based HVDC Power Transmission Systems: An Overview. *IEEE Trans. Power Electron.* **2009**, *24*, 592–602. [CrossRef]
5. Hammons, T.J.; Woodford, D.; Loughtan, J.; Chamia, M.; Donahoe, J.; Povh, D.; Bisewski, B.; Long, W. Role of HVDC transmission in future energy development. *IEEE Power Eng. Rev.* **2000**, *20*, 10–25. [CrossRef]
6. Rodriguez-Diaz, E.; Savaghebi, M.; Vasquez, J.C.; Guerrero, J.M. An overview of low voltage DC distribution systems for residential applications. In Proceedings of the 2015 IEEE 5th International Conference on Consumer Electronics—Berlin (ICCE-Berlin), Berlin, Germany, 6–9 September 2015; pp. 318–322.
7. She, X.; Burgos, R.; Wang, G.; Wang, F.; Huang, A.Q. Review of solid state transformer in the distribution system: From components to field application. In Proceedings of the 2012 IEEE Energy Conversion Congress and Exposition (ECCE), Raleigh, NC, USA, 15–20 September 2012; pp. 4077–4084.
8. She, X.; Huang, A. Solid state transformer in the future smart electrical system. In Proceedings of the 2013 IEEE Power Energy Society General Meeting, Vancouver, BC, Canada, 21–25 July 2013; pp. 1–5.
9. Bignucolo, F.; Bertoluzzo, M.; Fontana, C. Applications of the solid state transformer concept in the electrical power system. In Proceedings of the 2015 AEIT International Annual Conference (AEIT), Naples, Italy, 14–16 October 2015; pp. 1–6.
10. Shah, D.G.; Crow, M.L. Stability Design Criteria for Distribution Systems With Solid-State Transformers. *IEEE Trans. Power Deliv.* **2014**, *29*, 2588–2595. [CrossRef]
11. Wang, G.; Baek, S.; Elliott, J.; Kadavelugu, A.; Wang, F.; She, X.; Dutta, S.; Liu, Y.; Zhao, T.; Yao, W.; et al. Design and hardware implementation of Gen-1 silicon based solid state transformer. In Proceedings of the 2011 Twenty-Sixth Annual IEEE Applied Power Electronics Conference and Exposition (APEC), Fort Worth, TX, USA, 6–11 March 2011; pp. 1344–1349.
12. Bifaretti, S.; Zanchetta, P.; Watson, A.; Tarisciotti, L.; Clare, J.C. Advanced Power Electronic Conversion and Control System for Universal and Flexible Power Management. *IEEE Trans. Smart Grid* **2011**, *2*, 231–243. [CrossRef]
13. Zhao, C.; Dujic, D.; Mester, A.; Steinke, J.K.; Weiss, M.; Lewdeni-Schmid, S.; Chaudhuri, T.; Stefanutti, P. Power Electronic Traction Transformer-Medium Voltage Prototype. *IEEE Trans. Ind. Electron.* **2014**, *61*, 3257–3268. [CrossRef]
14. Dujic, D.; Zhao, C.; Mester, A.; Steinke, J.K.; Weiss, M.; Lewdeni-Schmid, S.; Chaudhuri, T.; Stefanutti, P. Power Electronic Traction Transformer-Low Voltage Prototype. *IEEE Trans. Power Electron.* **2013**, *28*, 5522–5534. [CrossRef]
15. Zhao, C.; Weiss, M.; Mester, A.; Lewdeni-Schmid, S.; Dujic, D.; Steinke, J.K.; Chaudhuri, T. Power electronic transformer (PET) converter: Design of a 1.2 MW demonstrator for traction applications. In Proceedings of the International Symposium on Power Electronics Power Electronics, Electrical Drives, Automation and Motion, Sorrento, Italy, 20–22 June 2012; pp. 855–860.
16. Cecati, C.; Dell'Aquila, A.; Liserre, M.; Monopoli, V.G. A passivity-based multilevel active rectifier with adaptive compensation for traction applications. *IEEE Trans. Ind. Appl.* **2013**, *39*, 1404–1413. [CrossRef]
17. Liu, Y.; Huang, A.Q.; Song, W.; Bhattacharya, S.; Tan, G. Small-Signal Model-Based Control Strategy for Balancing Individual DC Capacitor Voltages in Cascade Multilevel Inverter-Based STATCOM. *IEEE Trans. Ind. Electron.* **2009**, *56*, 2259–2269. [CrossRef]
18. Dell'Aquila, A.; Liserre, M.; Monopoli, V.G.; Rotondo, P. An energy-based control for an n-H-bridges multilevel active rectifier. *IEEE Trans. Ind. Electron.* **2005**, *52*, 670–678. [CrossRef]

19. Zhao, T.; Wang, G.; Zeng, J.; Dutta, S.; Bhattacharya, S.; Huang, A.Q. Voltage and power balance control for a cascaded multilevel solid state transformer. In Proceedings of the 2010 Twenty-Fifth Annual IEEE Applied Power Electronics Conference and Exposition (APEC), Palm Springs, CA, USA, 21–25 February 2010; pp. 761–767.
20. Zhao, T.; Wang, G.; Bhattacharya, S.; Huang, A.Q. Voltage and Power Balance Control for a Cascaded H-Bridge Converter-Based Solid-State Transformer. *IEEE Trans. Power Electron.* **2013**, *28*, 1523–1532. [CrossRef]
21. Barrena, J.A.; Marroyo, L.; Vidal, M.Á.R.; Apraiz, J.R.T. Individual Voltage Balancing Strategy for PWM Cascaded H-Bridge Converter-Based STATCOM. *IEEE Trans. Ind. Electron.* **2008**, *55*, 21–29. [CrossRef]
22. She, X.; Huang, A.Q.; Zhao, T.; Wang, G. Coupling Effect Reduction of a Voltage-Balancing Controller in Single-Phase Cascaded Multilevel Converters. *IEEE Trans. Power Electron.* **2012**, *27*, 3530–3543. [CrossRef]
23. Wang, H.; Cheng, Q.; Li, M.; Chen, G.; Deng, L. The study of single-phase PWM rectifier based on PR control strategy. In Proceedings of the 26th Chinese Control and Decision Conference (2014 CCDC), Changsha, China, 31 May–2 June 2014; pp. 3818–3823.
24. Park, Y.M.; Yoo, J.Y.; Lee, S.B. Practical Implementation of PWM Synchronization and Phase-Shift Method for Cascaded H-Bridge Multilevel Inverters Based on a Standard Serial Communication Protocol. *IEEE Trans. Ind. Appl.* **2008**, *44*, 634–643. [CrossRef]
25. Kheraluwala, M.N.; Gascoigne, R.W.; Divan, D.M.; Baumann, E.D. Performance characterization of a high-power dual active bridge DC-to-DC converter. *IEEE Trans. Ind. Appl.* **1992**, *28*, 1294–1301. [CrossRef]
26. Zhao, B.; Song, Q.; Liu, W.; Sun, Y. Overview of Dual-Active-Bridge Isolated Bidirectional DC-DC Converter for High-Frequency-Link Power-Conversion System. *IEEE Trans. Power Electron.* **2014**, *29*, 4091–4106. [CrossRef]
27. Bhattacharya, S.; Zhao, T.; Wang, G.; Dutta, S.; Baek, S.; Du, Y.; Parkhideh, B.; Zhou, X.; Huang, A.Q. Design and development of Generation-I silicon based Solid State Transformer. In Proceedings of the 2010 Twenty-Fifth Annual IEEE Applied Power Electronics Conference and Exposition (APEC), Palm Springs, CA, USA, 21–25 February 2010; pp. 1666–1673.
28. Engel, S.P.; Stieneker, M.; Soltau, N.; Rabiee, S.; Stagge, H.; de Doncker, R.W. Comparison of the Modular Multilevel DC Converter and the Dual-Active Bridge Converter for Power Conversion in HVDC and MVDC Grids. *IEEE Trans. Power Electron.* **2015**, *30*, 124–137. [CrossRef]
29. Da Silva, M.M.; Pinheiro, H. Voltage balancing in flying capacitor converter multilevel using space vector modulation. In Proceedings of the 2017 IEEE 8th International Symposium on Power Electronics for Distributed Generation Systems (PEDG), Florianopolis, Brazil, 17–20 April 2017; pp. 1–5.
30. Zhao, C.; Round, S.D.; Kolar, J.W. An Isolated Three-Port Bidirectional DC-DC Converter With Decoupled Power Flow Management. *IEEE Trans. Power Electron.* **2008**, *23*, 2443–2453. [CrossRef]
31. Baek, S.; Roy, S.; Bhattacharya, S.; Kim, S. Power flow analysis for 3-port 3-phase dual active bridge dc/dc converter and design validation using high frequency planar transformer. In Proceedings of the 2013 IEEE Energy Conversion Congress and Exposition, Denver, CO, USA, 15–19 September 2013; pp. 388–395.
32. De Doncker, R.W.A.A.; Divan, D.M.; Kheraluwala, M.H. A three-phase soft-switched high-power-density DC/DC converter for high-power applications. *IEEE Trans. Ind. Appl.* **1991**, *27*, 63–73. [CrossRef]
33. Zhang, Z.; Andersen, M.A.E. High frequency AC inductor analysis and design for dual active bridge (DAB) converters. In Proceedings of the 2016 IEEE Applied Power Electronics Conference and Exposition (APEC), Long Beach, CA, USA, 20–24 March 2016; pp. 1090–1095.
34. Shah, M.; Ngo, K.D.T. Parameter extraction for the extended cantilever model of magnetic component windings. *IEEE Trans. Aerosp. Electron. Syst.* **2000**, *36*, 260–266. [CrossRef]
35. Moonem, M.; Pechacek, C.; Hemandez, R.; Krishnaswami, H. Analysis of a Multilevel Dual Active Bridge (ML-DAB) DC-DC Converter Using Symmetric Modulation. *Electronics* **2015**, *4*, 239–260. [CrossRef]
36. Moonem, M.A.; Krishnaswami, H. Analysis and control of multi-level dual active bridge DC-DC converter. In Proceedings of the 2012 IEEE Energy Conversion Congress and Exposition (ECCE), Raleigh, NC, USA, 15–20 September 2012; pp. 1556–1561.
37. Wu, Z.; Xue, Y.; Pan, L.; Li, D.; He, T.; Sun, L.; Yang, Y. Active disturbance rejection control based simplified decoupling for two-input-two-output processes. In Proceedings of the 2017 36th Chinese Control Conference (CCC), Dalian, China, 26–28 July 2017; pp. 399–404.

38. Vasanthakumar, D.; Srikanth, V. DC-DC converter control using IP controller. In Proceedings of the 2014 International Conference on Computation of Power, Energy, Information and Communication (ICCPEIC), Chennai, India, 16–17 April 2014; pp. 245–249.
39. Segaran, D.; Holmes, D.G.; McGrath, B.P. Enhanced Load Step Response for a Bidirectional DC-DC Converter. *IEEE Trans. Power Electron.* **2013**, *28*, 371–379. [CrossRef]
40. Huang, Y.; Tse, C.K. Circuit Theoretic Classification of Parallel Connected DC-DC Converters. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2007**, *54*, 1099–1108. [CrossRef]
41. Luo, S.; Ye, Z.; Lin, Ra.; Lee, F.C. A classification and evaluation of paralleling methods for power supply modules. In Proceedings of the 30th Annual IEEE Power Electronics Specialists Conference, Charleston, SC, USA, 1 July 1999; pp. 901–908.
42. Du, S.B.Y.; Wang, G.; Bhattacharya, S. Design considerations of high voltage and high frequency transformer for solid state transformer application. In Proceedings of the IECON 2010–36th Annual Conference on IEEE Industrial Electronics Society, Glendale, AZ, USA, 7–10 November 2010; pp. 421–426.
43. *IEEE Standard for General Requirements for Dry-Type Distribution and Power Transformers*; IEEE Std C57.12.01-2015 (Revision of IEEE Std C57.12.01-2005); IEEE: Piscataway, NJ, USA, 2015; pp. 1–52.
44. Schwodiauer, R.; Neugschwandtner, G.; Bauer-Gogonea, S.; Bauer, S.; Heitz, J.; Bauerle, D. Dielectric and electret properties of novel Teflon PTFE and PTFE-like polymers. In Proceedings of the10th International Symposium on Electrets (ISE 10), Athens, Greece, 22–24 September 1999; pp. 313–316.
45. Dowcorning. Sylgard 170 Silicone Elastomer. In *Sylgard Datasheet*; Dowcorning: Midland, MI, USA, 2015.