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Three Topologies of a Non-Isolated High Gain Switched-Inductor Switched-Capacitor Step-Up Cuk Converter for Renewable Energy Applications

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Abstract: This paper introduces three topologies of a non-isolated high gain step-up Cuk converter based on a switched-inductor (SL) and switched-capacitor (SC) techniques for renewable energy applications, such as photovoltaic and fuel cells. These kinds of Cuk converters provide a negative-to-positive step-up dc–dc voltage conversion. The proposed three topologies SLSC Cuk converters increase the voltage boost ability significantly using the switched-inductor and switched-capacitor techniques compared with the classical Cuk and boost converters. The proposed Cuk converters are derived from the classical Cuk converter by replacing the single inductor at the input and output sides with a SL and the transferring energy capacitor by a SC. The main advantages of the proposed SLSC Cuk converters are achieving a high voltage conversion ratio and reducing the voltage stress across the main switch. Therefore, a switch with low voltage rating and thus, of low R_{DS-ON} can be used, and that leads to a higher efficiency. For example, the third topology have the ability to boost the input voltage up to 13 times when D = 0.75, D is the duty cycle. The voltage gain and the voltage stress across the main switch in the three topologies have been compared with the classical Cuk and boost converter. The proposed three topologies avoid using a transformer, coupled inductors, or extreme duty cycles leading to less volume, loss, and cost. The proposed SLSC Cuk converters are analyzed in continuous conduction mode (CCM), and they have been designed for 12 V input supply voltage, 100 W rated power, 50 kHz switching frequency, and 75% duty cycle. A detailed theoretical analysis of the CCM is represented and all the equations have been derived and matched with the results. The proposed three topologies SLSC Cuk converters have been simulated in MATLAB/SIMULINK and results are discussed.

Keywords: cuk converter; dc–dc converter; photovoltaic; Switch-capacitor (SC); Switch-inductor (SL)

1. Introduction

Various dc–dc converter topologies include isolated converters and non-isolated converters have been developed to achieve a high voltage gain without an extremely high duty cycle. Usually, isolated dc–dc converters using transformers are used when a high step-up ratio is required because the voltage gain can be adjusted by increasing the turns ratio of the transformer [1–6]. However, the isolated converters have some difficulties in achieving a high efficiency due to the power transformer losses and the leakage inductance besides the heavy weight and large volume of the converter. So, the best solution is to use a non-isolated converters with an additional technique associated to achieve a high voltage gain [7–9].

A high output voltage classical boost converter requires a MOSFET with high current and voltage ratings. Therefore, this MOSFET has a high on-resistance, which increases cost, size, and conduction

loss [10]. A number of high step-up topologies have been presented in order to increase the voltage gain and efficiency. In [11], a cascade boost converter is presented. It can supply a load with a high voltage and relatively high efficiency. The major drawbacks of using this topology are higher cost because of using two dc–dc converters and the complexity.

Converters with coupled inductors topology can accomplish high voltage gain [12–17]. However, using coupled inductors topology will reduce the efficiency due to the losses associated with the leakage inductors. Other drawbacks are requiring high voltage rated switch and suffering from EMI problems [10].

In some special industrial applications such as automobiles, space stations, and manufacturing industries, dc–dc converters that can achieve the negative to positive voltage conversion play an important role [18]. In such applications, the negative dc voltage source requires a dc–dc converter that realizes the polarity inversion to provide the positive voltage to the load with respect to the common ground. In designing the dc–dc converter for the negative dc voltage bus, two features should be considered: a negative to positive voltage conversion path and high voltage conversion ratios [19].

The classical Cuk (shown in Figure 1) and buck boost converters are two dc–dc converters that have an output voltage magnitude that is either greater or less than the input voltage with a polarity inversion due to their voltage conversion ratio as described in (1). The value of D which is the duty cycle cannot be too high (more than 0.9) and consequently, their boost voltage abilities have been restricted due to the effect of parasitic components [19]. The classical Cuk converter has three modes (buck mode, boost mode, and buck-boost mode) [20]. The classical Cuk converter has advantages such as having an energy transfer capacitor, good steady-state performance, continuous input and output current, and low output voltage ripple [20–22]. Ref. [23–26] present Cuk converters using different techniques, however, the voltage conversion ratio is low. A number of switched-inductor and switched-capacitor topologies are presented in [27] to achieve high voltage gain.

$$M_{Cuk} = M_{buck-boost} = \frac{V_{out}}{V_{in}} = -\frac{D}{(1-D)} \quad (1)$$

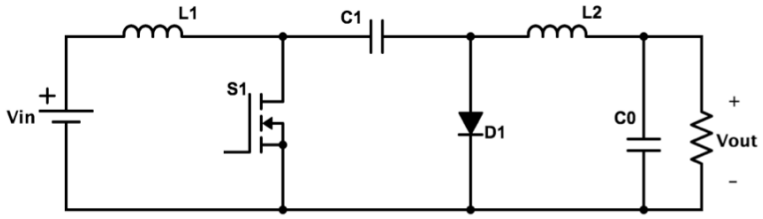


Figure 1. Classical Cuk converter.

In this paper, the concept of a switched-inductor (SL) and switched-capacitor (SC) techniques have been integrated to the classical Cuk converter, and consequently, new step-up Cuk converters are proposed. From the viewpoint of a circuit topology (combining SL with SC in Cuk converter), the proposed converters are different from any other existing Cuk converter. The main advantages of the proposed converters are summarized as follow.

- provide a non-isolated negative to positive voltage path with respect to a common ground;
- higher voltage conversion ratios than the classical Cuk and boost converter due to the SL and SC techniques;
- lower voltage stress across the main switch than the classical Cuk and boost converter, therefore, a switch with low voltage rating and low R_{DS-ON} can be used;
- according to the topology, number of diodes, one capacitor, and one or three inductors have been added to the main Cuk converter to perform the SL and SC in order to increase the voltage gain;
- use of a single switch;

- the main advantage of the classical Cuk converter which is having continuous current in the input and output sides due to the input and output inductors have been kept when designing the proposed topologies.

Topology-I, -II, and -III are described in Sections 2–4. Each topology section contains a power circuit, modes of operation, and a detailed circuit analysis. In Section 5, a comparison analysis is performed between the proposed Cuk topologies, a classical Cuk converter, and classical boost converter in terms of a voltage gain and switch voltage stress. Results are discussed in Section 6. Finally, a brief summary is given in the conclusion in Section 7.

2. Topology-I

2.1. Power Circuit

The SLSC Cuk converter topology-I is obtained from the classical Cuk converter by replacing the input side inductor with a SL and the transferring energy capacitor with a SC. Figure 2 shows the power circuit diagram of the SLSC topology-I. Compared with the Cuk prototype, one inductor, one capacitor, and four diodes are added into the proposed circuit of Figure 2.

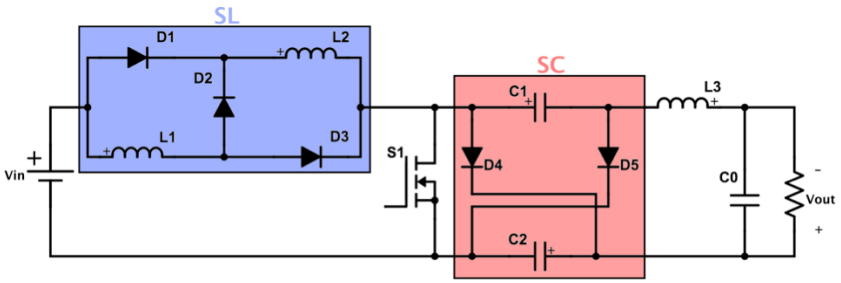


Figure 2. Proposed topology-I SLSC Cuk converter.

2.2. Modes of Operation

The proposed three topologies SLSC Cuk converters are analyzed in continuous conduction mode (CCM). In CCM, the operation of the proposed three topologies is divided into two modes. ON-mode when switch S_1 is conducting and OFF-mode when switch S_1 is not conducting.

2.2.1. ON-Mode

When switch S_1 is conducting (turned on), the current direction is shown in Figure 3a. Inductors L_1 and L_2 are charged in parallel by input supply voltage V_{in} through diodes D_1, D_3, and switch S_1. Diodes D_2, D_4, and D_5 are reversed-biased. Input supply voltage V_{in} with the discharged energy of capacitors C_1 and C_2 supply the load and charge inductor L_3 through switch S_1. Equal amount of current flowing through inductors L_1 and L_2 since both inductors are the same.

2.2.2. OFF-Mode

When switch S_1 is not conducting (turned off), the current direction is shown in Figure 3b. Input supply voltage V_{in} with the discharged energy of inductors L_1 and L_2 charge capacitors C_1 and C_2 connected in parallel. Likewise, the discharged energy of inductor L_3 charges capacitors C_1 and C_2 and supply the load. Diodes D_1 and D_3 are reversed-biased. Switching diagrams in CCM of the main steady-state waveforms with enlarged variations for the SLSC topology-I are shown in Figure 4.

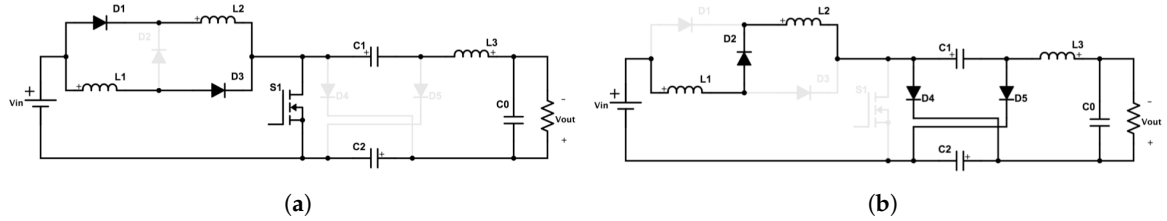


Figure 3. Operation modes. (**a**) ON-mode. (**b**) OFF-mode.

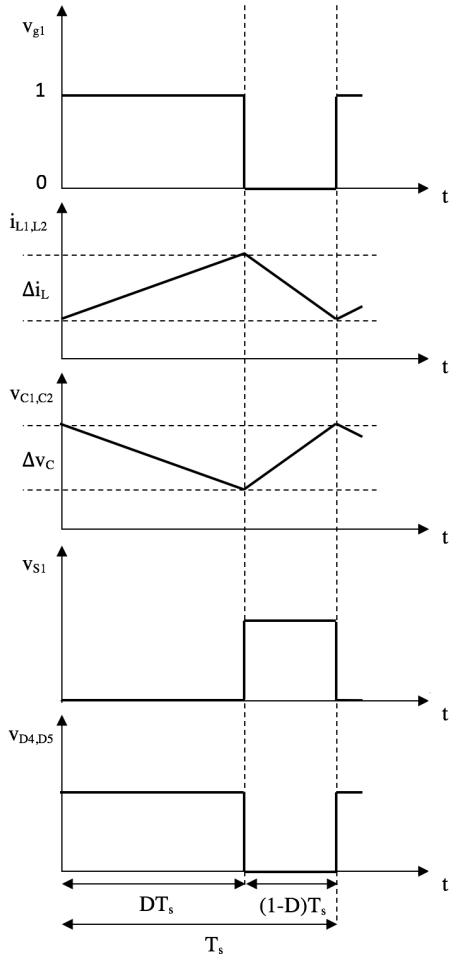


Figure 4. Main steady-state waveforms of SLSC topology-I.

2.3. Circuit Analysis

It is assumed that all three topologies SLSC Cuk converters are operating in steady-state to simplify the analysis. Also, the following assumptions are made: all components are ideal (100% efficiency), input voltage V_{in} is a pure dc, and all capacitors are sized to have a relatively small voltage ripple at switching frequency f_s.

When MOSFET S_1 is conducting, the voltage across inductors L_1, L_2, and L_3 are expressed in (2) and (3). ($C_1 = C_2 = C$)

$$V_{L_1} = V_{L_2} = V_{in} \tag{2}$$

$$V_{L_3} = 2V_C - V_{out} \tag{3}$$

When MOSFET S_1 is not conducting, the voltage across inductors L_1, L_2, and L_3 are expressed in (4) and (5).

$$V_{L_1} = V_{L_2} = \frac{V_{in} - V_C}{2} \tag{4}$$

$$V_{L_3} = V_C - V_{out} \tag{5}$$

By applying the volt-second method to the inductors L_1, L_2, and L_3 the two expressions in (6) and (7) can be obtained.

$$V_{in}D + (\frac{V_{in} - V_C}{2})(1 - D) = 0 \tag{6}$$

$$(2V_C - V_{out})D + (V_C - V_{out})(1 - D) = 0 \tag{7}$$

The voltage expression across C_1 and C_2 can be expressed in (8).

$$V_C = \frac{(1 + D)}{(1 - D)} V_{in} \tag{8}$$

The ideal voltage gain in CCM can be expressed in (9)

$$M_{CCM_I} = \frac{V_{out}}{V_{in}} = \frac{I_{in}}{I_{out}} = \frac{(1 + D)^2}{(1 - D)} \tag{9}$$

From Figure 3a,b, it is possible to find an equation to calculate the current of the two input inductors. Because the two input inductors have the same inductance values, $I_{L_1} = I_{L_2} = I_{L_{in}}$ is obtained in (11) from (10).

$$I_{in} = 2I_{L_{in}}D + I_{L_{in}}(1 - D) \tag{10}$$

$$I_{L_{in}} = \frac{I_{in}}{(1 + D)} = \frac{P_{out}}{(1 + D)V_{in}} \tag{11}$$

Capacitor C_O acts as low-pass filter, so (12) is obtained for $I_{L_3} = I_{L_{out}}$.

$$I_{L_{out}} = I_{out} = \frac{P_{out}}{V_{out}} \tag{12}$$

The reverse voltage across D_1 and D_3 applied when they are blocked (OFF-mode) is expressed in (13).

$$V_{D_1} = V_{D_3} = \frac{D}{(1 - D)} V_{in} \tag{13}$$

The reverse voltage across D_2 applied when it is blocked (ON-mode) is expressed in (14).

$$V_{D_2} = V_{in} \tag{14}$$

The reverse voltage across D_4 and D_5 of the SC applied when they are blocked (ON-mode) is expressed in (15).

$$V_{D_4} = V_{D_5} = \frac{(1 + D)}{(1 - D)} V_{in} \tag{15}$$

The voltage stress across the power switch S_1 when it is blocked (OFF-mode) is expressed in (16).

$$V_{S_1} = \frac{(1 + D)}{(1 - D)} V_{in} \tag{16}$$

The peak-to-peak variation of the inductor's current at the input ($\triangle i_{L_1} = \triangle i_{L_2} = \triangle i_{L_{in}}$) and output ($\triangle i_{L_3} = \triangle i_{L_{out}}$) sides are expressed in (17) and (18), respectively.

$$\triangle i_{L_{in}} = \frac{DTV_{in}}{L_{in}} = \frac{DV_{in}}{fL_{in}} \tag{17}$$

$$\triangle i_{L_{out}} = \frac{DT(2V_C - V_{out})}{L_{out}} = \frac{D(2V_C - V_{out})}{fL_{out}} \tag{18}$$

The peak-to-peak variation of the capacitor's voltage ($\triangle v_{C_1} = \triangle v_{C_2} = \triangle v_C$) is expressed in (19).

$$\triangle v_C = \frac{DTI_{out}}{C} = \frac{DP_{out}}{M_{CCM_I} V_{in} fC} \tag{19}$$

3. Topology-II

3.1. Power Circuit

The SLSC Cuk converter topology-II is obtained from the classical Cuk converter by replacing the output side inductor with a SL and the transferring energy capacitor with a SC. Figure 5 shows the power circuit diagram of the SLSC Cuk converter topology-II. Compared with the Cuk prototype, one inductor, one capacitor, and four diodes are added into the proposed circuit of Figure 5.

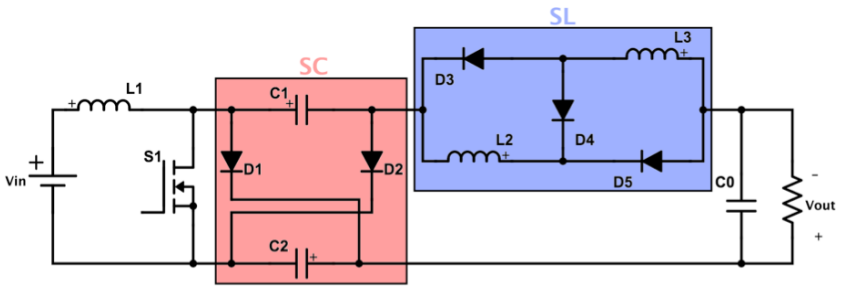


Figure 5. Proposed topology-II SLSC Cuk converter.

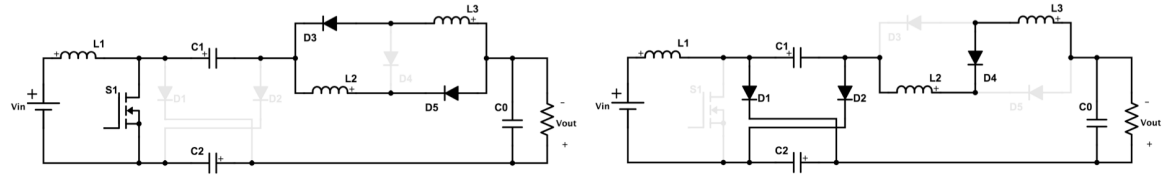
3.2. Modes of Operation

3.2.1. ON-Mode

When switch S_1 is conducting, the current direction is shown in Figure 6a. Inductor L_1 is charged by input supply voltage V_{in} through switch S_1. Input supply voltage V_{in} with the discharged energy of capacitors C_1 and C_2 supply the load and charge inductors L_2 and L_3 which is connected in parallel through diodes D_3, D_5, and switch S_1. Diodes D_1, D_2, and D_4 are reversed-biased. Equal amount of current flowing through inductors L_2 and L_3 since both inductors are the same.

3.2.2. OFF-Mode

When switch S_1 is not conducting, the current direction is shown in Figure 6b. The input supply voltage V_{in} and the discharged energy of inductor L_1 charge capacitors C_1 and C_2 connected in parallel. Likewise, the discharged energy of inductors L_2 and L_3 charges capacitors C_1 and C_2 and supplies the load. Diodes D_3 and D_5 are reversed-biased. Switching diagrams in CCM of the main steady-state waveforms with enlarged variations for the SLSC topology-II are shown in Figure 7.



(**a**) (**b**)

Figure 6. Operation modes. (**a**) On-mode. (**b**) Off-mode.

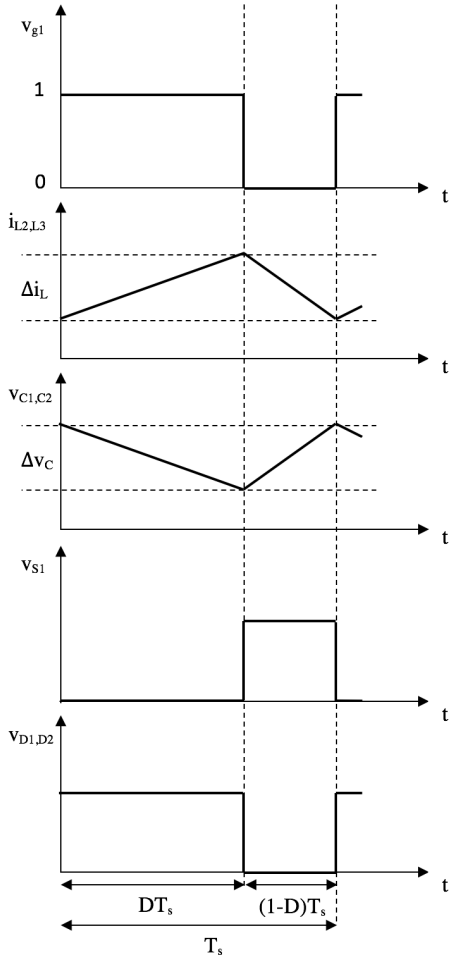


Figure 7. Main steady-state waveforms of SLSC topology-II.

3.3. Circuit Analysis

When MOSFET S_1 is conducting, the voltage across inductors L_1, L_2, and L_3 are expressed in (20) and (21). ($C_1 = C_2 = C$)

$$V_{L_1} = V_{in} \tag{20}$$

$$V_{L_2} = V_{L_3} = 2V_C - V_{out} \tag{21}$$

When MOSFET S_1 is not conducting, the voltage across inductors L_1, L_2, and L_3 are expressed in (22) and (23).

$$V_{L_1} = V_{in} - V_C \tag{22}$$

$$V_{L_2} = V_{L_3} = \frac{V_C - V_{out}}{2} \tag{23}$$

By applying the volt-second method to the inductors L_1, L_2, and L_3 the two expressions in (24) and (25) can be obtained.

$$V_{in}D + (V_{in} - V_C)(1 - D) = 0 \tag{24}$$

$$(2V_C - V_{out})D + (\frac{V_C - V_{out}}{2})(1 - D) = 0 \tag{25}$$

The voltage expression across C_1 and C_2 can be obtained in (26).

$$V_C = \frac{1}{(1 - D)}V_{in} \tag{26}$$

The ideal voltage gain in CCM can be expressed in (27)

$$M_{CCM_{II}} = \frac{V_{out}}{V_{in}} = \frac{I_{in}}{I_{out}} = \frac{(1 + 3D)}{(1 + D)(1 - D)} \tag{27}$$

The input inductor current ($I_{L_1} = I_{L_{in}}$) is obtained in (28) from (27).

$$I_{L_{in}} = I_{in} = \frac{(1 + 3D)}{(1 + D)(1 - D)}I_{out} = \frac{(1 + 3D)P_{out}}{(1 + D)(1 - D)V_{out}} \tag{28}$$

From Figure 6, it is possible to find an equation to calculate the current of the two output inductors. Because the two output inductors have the same inductance values, $I_{L_2} = I_{L_3} = I_{L_{out}}$ is obtained in (30) from (29).

$$I_{out} = 2I_{L_{out}}D + I_{L_{out}}(1 - D) \tag{29}$$

$$I_{L_{out}} = \frac{I_{out}}{(1 + D)} = \frac{P_{out}}{(1 + D)V_{out}} \tag{30}$$

The reverse voltage across D_1 and D_2 of the SC applied when they are blocked (ON-mode) is expressed in (31).

$$V_{D_1} = V_{D_2} = \frac{V_{in}}{(1 - D)} \tag{31}$$

The voltage stress across the power switch S_1 when it is blocked (OFF-mode) is expressed in (32).

$$V_{S_1} = \frac{V_{in}}{(1 - D)} \tag{32}$$

The reverse voltage across D_3 and D_5 applied when they are blocked (OFF-mode) is expressed in (33).

$$V_{D_3} = V_{D_5} = \frac{D}{(1 + D)(1 - D)}V_{in} \tag{33}$$

The reverse voltage across D_4 applied when it is blocked (ON-mode) is expressed in (34).

$$V_{D_4} = \frac{V_{in}}{(1 + D)} \tag{34}$$

The peak-to-peak variation of the inductor's current at the input ($\triangle i_{L_1} = \triangle i_{L_{in}}$) and output ($\triangle i_{L_2} = \triangle i_{L_3} = \triangle i_{L_{out}}$) sides are expressed in (35) and (36), respectively.

$$\triangle i_{L_{in}} = \frac{DTV_{in}}{L_{in}} = \frac{DV_{in}}{fL_{in}} \tag{35}$$

$$\triangle i_{L_{out}} = \frac{DT(2V_C - V_{out})}{L_{out}} = \frac{D(2V_C - V_{out})}{fL_{out}} \tag{36}$$

The peak-to-peak variation of the capacitor's voltage ($\triangle v_{C_1} = \triangle v_{C_2} = \triangle v_C$) is expressed in (37).

$$\triangle v_C = \frac{DTI_{out}}{C} = \frac{DP_{out}}{M_{CCM_{II}} V_{in} f C} \tag{37}$$

4. Topology-III

4.1. Power Circuit

The SLSC Cuk converter topology-III is obtained from the classical Cuk converter by replacing both the input and output side inductors with two SLs and the transferring energy capacitor with a SC. Figure 8 shows the power circuit diagram of the SLSC Cuk converter topology-III. Compared with the Cuk prototype, two inductors, one capacitor, and seven diodes are added into the proposed circuit of Figure 8.

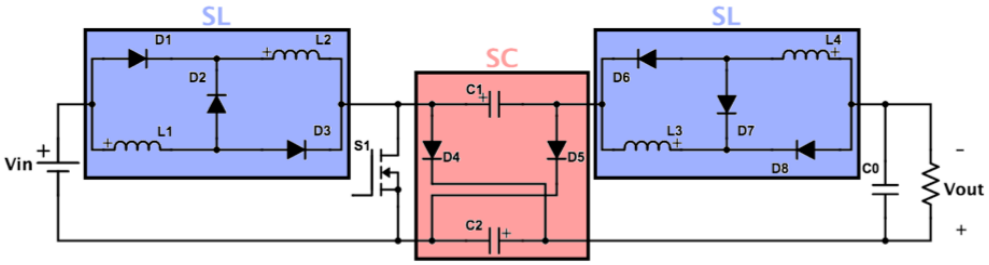


Figure 8. Proposed topology-III SLSC Cuk converter.

4.2. Modes of Operation

4.2.1. ON-Mode

When switch S_1 is conducting, the current direction is shown in Figure 9a. Inductors L_1 and L_2 are charged in parallel by the input supply voltage V_{in} through diodes D_1, D_3, and switch S_1. On the other hand, the input supply voltage V_{in} with the discharged energy of capacitors C_1 and C_2 supply the load and charge inductors L_3 and L_4 connected in parallel through diodes D_6, D_8, and switch S_1. Diodes D_2, D_4, D_5, and D_7 are reversed-biased. An equal amount of current flowing through inductors L_1 and L_2 since both inductors are the same. Likewise, an equal amount of current flowing through inductors L_3 and L_4 since both inductors are the same.

4.2.2. OFF-Mode

When switch S_1 is not conducting, the current direction is shown in Figure 9b. The input supply voltage V_{in} with the discharged energy of inductors L_1 and L_2 charge capacitors C_1 and C_2 connected in parallel. Likewise, the discharged energy of inductors L_3 and L_4 charges capacitors C_1 and C_2 and supplies the load. Diodes D_1, D_3, D_6, and D_8 are reversed-biased. Switching diagrams in CCM of the main steady-state waveforms with enlarged variations for the SLSC topology-III are shown in Figure 10.

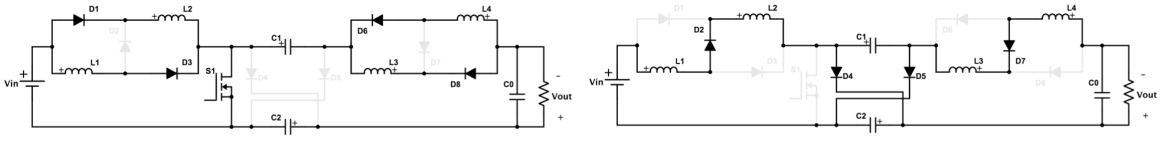


Figure 9. Operation modes. (**a**) On-mode. (**b**) Off-mode.

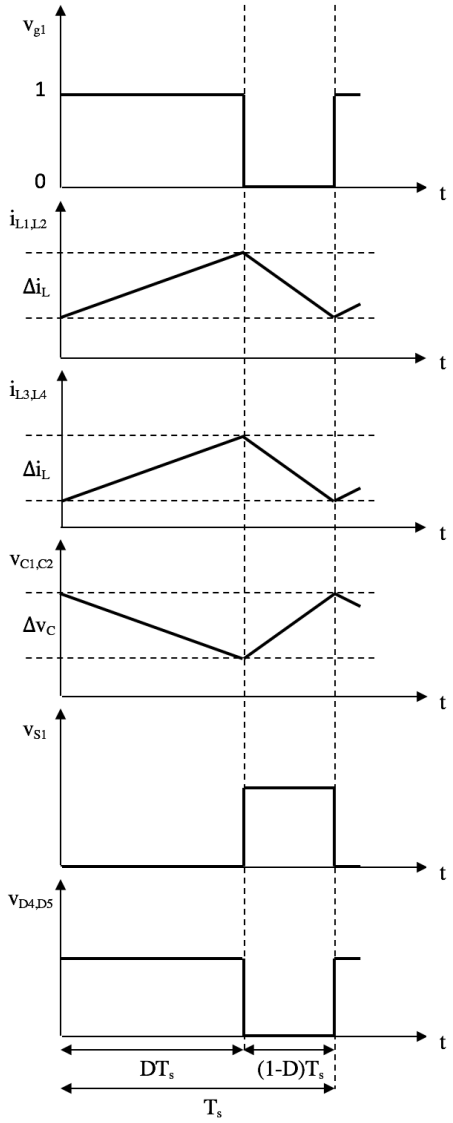


Figure 10. Main steady-state waveforms of SLSC topology-III.

4.3. Circuit Analysis

When MOSFET S_1 is conducting, the voltage across inductors L_1, L_2, L_3, and L_4 are expressed in (38) and (39). ($C_1 = C_2 = C$)

$$V_{L_1} = V_{L_2} = V_{in} \tag{38}$$

$$V_{L_3} = V_{L_4} = 2V_C - V_{out} \tag{39}$$

When MOSFET S_1 is not conducting, the voltage across inductors L_1, L_2, L_3, and L_4 are expressed in (40) and (41).

$$V_{L_1} = V_{L_2} = \frac{V_{in} - V_C}{2} \tag{40}$$

$$V_{L_3} = V_{L_4} = \frac{V_C - V_{out}}{2} \tag{41}$$

By applying the volt-second method to the inductors L_1, L_2, L_3, and L_4 the two expressions in (42) and (43) can be obtained.

$$V_{in}D + (\frac{V_{in} - V_C}{2})(1 - D) = 0 \tag{42}$$

$$(2V_C - V_{out})D + (\frac{V_C - V_{out}}{2})(1 - D) = 0 \tag{43}$$

The voltage expression across C_1 and C_2 can be obtained in (44).

$$V_C = \frac{(1 + D)}{(1 - D)} V_{in} \tag{44}$$

The ideal voltage gain in CCM can be expressed in (45).

$$M_{CCM_{III}} = \frac{V_{out}}{V_{in}} = \frac{I_{in}}{I_{out}} = \frac{I_{in}}{I_{out}} = \frac{(1 + 3D)}{(1 - D)} \tag{45}$$

From Figure 9a,b and as done in (10) and (29), $I_{L_1} = I_{L_2} = I_{L_{in}}$ and $I_{L_3} = I_{L_4} = I_{L_{out}}$ are expressed in (46) and (47), respectively.

$$I_{L_{in}} = \frac{I_{in}}{(1 + D)} = \frac{P_{out}}{(1 + D)V_{in}} \tag{46}$$

$$I_{L_{out}} = \frac{I_{out}}{(1 + D)} = \frac{P_{out}}{(1 + D)V_{out}} \tag{47}$$

The reverse voltage across D_1, D_3, D_6, and D_8 applied when they are blocked (OFF-mode) is expressed in (48).

$$V_{D_1} = V_{D_3} = V_{D_6} = V_{D_8} = \frac{D}{(1 - D)} V_{in} \tag{48}$$

The reverse voltage across D_2 and D_7 applied when they are blocked (ON-mode) is expressed in (49).

$$V_{D_2} = V_{D_7} = V_{in} \tag{49}$$

The reverse voltage across D_4 and D_5 of the SC applied when they are blocked (ON-mode) is expressed in (50).

$$V_{D_4} = V_{D_5} = \frac{(1 + D)}{(1 - D)} V_{in} \tag{50}$$

The voltage stress across the power switch S_1 when it is blocked (OFF-mode) is expressed in (51).

$$V_{S_1} = \frac{(1 + D)}{(1 - D)} V_{in} \tag{51}$$

The peak-to-peak variation of the inductor's current at the input ($\triangle i_{L_1} = \triangle i_{L_2} = \triangle i_{L_{in}}$) and output ($\triangle i_{L_3} = \triangle i_{L_4} = \triangle i_{L_{out}}$) sides are expressed in (52) and (53), respectively.

$$\triangle i_{L_{in}} = \frac{DTV_{in}}{L_{in}} = \frac{DV_{in}}{fL_{in}} \tag{52}$$

$$\triangle i_{L_{out}} = \frac{DT(2V_C - V_{out})}{L_{out}} = \frac{D(2V_C - V_{out})}{fL_{out}} \tag{53}$$

The peak-to-peak variation of the capacitor's voltage ($\triangle v_{C_1} = \triangle v_{C_2} = \triangle v_C$) is expressed in (54).

$$\triangle v_C = \frac{DTI_{out}}{C} = \frac{DP_{out}}{M_{CCM_{III}} V_{in} fC} \tag{54}$$

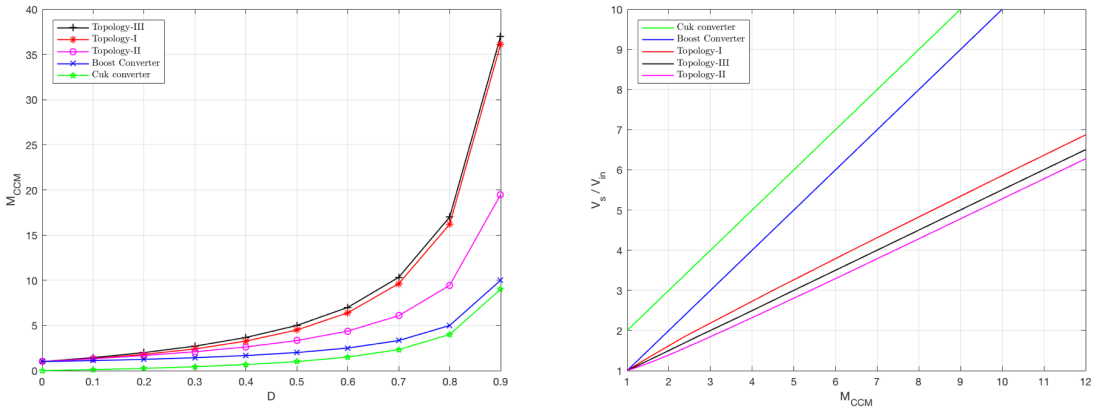
5. Comparison Analysis

A comparison has been made between the proposed three topologies SLSC Cuk converters with the classical Cuk and boost converters as shown in Table 1. The proposed three topologies have a higher voltage gain, and the highest is topology-III as shown graphically in Figure 11a.

The normalized voltage (V_s/V_{in}) on the main switch that describes the voltage stress across semiconductor device MOSFET S_1 of these three topologies are compared with those in the classical Cuk and boost converters and graphically represented in Figure 11b. As can be seen the three topologies have a lower voltage stress, and the lowest is topology-II.

Table 1. Comparison between boost converter, Cuk converter, and three proposed converters.

Topology	Boost	Cuk	Topology-I	Topology-II	Topology-III
Active switches	1	1	1	1	1
Diodes	1	1	5	5	8
Inductors	1	2	3	3	4
Capacitors	1	2	3	3	3
Voltage Gain	$\frac{1}{1-D}$	$\frac{D}{1-D}$	$\frac{(1+D)^2}{(1-D)}$	$\frac{(1+3D)}{(1+D)(1-D)}$	$\frac{(1+3D)}{(1-D)}$



(**a**) (**b**)

Figure 11. Voltage gain and voltage stress comparison. (**a**) Voltage gain comparison. (**b**) Voltage stress on the active switch.

6. Results and Discussion

The three proposed topologies are designed for 12 V input voltage, 100 W rated power, 50 kHz switching frequency, and 75% duty cycle. They all have been simulated in MATLAB/SIMULINK. Specifications of the proposed SLSC Cuk converters are shown in Table 2.

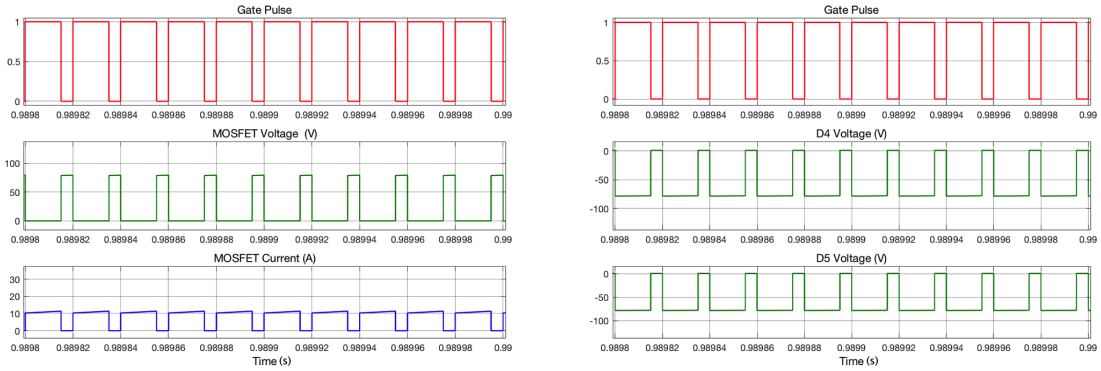
Table 2. Components specifications.

Parameter	Value	Unit
Input voltage (V_{in})	12	V
Output voltages (V_{out})	$-137/-87/-145$	V
Rated power (P_{out})	100	W
Switching frequency (f_s)	50	kHz
Duty cycle (D)	75%	-
Inductors ($L_1 \sim L_4$)	600	µH
Capacitors (C_1 and C_2)	22	µF
Load (R_L)	190/75/210	Ω

6.1. Topology-I

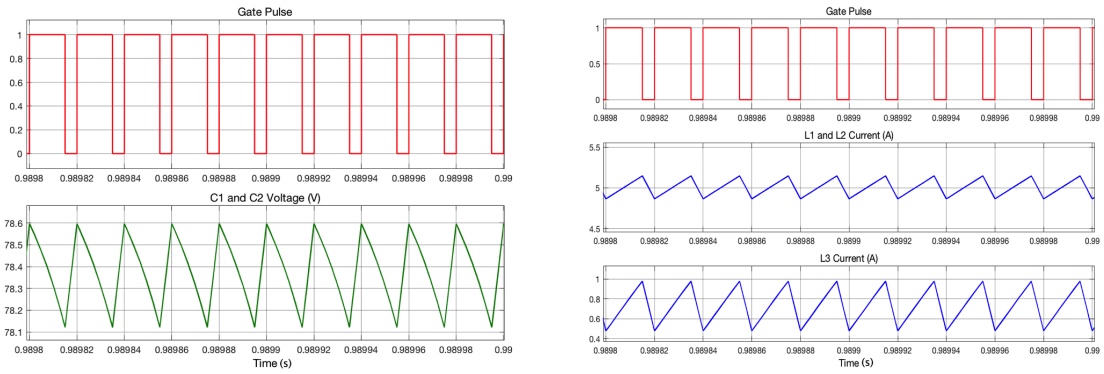
The SLSC Cuk converter topology-I is designed for -137 output voltage. The voltage stress and current stress on MOSFET S_1 are shown in Figure 12a. The voltage stress and current stress are approximately 78 V and 10 A, respectively. The voltage stress on the two diodes D_4 and D_5 of the

SC is shown in Figure 12b. The voltage stress across the two diodes of the SC is −78 V. Diodes D_4 and D_5 are conducting during the off time period of MOSFET S_1, and they are not conducting during the on time period of MOSFET S_1 as shown in Figure 12b. The voltage waveforms of capacitors C_1 and C_2 are shown in Figure 13a. From the figure, the two capacitors get charged when MOSFET S_1 is off, and they get discharged when MOSFET S_1 is on. The current waveforms of inductors L_1, L_2, and L_3 are shown in Figure 13b. The three inductors get charged when MOSFET S_1 is on, and they get discharged when MOSFET S_1 is off. The input voltage, output voltage, and output power waveforms are shown in Figure 14.



(**a**) (**b**)

Figure 12. Semiconductor devices' stresses of topology-I (**a**) Voltage and current stresses on S_1. (**b**) Voltage stresses on D_4 and D_5.



(**a**) (**b**)

Figure 13. Voltage waveform of the two capacitors of SC, current waveform of the two inductors of SL, and current of the output inductor of topology-I (**a**) Voltage waveform of C_1 and C_2. (**b**) Current waveforms of L_1,L_2, and L_3.

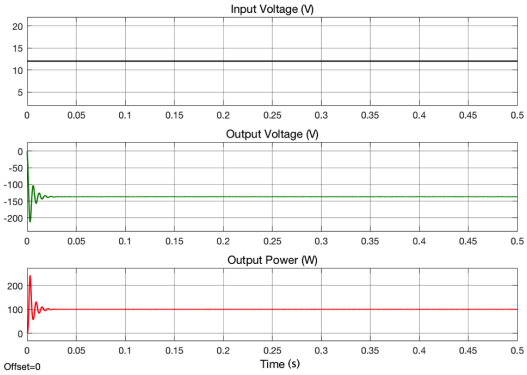
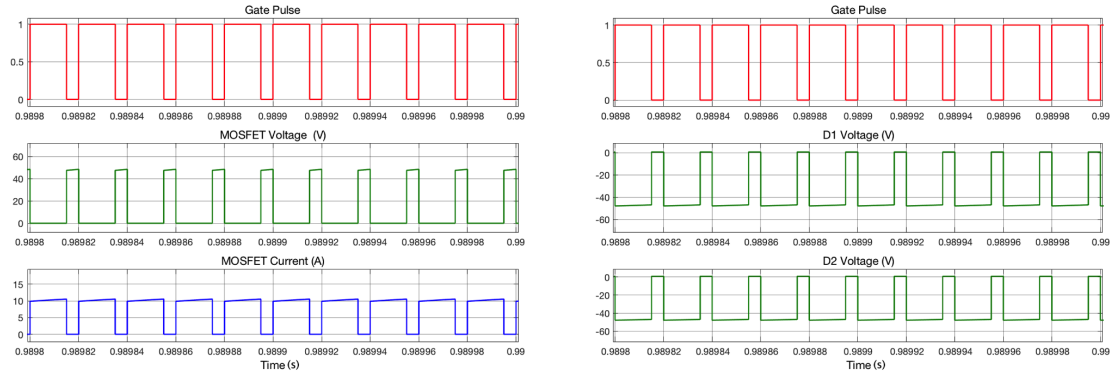


Figure 14. V_{in}, V_{out}, and P_{out} waveforms of topology-I.

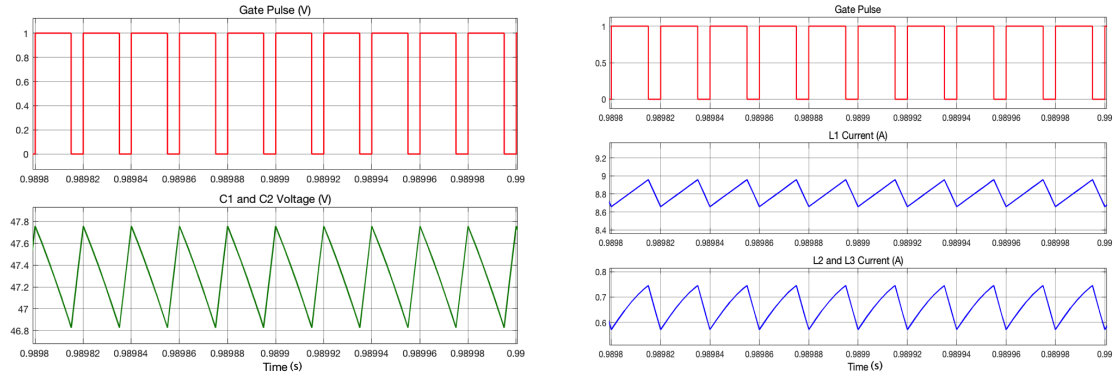
6.2. Topology-II

The SLSC Cuk converter topology-II is designed for −87 output voltage. The voltage stress and current stress on MOSFET S_1 are shown in Figure 15a. The voltage stress and current stress are approximately 48 V and 10 A, respectively. The voltage stress on the two diodes D_1 and D_2 of the SC is shown in Figure 15b. The voltage stress across the two diodes of the SC is −48V. Diodes D_1 and D_2 are conducting during the off time period of MOSFET S_1, and they are not conducting during the on time period of MOSFET S_1 as shown in Figure 15b. The voltage waveforms of capacitors C_1 and C_2 are shown in Figure 16a. From the figure, the two capacitors get charged when MOSFET S_1 is off, and they get discharged when MOSFET S_1 is on. The current waveforms of inductors L_1, L_2, and L_3 are shown in Figure 16b. The three inductors get charged when MOSFET S_1 is on, and they get discharged when MOSFET S_1 is off. The input voltage, output voltage, and output power waveforms are shown in Figure 17.



(**a**) (**b**)

Figure 15. Semiconductor devices' stresses of topology-II (**a**) Voltage and current stresses on S_1. (**b**) Voltage stresses on D_1 and D_2.



(**a**) (**b**)

Figure 16. Voltage waveform of the two capacitors of SC, current waveform of the two inductors of SL, and current of the output inductor of topology-II (**a**) Voltage waveform of C_1 and C_2. (**b**) Current waveforms of L_1,L_2, and L_3.

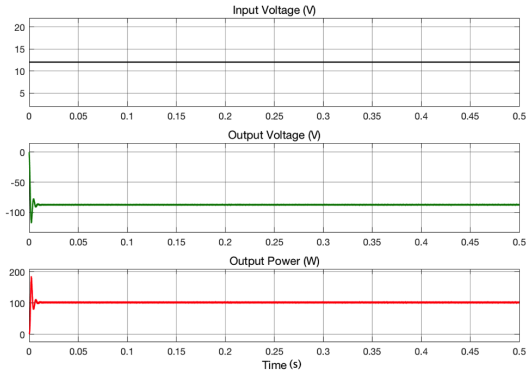
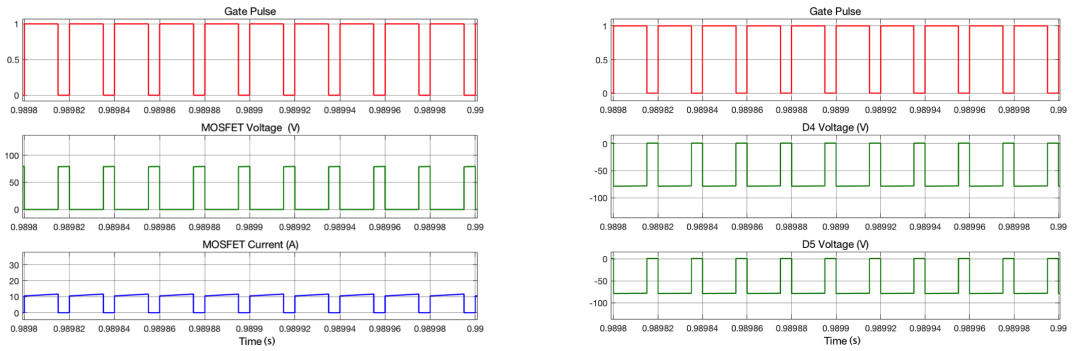


Figure 17. V_{in}, V_{out}, and P_{out} waveforms of topology-II.

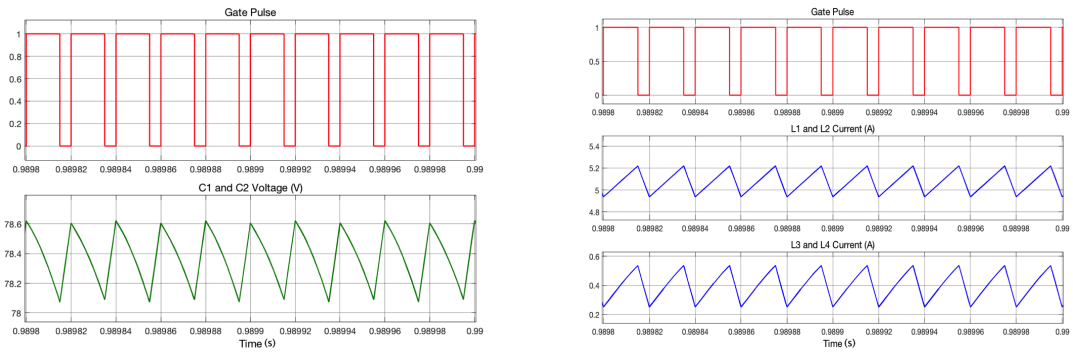
6.3. Topology-III

The SLSC Cuk converter topology-II is designed for −145 output voltage. The voltage and current stress on MOSFET S_1 are shown in Figure 18a. The voltage and current stress are approximately 78 V and 10 A, respectively. The voltage stress on the two diodes D_4 and D_5 of the SC is shown in Figure 18b. The voltage stress across the two diodes of the SC is −78 V. Diodes D_4 and D_5 are conducting during the off time period of MOSFET S_1, and they are not conducting during the on time period of MOSFET S_1 as shown in Figure 18b. The voltage waveforms of capacitors C_1 and C_2 are shown in Figure 19a. From the figure, the two capacitors get charged when MOSFET S_1 is off, and they get discharged when MOSFET S_1 is on. The current waveforms of inductors L_1, L_2, and L_3 are shown in Figure 19b. The three inductors get charged when MOSFET S_1 is on, and they get discharged when MOSFET S_1 is off. The input voltage, output voltage, and output power waveforms are shown in Figure 20.



(**a**) (**b**)

Figure 18. Semiconductor devices' stresses of topology-III (**a**) Voltage and current stresses on S_1. (**b**) Voltage stresses on D_4 and D_5.



(**a**) (**b**)

Figure 19. Voltage waveform of the two capacitors of SC, current waveform of the two inductors of SLs of topology-III (**a**) Voltage waveform of C_1 and C_2. (**b**) Current waveforms of L_1,L_2, L_3, and L_4.

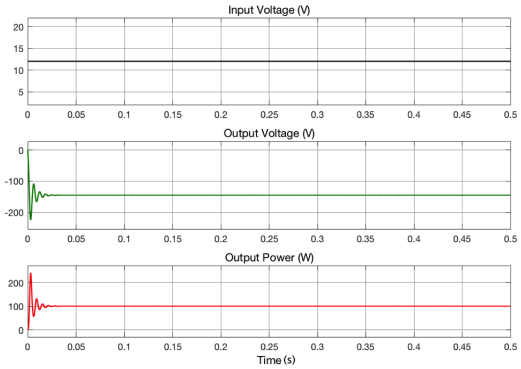


Figure 20. V_{in}, V_{out}, and P_{out} waveforms of topology-III.

6.4. Efficiency

An efficiency comparison between the three topologies of the proposed SLSC Cuk converter has been made using the numerical values assumed for parasitic parameters of the semiconductor switches shown in Table 3. The efficiency is graphically represented in Figure 21. Peak efficiencies of 86% for topology-I, 94.33% for topology-II, and 85% for topology-III are achieved when the output power is 120 W and the input voltage is 12 V. As highlighted by [28], The efficiency increases for higher input voltages because the input current decreases, and therefore, the conduction losses of power switches are reduced.

Table 3. Parasitic parameters of the semiconductor switches.

r_{DS-ON}	V_D	r_D
15 mΩ	0.7 V	30 mΩ

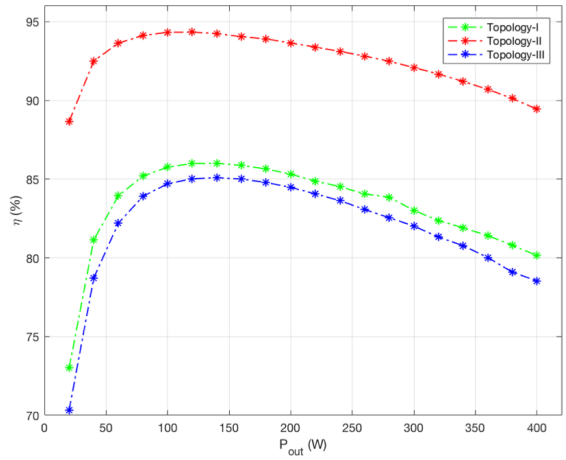


Figure 21. Efficiency curves as function of the output power.

7. Conclusions

This study has successfully developed three topologies of Cuk converters with high voltage gain and reduced active switch stress. This high voltage gain is accomplished without using a transformer, coupled inductors, or extreme duty cycle. The operation of the proposed converters was analyzed for continuous conduction mode. The proposed converters are regulated by the PWM technique at a constant frequency. Comparisons are made between the proposed converters, the classical Cuk converter, and the classical boost converter. The main advantages of the proposed converters include high voltage gain, low voltage stress which leads to select active switch with low voltage rating and

low R_{DS-ON}, continuous input and output current, use of single switch, high efficiency, and simplicity of the design. The steady-state analysis of the voltage gain is discussed in detail. The simulation results agree with the operating modes and the equations derived. The three converters are simulated using MATLAB/SIMULINK.

Author Contributions: Yasser Almalaq conceived and organized this work. Also, Yasser Almalaq performed the power simulations in the software MATLAB/SIMULINK and acquired and analyzed the data. Mohammad Matin provided the technical feedback and revised the manuscript. All authors proofread the manuscript.

Conflicts of Interest: The authors declare no conflict of interest.

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