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Improved Neutral-Point Voltage-Shifting Strategy for Power Balancing in Cascaded NPC/H-Bridge Inverter

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Abstract: This paper investigates the fault-tolerance control of a multilevel cascaded NPC/H-bridge (CNHB) inverter. The fault-tolerance control method has been widely used for multilevel inverters, such as the neutral-point voltage-shifting control, which can operate for a certain period of time by compensating for the phase voltage of a faulty stack even if one stack is broken. Even though the three-phase equilibrium is maintained in the case of failure by using the conventional neutral-point voltage-shifting control, an imbalance in the output power occurs between each stack, which causes problems for maintenance and lifetime. Therefore, this paper proposes a fault-tolerance control that can maintain three-phase equilibrium in a case of stack failures and minimize power imbalances between the stacks. The problem of the conventional neutral-point voltage-shifting control is presented based on the output power. In addition, the power imbalance is improved by performing selective neutral-point voltage-shifting control according to the reference voltage range. To verify the principle and feasibility of the proposed neutral-point voltage-shifting control method, a simulation and an experiment are implemented with the CNHB inverter.

Keywords: neutral-point voltage-shifting control; cascaded NPC/H-bridge inverter; power balancing

1. Introduction

Multilevel topology is widely used in high-power and high-voltage applications due to its lower total harmonic distortion (THD), lower filter size, and lower switching losses in each switching device than those of the conventional two-level PWM converters and inverters [1]. Each use of multilevel topology increases the number of voltage levels, making the output voltage even closer to the sinusoidal wave and reducing the harmonic distortion [2,3]. Among the various multilevel topologies, the cascaded NPC/H-bridge (CNHB) topology is advantageous in that it is easier to increase the output voltage levels and modularity than it is through the use of other topologies such as cascaded H-bridge (CHB), neutral-point clamped (NPC), and flying capacitor (FC) [4–6].

As shown in Figure 1, the CNHB inverter requires a large number of switching devices. This growing number of switching devices increases components such as signal cables and gate units, which can eventually lead to system failures more frequently. Especially in this system, when one power stack fault occurs by components, it can potentially lead to expensive downtime. This is the biggest disadvantage of the CNHB inverter [7–9].

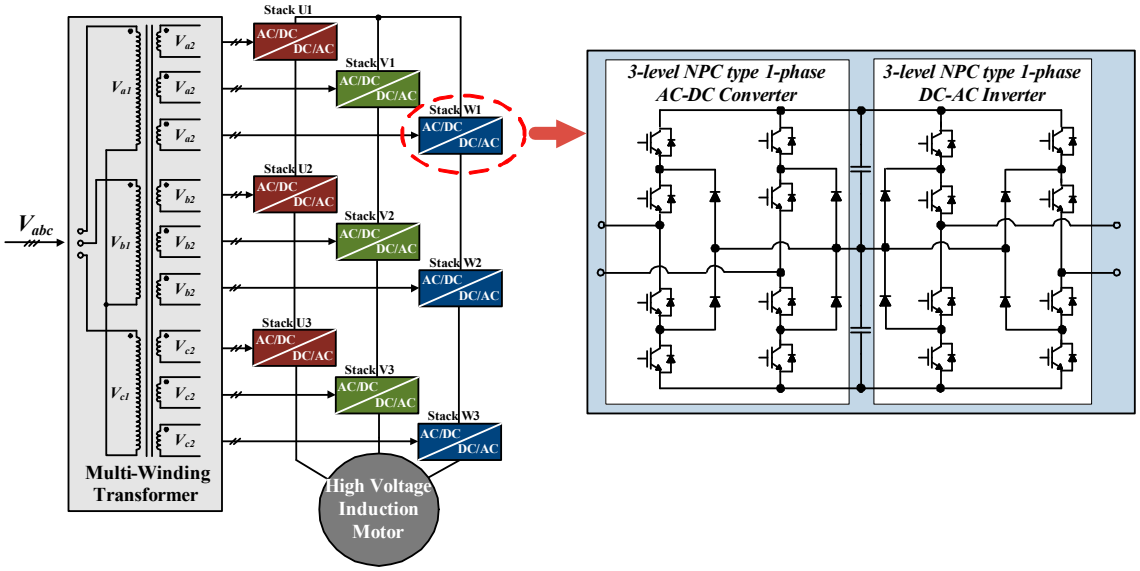

Figure 1. Configuration of 13-level cascaded NPC/H-bridge inverter with single-phase AFE (Active Front End) rectifier.

To solve this problem, the CNHB inverters have a controlling method for maintaining the reduced rated voltage and power rating in order to enable continuous operation even in the case that the switching device fails in open or short circuit. The so-called "fault tolerance" for cascaded inverters has been previously investigated in the literature [10–16].

Figure 2 shows the result of applying the neutral-point voltage-shifting control, which is a conventional fault-tolerance control method. The two failed stacks are bypassed, and through fundamental-frequency zero-sequence voltage injection, the magnitude and status of the phase voltage are adjusted so that the output line-to-line voltage has a phase difference of 120 degrees [17,18]. This neutral-point voltage-shifting control allows the entire system to be driven without stopping. However, there arises a problem in that the available voltage range of the system is reduced and the output power is unbalanced according to the number and distribution of fault stacks. [19,20].

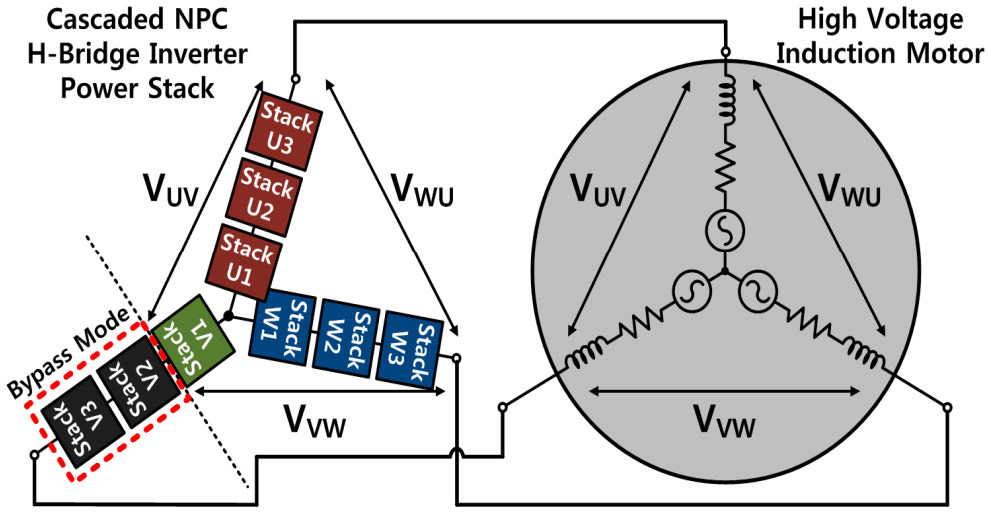

Figure 2. Neutral-point voltage-shifting control for high-voltage induction motor in failure situation of stack V2 and V3.

Therefore, this paper analyzes the conventional neutral-point voltage-shifting control for fault-tolerance control and proposes a novel neutral-point voltage-shifting control that can improve the individual stack output power imbalance caused by the conventional method.

This paper is organized as follows: Section 2 analyzes the conventional fault-tolerance control for CNHB inverter; Section 3 proposes a neutral-point voltage-shifting control that can maintain the RMS value of the output voltage of the individual stack and also describes the difference from the conventional method; Sections 4 and 5 give the simulation and experimental results for the validation of the proposed control method based on the adaptive filter; and Section 6 provides the conclusion.

2. Conventional Fault-Tolerance Control

2.1. Conventional Fault-Tolerance Control

Figure 3 shows the phase and line-to-line voltage vector diagrams for normal operation and bypass operation when only one stack fails [21]. As shown in Figure 3a, the output voltage of each phase is equal to the number of output voltage of each stack and the line voltage of the three-phase equilibrium appears in the absence of a failed stack. In this case, if a failure occurs on one stack of the U phase as shown in Figure 3b, the maximum voltage of the U phase is reduced. The V_{UV} and V_{WU} are line-to-line voltages affected by reduced magnitude and the status of the U phase voltage. Assuming that the three stacks are connected in series, the output phase voltage appears as shown in Equation (1), and the line-to-line voltage appears as shown in Equation (2). V_{DC} is the DC-link voltage of each phase; M_a is the amplitude of the reference voltage; V_U, V_V, and V_W are the phase voltages of the inverter; and V_{UV}, V_{VW}, and V_{WU} are the line voltage of the inverter.

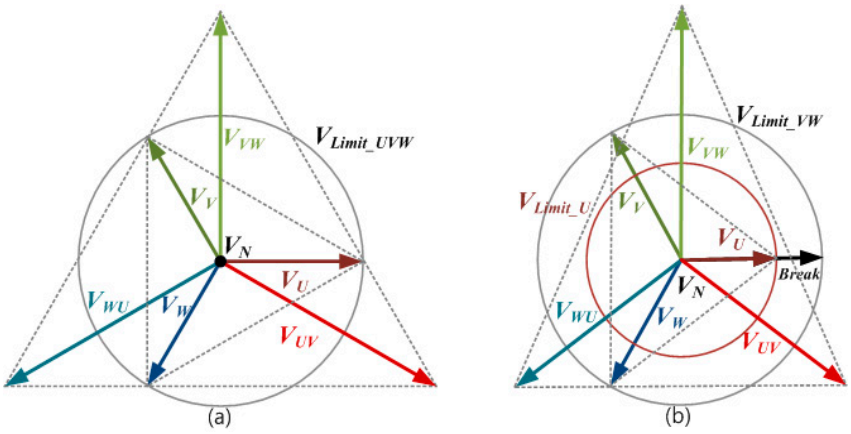

Figure 3. (**a**) Normal operation, (**b**) phase voltage and line-to-line voltage vector diagram of bypass operation when one failure occurs in the U stack.

$$\begin{aligned} V_U &= 2V_{DC}M_a\angle 0^\circ \\ V_V &= 3V_{DC}M_a\angle 120^\circ \\ V_W &= 3V_{DC}M_a\angle 240^\circ \end{aligned} \tag{1}$$

$$\begin{aligned} V_{UV} &= 2V_{DC}M_a\angle 0^\circ - 3V_{DC}M_a\angle 120^\circ \simeq \sqrt{19}V_{DC}M_a\angle -36.587^\circ \\ V_{VW} &= 3V_{DC}M_a\angle 0^\circ - 3V_{DC}M_a\angle 120^\circ \simeq 3\sqrt{3}V_{DC}M_a\angle 90^\circ \\ V_{WU} &= 3V_{DC}M_a\angle 240^\circ - 2V_{DC}M_a\angle 0^\circ \simeq \sqrt{19}V_{DC}M_a\angle -143.413^\circ \end{aligned} \tag{2}$$

When the phase voltage of the U phase is decreased as shown in Equation (2), the magnitude of each line-to-line voltage changes along with the phase, resulting in a three-phase imbalance based on the line-to-line voltage.

Figure 4 shows the application of a conventional neutral-point voltage-shifting control in the case of a single U phase stack failure. Figure 4a is a vector diagram showing the over-modulation phenomenon according to the existing neutral transition technique, and Figure 4b is a vector diagram considering the maximum voltage source of the inverter [22].

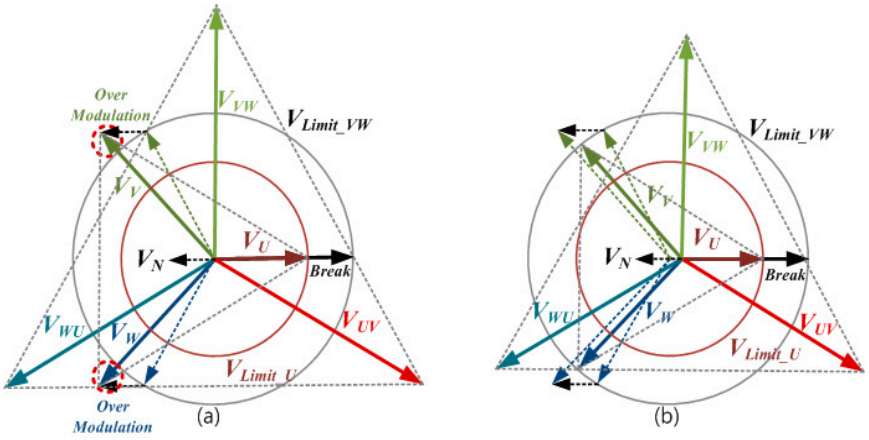

Figure 4. Conventional neutral-point voltage-shifting control of single U phase stack failure (**a**) over-modulation operation, (**b**) considering the maximum voltage source.

By injecting zero-sequence voltage, the phase voltage is applied to the other phase by a voltage that cannot be modulated on the failed phase, thus maintaining the three-phase equilibrium. Therefore, the voltage vector applied to each phase is one-third of the U phase voltage, and the phase voltages and line-to-line voltages corresponding to these voltages are given by Equations (3) and (4), respectively.

$$\begin{aligned} V_U &= 2V_{DC}M_a\angle 0^\circ \\ V_V &= 3V_{DC}M_a\angle 120^\circ - V_{DC}M_a\angle 0^\circ \simeq \sqrt{13}V_{DC}M_a\angle 133.898^\circ \\ V_W &= 3V_{DC}M_a\angle 240^\circ - V_{DC}M_a\angle 0^\circ \simeq \sqrt{13}V_{DC}M_a\angle -133.898^\circ \\ V_N &= (2V_{DC}\angle 0^\circ + \sqrt{13}V_{DC}\angle 133.898^\circ + \sqrt{13}V_{DC}\angle -133.898^\circ)/3 \simeq -V_{DC}\angle 0^\circ \end{aligned} \tag{3}$$

$$\begin{aligned} V_{UV} &= 2V_{DC}M_a\angle -13.9^\circ - \sqrt{13}V_{DC}M_a\angle 120^\circ = 3\sqrt{3}V_{DC}M_a\angle -30^\circ \\ V_{VW} &= \sqrt{13}V_{DC}M_a\angle 120^\circ - \sqrt{13}V_{DC}M_a\angle -106.1^\circ = 3\sqrt{3}V_{DC}M_a\angle 90^\circ \\ V_{WU} &= \sqrt{13}V_{DC}M_a\angle -106.1^\circ - 2V_{DC}M_a\angle -13.9^\circ = 3\sqrt{3}V_{DC}M_a\angle 150^\circ \end{aligned} \tag{4}$$

As shown in Equation (3), the V_N voltage appears to be the same as the offset voltage. By applying the neutral-point voltage-shifting control as shown in Equation (4), it can be seen that the line-to-line voltage is the same in magnitude and that the phase is different by 120 degrees.

Figure 5 shows a graph of the phase and line-to-line voltage characteristics for each time point using the conventional neutral-point voltage-shifting control when a single stack fault occurs. As shown in Figure 5, if the voltage is added to the reference voltage on V and W phase due to a failure of the U phase voltage, the V phase and W phase voltages can be varied, so that a three-phase balanced line-to-line voltage can be obtained. The phase and line-to-line voltage characteristics from t_0 to t_5 are as follows.

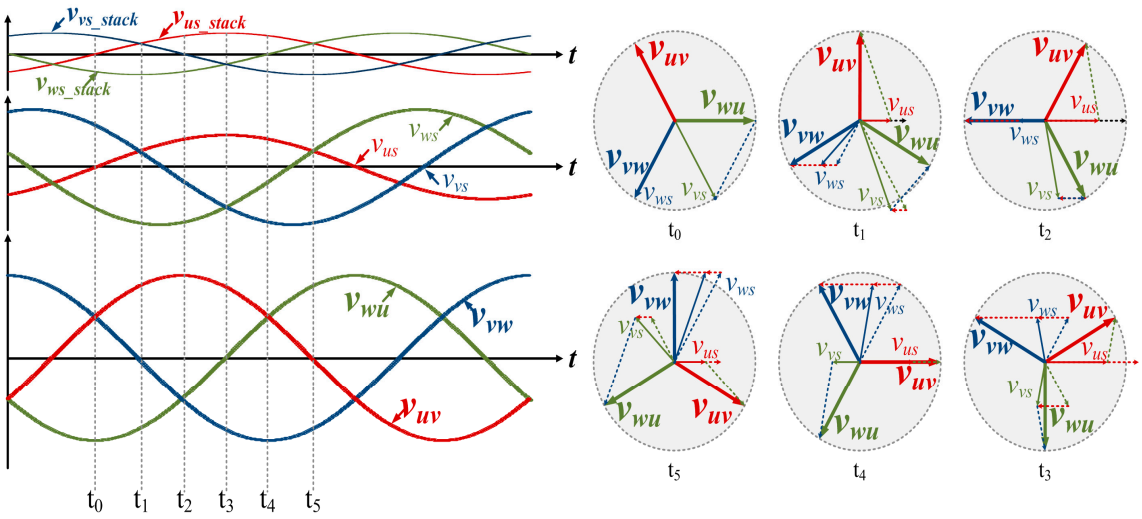

Figure 5. Vector diagram according to time applying the conventional neutral-point voltage-shifting control in case of stack failure.

t_0: The U phase voltage is 0 V, and the V and W phases are $-\sqrt{3}/2V_{peak\_xs}\angle 0°$ [V] and $-\sqrt{3}/2V_{peak\_xs}\angle 0°$ [V], respectively. The line-to-line voltage is then given by Equation (5).

$$\begin{aligned} V_{UV}(t_0) &= 0\angle 0° + \sqrt{3}/2V_{peak\_xs}\angle 120° = \sqrt{3}/2V_{peak\_xs}\angle 120° \\ V_{VW}(t_0) &= -\sqrt{3}/2V_{peak\_xs}\angle 120° - \sqrt{3}/2V_{peak\_xs}\angle 240° = \sqrt{3}/2V_{peak\_xs}\angle 0° \\ V_{WU}(t_0) &= \sqrt{3}/2V_{peak\_xs}\angle 240° - 0\angle 0° = \sqrt{3}/2V_{peak\_xs}\angle 240° \end{aligned} \tag{5}$$

t_1: The phase voltage on u is $1/3V_{peak\_xs}\angle 0°$ [V] due to the stack fault and the unmodulated voltage is $1/6V_{peak\_xs}\angle 0°$ [V]. When this voltage is applied to the V and W phase voltages, the V phase voltage becomes $\sqrt{7.75}/3V_{peak\_xs}\angle -68.948°$ [V] and the W phase voltage becomes $\sqrt{3.25}/3V_{peak\_xs}\angle -133.898°$ [V]. The line-to-line voltage can be expressed as follows:

$$\begin{aligned} V_{UV}(t_1) &= 1/3V_{peak\_xs}\angle 0° + \sqrt{7.75}/3V_{peak\_xs}\angle -68.948° \simeq \sqrt{3}/2V_{peak\_xs}\angle 90° \\ V_{VW}(t_1) &= -\sqrt{7.75}/3V_{peak\_xs}\angle -68.948° - \sqrt{3.25}/3V_{peak\_xs}\angle -133.898° \\ &= \sqrt{3}/2V_{peak\_xs}\angle -30° \\ V_{WU}(t_1) &= \sqrt{3.25}/3V_{peak\_xs}\angle -133.898° - 1/3V_{peak\_xs}\angle 0° \\ &\simeq \sqrt{3}/2V_{peak\_xs}\angle -150° \end{aligned} \tag{6}$$

t_2: The U phase voltage is $1/\sqrt{3}V_{peak\_xs}\angle 0°$ [V] and the unmodulated voltage is $1/2\sqrt{3}V_{peak\_xs}\angle 0°$ [V]. When this voltage is applied to the V and W phase voltages, the V phase voltage becomes $\sqrt{5.25}/3V_{peak\_xs}\angle -79.107°$ [V] and the W phase voltage becomes $-1/2\sqrt{3}V_{peak\_xs}\angle 0°$ [V]. The line-to-line voltage is given by Equation (7).

$$\begin{aligned} V_{UV}(t_2) &= 1/\sqrt{3}V_{peak\_xs}\angle 0° - \sqrt{5.25}/3V_{peak\_xs}\angle -79.107° \\ &\simeq \sqrt{3}/2V_{peak\_xs}\angle 60° \\ V_{VW}(t_2) &= \sqrt{5.25}/3V_{peak\_xs}\angle -79.107° + 1/2\sqrt{3}V_{peak\_xs}\angle 0° \\ &= \sqrt{3}/2V_{peak\_xs}\angle -60° \\ V_{WU}(t_2) &= -1/2\sqrt{3}V_{peak\_xs}\angle 0° - 1/\sqrt{3}V_{peak\_xs}\angle 0° = \sqrt{3}/2V_{peak\_xs}\angle 180° \end{aligned} \tag{7}$$

t_3: The U phase voltage is $2/3V_{peak\_xs}\angle 0°$ [V] and the unmodulated voltage is $1/3V_{peak\_xs}\angle 0°$ [V]. When this voltage is applied to the V and W phase voltages, the V phase voltage becomes

$\sqrt{1.75}/3V_{peak\_xs}\angle -100.893°$ [V] and the W phase voltage becomes $\sqrt{1.75}/3V_{peak\_xs}\angle 100.893°$ [V]. The line-to-line voltage can be expressed as follows:

$$\begin{aligned} V_{UV}(t_3) &= 2/3V_{peak\_xs}\angle 0° + \sqrt{1.75}/3V_{peak\_xs}\angle -100.893° \\ &\simeq \sqrt{3}/2V_{peak\_xs}\angle 30° \\ V_{VW}(t_3) &= \sqrt{1.75}/3V_{peak\_xs}\angle -100.893° - \sqrt{1.75}/3V_{peak\_xs}\angle 100.893° \\ &= \sqrt{3}/2V_{peak\_xs}\angle -90° \\ V_{WU}(t_3) &= \sqrt{1.75}/3V_{peak\_xs}\angle 100.893° - 2/3V_{peak\_xs}\angle 0° \\ &\simeq \sqrt{3}/2V_{peak\_xs}\angle 150° \end{aligned} \tag{8}$$

t_4: The U phase voltage is $1/\sqrt{3}V_{peak\_xs}\angle 0°$ [V] and the unmodulated voltage is $1/2\sqrt{3}V_{peak\_xs}\angle 0°$ [V]. When this voltage is applied to the V and W phase voltages, the V phase voltage becomes $-1/2\sqrt{3}V_{peak\_xs}\angle 0°$ [V] and the W phase voltage becomes $\sqrt{5.25}/3V_{peak\_xs}\angle 79.107°$ [V]. The line-to-line voltage can be expressed as follows:

$$\begin{aligned} V_{UV}(t_4) &= 1/\sqrt{3}V_{peak\_xs}\angle 0° + 1/2\sqrt{3}V_{peak\_xs}\angle 0° = \sqrt{3}/2V_{peak\_xs}\angle 0° \\ V_{VW}(t_4) &= -1/2\sqrt{3}V_{peak\_xs}\angle 0° - \sqrt{5.25}/3V_{peak\_xs}\angle 79.107° \\ &= \sqrt{3}/2V_{peak\_xs}\angle -120° \\ V_{WU}(t_4) &= \sqrt{5.25}/3V_{peak\_xs}\angle 79.107° - 1/\sqrt{3}V_{peak\_xs}\angle 0° \\ &\simeq \sqrt{3}/2V_{peak\_xs}\angle 120° \end{aligned} \tag{9}$$

t_5: The phase voltage on u is $1/3V_{peak\_xs}\angle 0°$ [V] and the unmodulated voltage is $1/6V_{peak\_xs}\angle 0°$ [V]. When this voltage is applied to the V and W phase voltages, the V phase voltage becomes $\sqrt{3.25}/3V_{peak\_xs}\angle 133.898°$ [V] and the W phase voltage becomes $\sqrt{7.75}/3V_{peak\_xs}\angle 68.948°$ [V]. The line-to-line voltage is given by Equation (10).

$$\begin{aligned} V_{UV}(t_5) &= 1/3V_{peak\_xs}\angle 0° - \sqrt{3.25}/3V_{peak\_xs}\angle 133.898° \\ &\simeq \sqrt{3}/2V_{peak\_xs}\angle -30° \\ V_{VW}(t_5) &= \sqrt{3.25}/3V_{peak\_xs}\angle 133.898° - \sqrt{7.75}V_{peak\_xs}\angle 68.948° \\ &= \sqrt{3}/2V_{peak\_xs}\angle -150° \\ V_{WU}(t_5) &= \sqrt{7.75}V_{peak\_xs}\angle 68.948° - 1/3V_{peak\_xs}\angle 0° \\ &\simeq \sqrt{3}/2V_{peak\_xs}\angle 90° \end{aligned} \tag{10}$$

By applying neutral-point voltage-shifting control, it can be seen that the line-to-line voltage for each time point from t_0 to t_5 is equal to the vector size and the phase difference is 120 degrees.

2.2. Power Characteristics of Each Module in Conventional Fault-Tolerance Control

Figure 6 shows the output voltage, phase current, and output power for the first stack of each phase, using the conventional neutral-point voltage-shifting control. As shown in Figure 6, when a failure occurs in the W phase stack, the reference voltages of the U and V phase increase. However, when the neutral-point voltage-shifting control is used, the three-phase equilibrium of the line-to-line voltage causes the three-phase equilibrium of the load phase voltage and phase current, and the three-phase equilibrium current flows in each stack. As a result, an unhealthy stack will be able to handle the additional power required by the failed stack, resulting in a power imbalance.

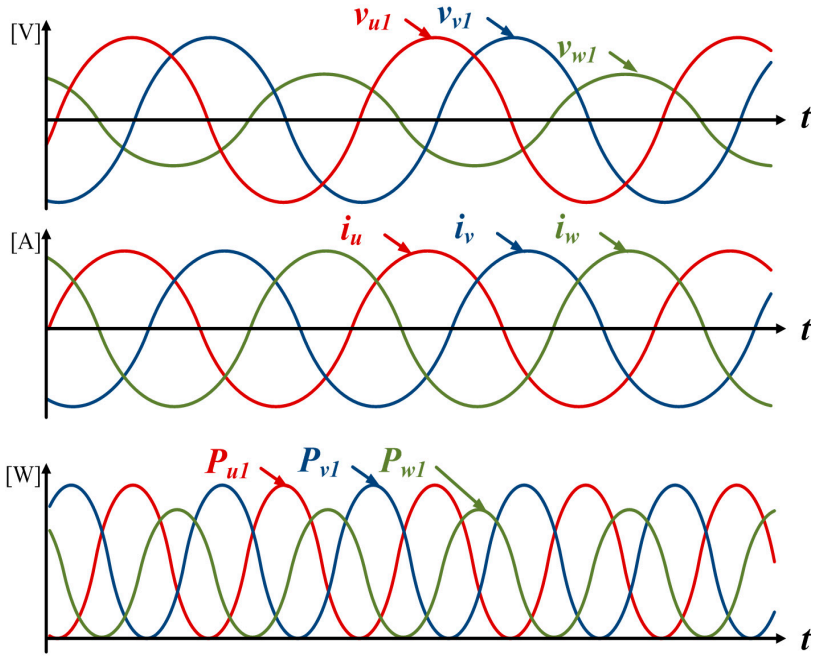

Figure 6. Stack voltage and phase current and stack power of each phase in conventional neutral-point voltage-shifting control.

Equation (11) represents the output voltage and phase current of the first stack of each phase, and Equation (12) represents the power per stack. In this case, the number of stacks is three, and Z_{X_motor} is the impedance to each phase of the motor.

$$\begin{aligned} v_{u1}(t) &= V_{DC}M_a \sin(\omega t) \\ v_{v1}(t) &= \sqrt{13}/3 V_{DC}M_a \sin(\omega t + 133.898^\circ) \\ v_{w1}(t) &= \sqrt{13}/3 V_{DC}M_a \sin(\omega t - 133.898^\circ) \\ i_u(t) &= 3V_{DC}M_a \sin(\omega t)/Z_{u\_motor} \\ i_v(t) &= 3V_{DC}M_a \sin(\omega t + 120^\circ)/Z_{v\_motor} \\ i_w(t) &= 3V_{DC}M_a \sin(\omega t - 120^\circ)/Z_{w\_motor} \end{aligned} \tag{11}$$

$$\begin{aligned} P_u(t) &= \frac{3(V_{DC}M_a)^2}{2Z_{u\_motor}}\{1 - \cos(2\omega t)\} \\ P_v(t) &= \frac{\sqrt{13}(V_{DC}M_a)^2}{2Z_{v\_motor}}\{\cos(13.898^\circ) - \cos(2\omega t + 253.898^\circ)\} \\ P_w(t) &= \frac{\sqrt{13}(V_{DC}M_a)^2}{2Z_{w\_motor}}\{\cos(13.898^\circ) - \cos(2\omega t - 253.898^\circ)\} \end{aligned} \tag{12}$$

Assuming that the impedance of each phase is the same, the average power for Equation (12) can be expressed as Equation (13).

$$\begin{aligned} P_u(t) &= \frac{3(V_{DC}M_a)^2}{2Z_{X\_motor}} = 1.5\frac{(V_{DC}M_a)^2}{Z_{u\_motor}} \\ P_v(t) &= \frac{\sqrt{13}(V_{DC}M_a)^2}{2Z_{X\_motor}}\cos(13.898^\circ) \simeq 1.75\frac{(V_{DC}M_a)^2}{Z_{v\_motor}} \\ P_w(t) &= \frac{\sqrt{13}(V_{DC}M_a)^2}{2Z_{X\_motor}}\cos(13.898^\circ) \simeq 1.75\frac{(V_{DC}M_a)^2}{Z_{w\_motor}} \end{aligned} \tag{13}$$

If a stack in one phase fails as shown in Equation (13), the stack that does not fail is approximately 16.7% more effective than the one with the failed stack using the conventional neutral-point voltage-shifting control.

The reason for this problem is that the RMS value of the reference voltage generated in each stack is different. In order to solve this problem, an additional method is needed for maintaining the RMS

value of the reference voltage so as to maintain the same output voltage of the individual stack while performing the neutral-point voltage-shifting control.

3. Proposed Fault-Tolerance Control

Figure 7 shows the time-dependent characteristics and the vector diagram of the proposed neutral-point voltage-shifting control. If one U phase stack fails, the phase voltage only changes in the colored area of the graph, and the phase voltage that was present in the uncolored area appears.

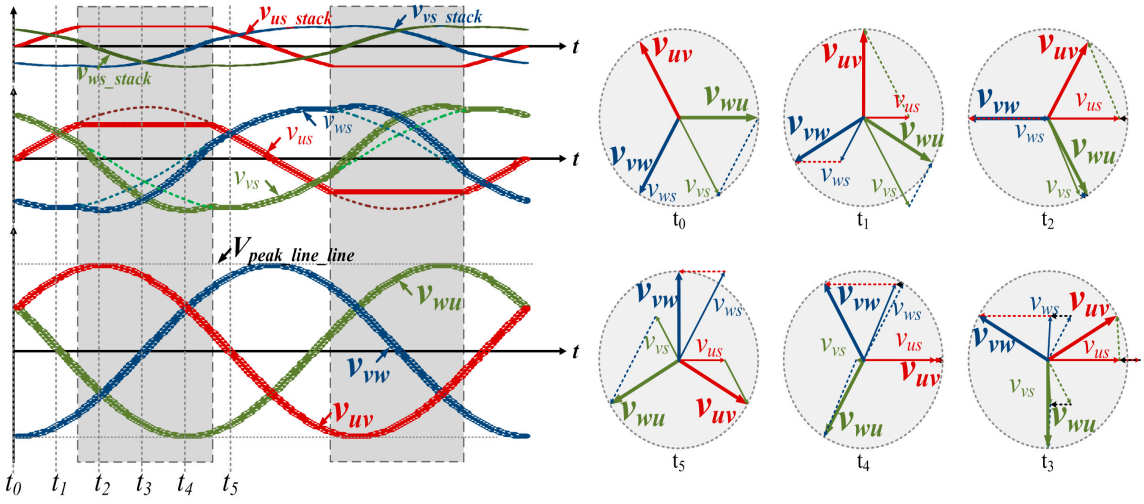

Figure 7. Time-dependent characteristics of proposed neutral-point voltage-shifting control.

When the stack failure of the CNHB inverter occurs, the maximum voltage that can be modulated is lowered in the phase including the faulty stack. The proposed control does not perform the neutral-point voltage-shifting control in all of the intervals, but rather performs it only as needed according to each interval. The characteristics of the proposed control for phase voltages and line-to-line voltages t_0 to t_5 are as follows:

t_0: The phase voltage of the phase is 0 [V], and the phases are shown as being $-\sqrt{3}/2V_{peak\_xs}\angle 120^\circ$ [V] and $\sqrt{3}/2V_{peak\_xs}\angle 120^\circ$ [V], respectively. In this case, since there is no phase voltage of U phase, the line-to-line voltage can be expressed as Equation (14):

$$\begin{aligned} V_{UV}(t_0) &= 0\angle 0^\circ + \sqrt{3}/2V_{peak\_xs}\angle 120^\circ = \sqrt{3}/2V_{peak\_xs}\angle 120^\circ \\ V_{VW}(t_0) &= -\sqrt{3}/2V_{peak\_xs}\angle 120^\circ - \sqrt{3}/2V_{peak\_xs}\angle 240^\circ = \sqrt{3}/2V_{peak\_xs}\angle 0^\circ \\ V_{WU}(t_0) &= \sqrt{3}/2V_{peak\_xs}\angle 240^\circ - 0\angle 0^\circ = \sqrt{3}/2V_{peak\_xs}\angle 240^\circ \end{aligned} \tag{14}$$

t_1: In the proposed control, the phase voltage of the three-phase equilibrium is modulated up to a certain voltage in the U phase including the failed stack. In this case, the phase voltage of the phase is $1/2V_{peak\_xs}\angle 0^\circ$ [V] and the phases are shown as $-V_{peak\_xs}\angle 120^\circ$ [V] and $1/2V_{peak\_xs}\angle 240^\circ$ [V], respectively. The line-to-line voltage can be expressed as Equation (15):

$$\begin{aligned} V_{UV}(t_1) &= 1/2V_{peak\_xs}\angle 0^\circ + V_{peak\_xs}\angle 120^\circ \simeq \sqrt{3}/2V_{peak\_xs}\angle 90^\circ \\ V_{VW}(t_1) &= -V_{peak\_xs}\angle 120^\circ - 1/2V_{peak\_xs}\angle 240^\circ = \sqrt{3}/2V_{peak\_xs}\angle -30^\circ \\ V_{WU}(t_1) &= 1/2V_{peak\_xs}\angle 240^\circ - 1/2V_{peak\_xs}\angle 0^\circ \simeq \sqrt{3}/2V_{peak\_xs}\angle -150^\circ \end{aligned} \tag{15}$$

t_2: In the proposed neutral-point voltage-shifting control, the fi is only used in the colored area. In Figure 7, the U phase voltage is only operated up to $\sqrt{3.25}/3V_{peak\_xs}\angle 0^\circ$ [V]. The voltage that should be output on U is $\sqrt{3}/2V_{peak\_xs}\angle 0^\circ$ [V], and the insufficient voltage is about $1/2\sqrt{3}V_{peak\_xs}\angle 0^\circ$ [V]. At this time, if the voltage which is insufficient in U is modulated on the V and W phases, the V phase

voltage is about $-\sqrt{5.25}/3V_{peak\_xs}\angle 103.495°$ [V] and the W phase voltage is about $1/2\sqrt{3}V_{peak\_xs}\angle 0°$. The line voltage is given by Equation (16):

$$\begin{aligned} V_{UV}(t_2) &= \sqrt{3.25}/3V_{peak\_xs}\angle 0° + \sqrt{5.25}/3V_{peak\_xs}\angle 103.495° \simeq \sqrt{3}/2V_{peak\_xs}\angle 60° \\ V_{VW}(t_2) &= -\sqrt{5.25}/3V_{peak\_xs}\angle 103.495° - 1/2\sqrt{3}V_{peak\_xs}\angle 0° \simeq \sqrt{3}/2V_{peak\_xs}\angle -60° \\ V_{WU}(t_2) &= 1/2\sqrt{3}V_{peak\_xs}\angle 0° - \sqrt{3.25}/3V_{peak\_xs}\angle 0° \simeq \sqrt{3}/2V_{peak\_xs}\angle 180° \end{aligned} \tag{16}$$

t_3: The phase voltage of the U phase maintains $\sqrt{3.25}/3V_{peak\_xs}\angle 0°$ [V] as in t_2. Accordingly, the insufficient voltage is $1/3V_{peak\_xs}\angle 0°$ [V], and when this voltage is compensated for, the V phase voltage and the W phase voltage are $\sqrt{1.75}/3V_{peak\_xs}\angle -107.557°$ [V] and $\sqrt{1.75}/3V_{peak\_xs}\angle 107.557°$ [V], respectively. The line voltage is given by Equation (17):

$$\begin{aligned} V_{UV}(t_3) &= \sqrt{3.25}/3V_{peak\_xs}\angle 0° - \sqrt{1.75}/3V_{peak\_xs}\angle -107.557° \\ &\simeq \sqrt{3}/2V_{peak\_xs}\angle 30° \\ V_{VW}(t_3) &= \sqrt{1.75}/3V_{peak\_xs}\angle -107.557° - \sqrt{1.75}/3V_{peak\_xs}\angle 107.557° \\ &\simeq \sqrt{3}/2V_{peak\_xs}\angle -90° \\ V_{WU}(t_3) &= \sqrt{1.75}/3V_{peak\_xs}\angle 107.557° - \sqrt{3.25}/3V_{peak\_xs}\angle 0° \\ &\simeq \sqrt{3}/2V_{peak\_xs}\angle 150° \end{aligned} \tag{17}$$

t_4: The phase voltage of the U phase maintains $\sqrt{3.25}/3V_{peak\_xs}\angle 0°$ [V] as in t_3. Accordingly, the insufficient voltage is $1/2\sqrt{3}V_{peak\_xs}\angle 0°$ [V], and when this voltage is compensated for, the V phase voltage and the W phase voltage are $-1/2\sqrt{3}V_{peak\_xs}\angle 0°$ [V] and $\sqrt{5.25}/3V_{peak\_xs}\angle 76.5°$ [V], respectively. The line voltage is given by Equation (18).

$$\begin{aligned} V_{UV}(t_4) &= \sqrt{3.25}/3V_{peak\_xs}\angle 0° + 1/2\sqrt{3}V_{peak\_xs}\angle 0° \simeq \sqrt{3}/2V_{peak\_xs}\angle 0° \\ V_{VW}(t_4) &= -1/2\sqrt{3}V_{peak\_xs}\angle 0° - \sqrt{5.25}/3V_{peak\_xs}\angle 76.5° \\ &\simeq \sqrt{3}/2V_{peak\_xs}\angle -120° \\ V_{WU}(t_4) &= \sqrt{5.25}/3V_{peak\_xs}\angle 76.5° - \sqrt{3.25}/3V_{peak\_xs}\angle 0° \simeq \sqrt{3}/2V_{peak\_xs}\angle 120° \end{aligned} \tag{18}$$

t_5: Since the phase voltage of the U phase should output a voltage less than $0.613V_{peak\_xs}\angle 0°$ [V] at $1/2V_{peak\_xs}\angle 0°$ [V], the neutral-point voltage-shifting control is not performed. Accordingly, V phase voltage and W phase voltage are output at $1/2V_{peak\_xs}\angle 120°$ [V] and $-V_{peak\_xs}\angle 240°$ [V], respectively. Therefore, the line voltage can be expressed by Equation (19).

$$\begin{aligned} V_{UV}(t_5) &= 1/2V_{peak\_xs}\angle 0° - 1/2V_{peak\_xs}\angle 120° = \sqrt{3}/2V_{peak\_xs}\angle -30° \\ V_{VW}(t_5) &= 1/2V_{peak\_xs}\angle 120° + 1V_{peak\_xs}\angle 240° = \sqrt{3}/2V_{peak\_xs}\angle -150° \\ V_{WU}(t_5) &= -V_{peak\_xs}\angle 240° - 1/2V_{peak\_xs}\angle 0° = \sqrt{3}/2V_{peak\_xs}\angle 90° \end{aligned} \tag{19}$$

This proposed control uses only the neutral-point voltage-shifting control as needed for the reference voltage of the fault including the faulty stack at a voltage higher than a certain voltage, so that fault-tolerance control can be effectively performed. It is capable of randomly selecting the voltage to be maintained as shown in Equations (16)–(19). Therefore, the selected voltage compensates only for the voltage that cannot be output.

Figure 8 shows the individual stack reference voltage when one U phase stack fails. Because one stack is broken, only the remaining two stacks are used to produce the same output voltage as the three stacks. Therefore, multiplying the ratio of 1.5 by the reference voltage increases the reference voltage M_a of the two stacks. Therefore, when the maximum and minimum values are selected for the increased reference voltage, the U phase individual stack reference voltage is generated, as shown in the red line in Figure 8. At this point, if the difference between the previous value and the subsequent value is subtracted from the V phase and the W phase, separate stack reference voltages, like the green line and blue line in Figure 8, are generated. In this paper, the criteria for selecting the maximum and

minimum values for the proposed neutral-point voltage-shifting control is selected as the limit value at which the RMS value of the output phase voltage of the individual stack becomes equal. This control method that is proposed enables the same output power for each stack.

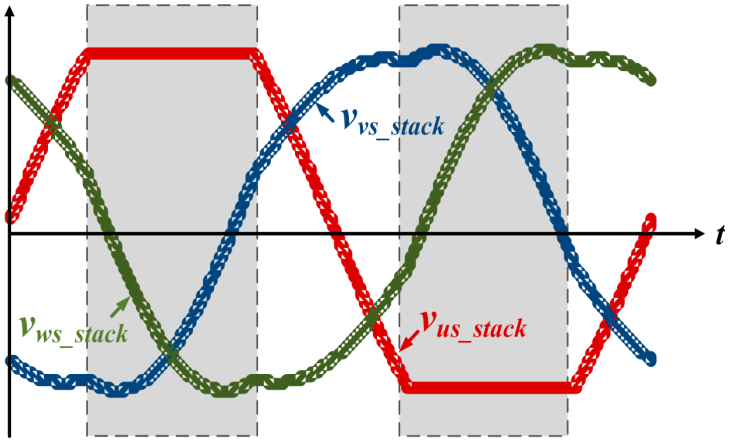

Figure 8. The individual stack reference voltage of proposed neutral-point voltage-shifting control.

Figure 9 shows a quarter period waveform of each stack reference voltage when the proposed neutral-point voltage-shifting control is used for U phase failure. v_{us_real} is the reference voltage before limit and v_{us_comp} is the reference voltage after limit. In this paper, in order to calculate the RMS value of the proposed reference voltage, the reference voltage on the non-sinusoidal periodic U is constructed as a primitive function. Then, the RMS values at t_1 and t_2 with respect to the 1/4 periodic wave are respectively calculated and added.

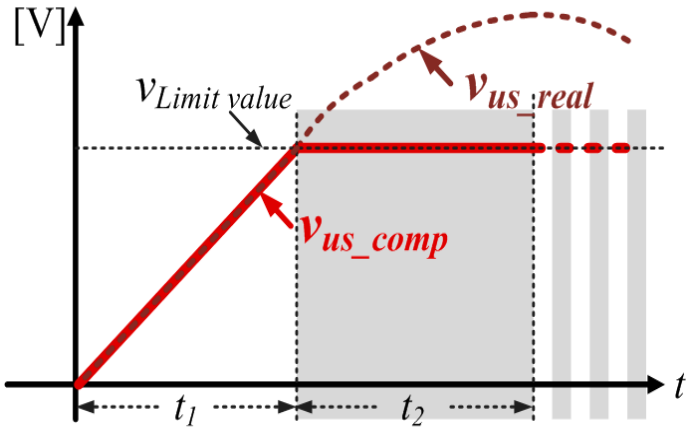

Figure 9. One-quarter of the U phase command voltage of the proposed neutral-point voltage-shifting control.

To calculate the RMS value, a calculation for t_1 is necessary. Since v_{us_real} and v_{us_comp} are the same during t_1, they can be expressed as Equation (20).

$$v_{us\_real} = \alpha V_{peak\_us} \sin \omega t \tag{20}$$

The time t_1 at which the reference voltage reaches the maximum value can be expressed by Equation (21) using Equation (20).

$$t_1 = \frac{\sin^{-1}\left(\frac{v_{Limit\_value}}{\alpha V_{peak\_us}}\right)}{\omega} \tag{21}$$

Through Equation (21), the RMS value of the reference voltage during the period t_1 can be expressed as Equation (22).

$$\begin{aligned} V_{rms\_t_1} &= \sqrt{\frac{1}{T}\int_0^{t_1}\left(\alpha V_{peak\_us}\sin\omega t\right)dt} \\ &= \sqrt{\frac{\alpha V_{peak\_us} - \sqrt{\alpha^2 V_{peak\_us}^2 - v_{Limit\_value}^2}}{2\pi}} \end{aligned} \tag{22}$$

The time t_2 can be expressed as Equation (23), and the RMS value can be expressed as Equation (24).

$$t_2 = \frac{\pi}{2\omega} - t_1 = \frac{1}{\omega}\left\{\frac{\pi}{2} - \sin^{-1}\left(\frac{v_{Limit\_value}}{\alpha V_{peak\_us}}\right)\right\} \tag{23}$$

$$V_{rms\_t_2} = t_2 \times v_{Limit\_value} = \frac{v_{Limit\_value}}{\omega}\left\{\frac{\pi}{2} - \sin^{-1}\left(\frac{v_{Limit\_value}}{\alpha V_{peak\_us}}\right)\right\} \tag{24}$$

Figure 10 shows a quarter period waveform of V phase stack reference voltage when using the proposed neutral-point voltage-shifting control for U phase failure. $v_{us\_remaind}$ is the value obtained by subtracting v_{us_real} from v_{us_comp} in Figure 10. In order to calculate the RMS value of the V phase reference voltage, the reference voltage on the non-sinusoidal phase V is constructed as a base function, and then the RMS value of v_{us_real} and the RMS value of $v_{us\_remaind}$ are calculated.

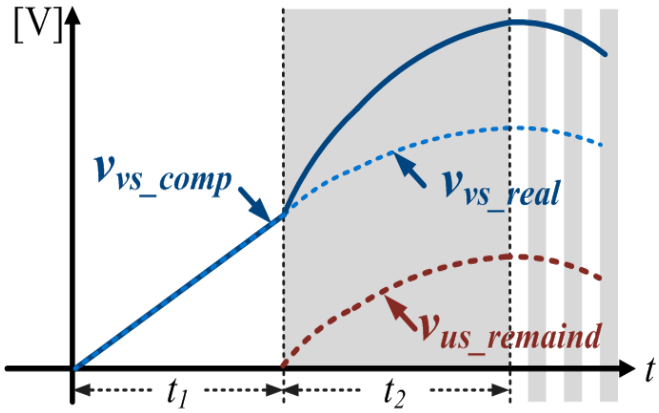

Figure 10. One-quarter of the V phase command voltage of the proposed neutral-point voltage-shifting control.

The quarter-period RMS value for v_{us_real} is given by Equation (25).

$$V_{rms\_v_{vs\_real}} = \frac{V_{peak\_vs}}{4\sqrt{2}} \tag{25}$$

The RMS value for $v_{us\_remaind}$ can be expressed by Equation (26) using Equations (24) and (25).

$$\begin{aligned} V_{rms\_v_{us\_remain}} &= \sqrt{\frac{1}{T}\int_{t_1}^{t_2}\left(\alpha V_{peak\_us}\sin\omega t\right)dt} - V_{rms\_t_2} \\ &= \sqrt{\frac{\sqrt{\alpha^2 V_{peak\_us}^2 - v_{Limit\_value}^2} - v_{Limit\_value}}{2\pi}} - \frac{v_{Limit\_value}}{\omega}\left\{\frac{\pi}{2} - \sin^{-1}\left(\frac{v_{Limit\_value}}{\alpha V_{peak\_us}}\right)\right\} \end{aligned} \tag{26}$$

The proposed control assigns v_{Limit_value} so that the value obtained by adding the RMS values of Equations (22) and (24) is equal to the sum of Equations (25) and (26). This can be expressed as Equation (27).

$$\begin{aligned} &V_{rms\_t_1} + V_{rms\_t_2} = V_{rms\_v_{us\_real}} + V_{rms\_v_{vs\_real}} \\ &v_{Limit\_value} \fallingdotseq 0.9292 \end{aligned} \tag{27}$$

Figure 11 shows the waveforms of the individual stack voltage waveforms, the phase voltage, the phase current, and the stack power in the proposed neutral-point voltage-shifting control. As shown in Figure 11, if the RMS value of each stack reference voltage is kept the same, the average value of output power of each stack can be the same. Therefore, even if the stack fails, the line-to-line voltage maintains three-phase equilibrium, and the output power imbalance, which is a disadvantage of the conventional neutral-point voltage-shifting control, can be improved.

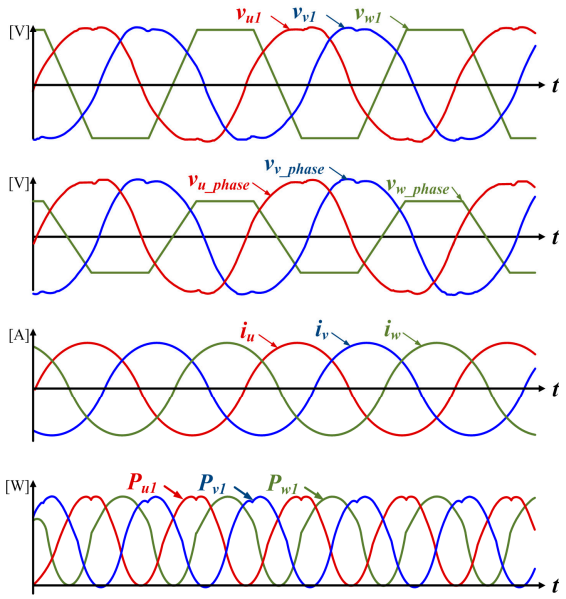

Figure 11. The main waveforms in the proposed neutral-point voltage-shifting control.

Figure 12 shows a block diagram of the proposed fault-tolerance control. The proposed control consists of three major parts: the part that varies the reference of the phase voltage and the reference voltage limiter, the part that subtracts the difference between the previous value and the subsequent value of each phase from the other phase reference voltage, and the part that calculates the maximum and minimum values of the reference voltage and limiter for the neutral-point voltage-shifting control.

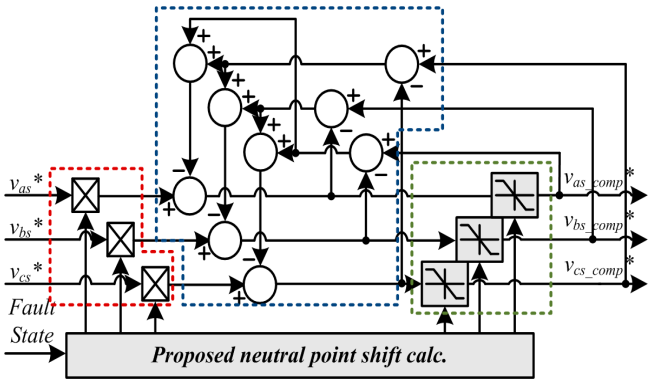

Figure 12. Proposed fault-tolerance control block diagram.

Figure 13 shows a schematic configuration and a control block diagram of a single cascaded NPC/H-bridge system using the proposed neutral-point voltage-shifting control. As shown in Figure 13, the system dealt with in this paper consists of NPC/H-bridge inverter and NPC/H-bridge converter in back to back. The NPC/H-bridge converter performs grid power factor control, DC-link voltage control, and DC-link neutral-point voltage-balancing control. In this case, the DC-link is represented by an equivalent circuit and the control block diagram of the 13-level cascaded NPC/H-bridge inverter is shown in Figure 14.

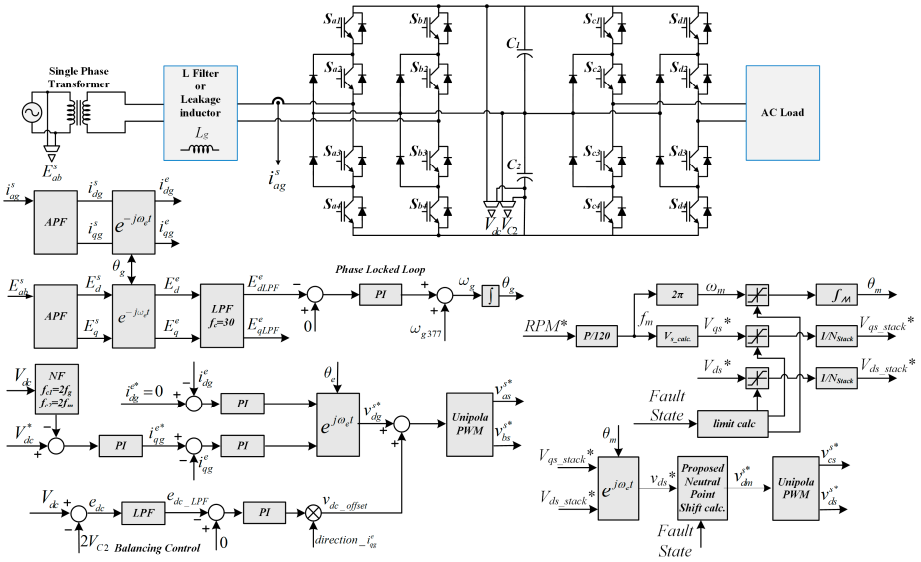

Figure 13. Control block diagram of one stack used in cascaded NPC/H-bridge system.

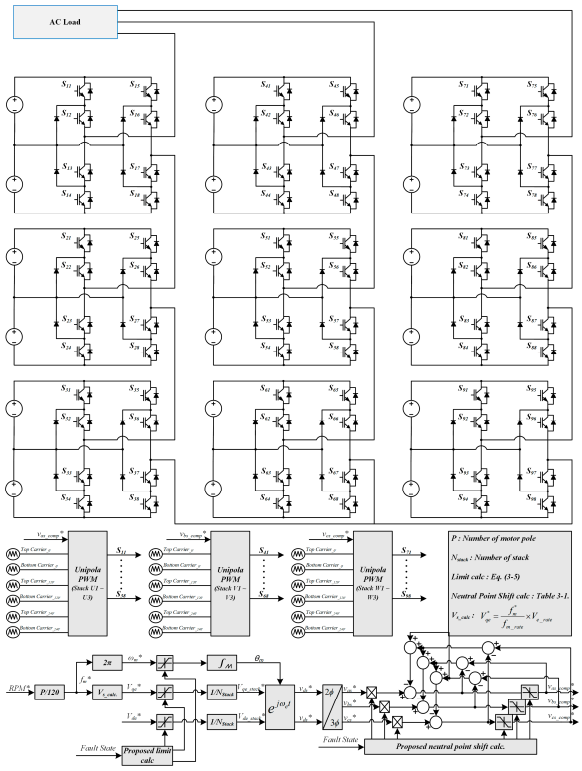

Figure 14. Proposed fault-tolerance control block diagram used in 13-level cascaded NPC/H-bridge inverter.

As shown in Figure 14, the proposed neutral-point voltage-shifting control is applied based on the V/F control method, and the maximum voltage and the maximum speed according to the fault state are set in the same condition as the conventional method.

4. Simulation Results

In order to verify the principle and feasibility of the proposed control method, a simulation has been developed using the PSIM software program. The simulation schematic in the 13-level cascaded NPC/H-bridge system is illustrated in Figure 1. The systems parameters of the simulation and experiment are shown in Table 1.

Table 1. Simulation and experiment parameters.

Parameter	Value	Unit	Parameter	Value	Unit
DC-link voltage	120	V	Filter inductance	1	mH
Rated power	15	kW	DC-link capacitance	4	mF
Rated voltage	380	Vrms	Switching frequency	10	kHz
Rated current	27.8	Arms	Rated power of each stack	1.1	kW

Figure 15 shows the operating waveform of the 13-level NPC/H-bridge converter and inverter. As shown in Figure 15, the converter was operated at first to control the DC-link voltage. Then the inverter reached the steady state and the inverter was operated.

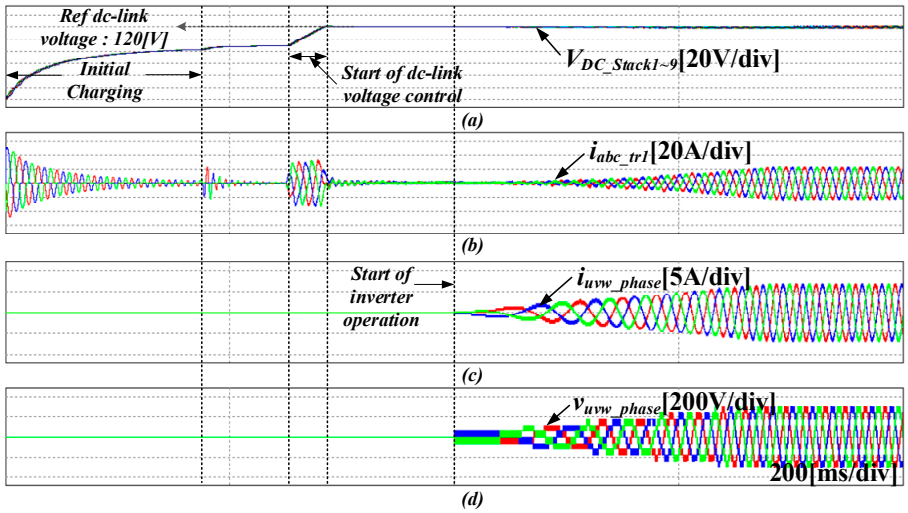

Figure 15. Simulation results of the 13-level cascaded NPC/H-bridge system (**a**) DC-link voltage, (**b**) input current of the converter, (**c**) output current of the inverter, (**d**) output voltage of the inverter.

Figure 16 shows the simulation result of the NPC/H-bridge converter applying the neutral-point voltage-balancing control of the DC-link mentioned in Figure 13. In the process of operating the 13-level NPC/H-bridge inverter, when imbalance occurs in the neutral voltage of the DC-link due to stack faults or sudden load change, it affects the output current of the inverter. Therefore, the neutral-point voltage balancing of the DC-link is continuously performed in the NPC/H-bridge converter. The simulations artificially applied an unbalanced load to the DC-link to verify the neutral-point voltage-balancing control and performed the balancing control at a certain point in time. As can be seen from the waveform of the simulation, the DC-link voltage-balancing control is performed stably even if the voltage of the top and bottom capacitors is unbalanced.

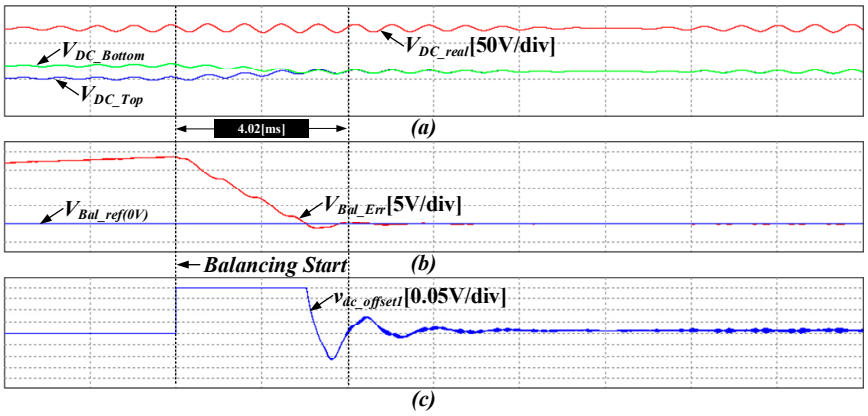

Figure 16. Simulation results of the DC-link neutral-point voltage balance used in 13-level cascaded NPC/H-bridge (**a**) DC-link voltage, (**b**) reference and error voltage between top capacitor and bottom capacitor, (**c**) offset voltage for DC-link voltage balancing.

Figure 17 shows the simulation waveform for the failure of the V phase fourth stack of the 13-level NPC/H-bridge inverter. The waveforms are, in order, individual stack reference voltage on U, V, W, output voltage of the first to ninth stack, voltage on U, V, W; line-to-line voltage of UV, VW, WU; phase voltage of U, V, W; and phase current.

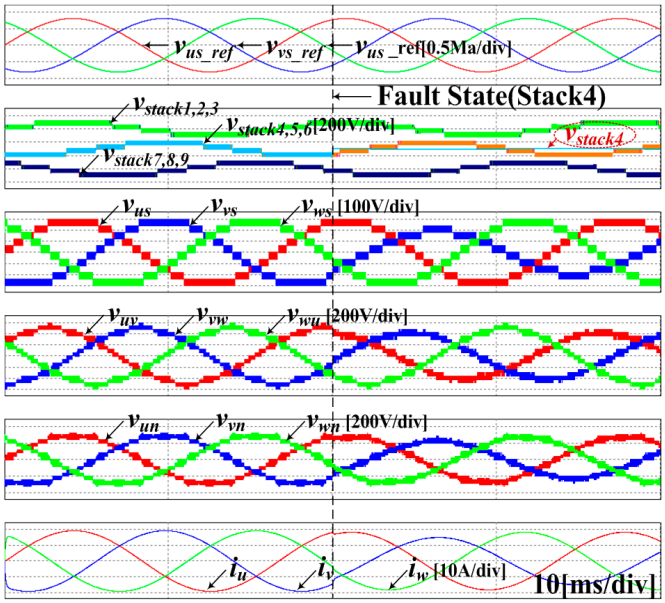

Figure 17. Simulation waveform when V phase 4th stack fails.

When operating with a reference voltage of three-phase equilibrium when a stack fault occurs as shown in Figure 17, the phase voltage of the phase including the fault stack, as the V phase voltage, is reduced and the three-phase equilibrium of the phase current is not made. Therefore, it is necessary to maintain the three-phase equilibrium of the line voltage using the neutral-point voltage-shifting control.

Figure 18 shows simulation waveform when V phase fourth stack fails in applying the conventional neutral-point voltage-shifting control. The order of the waveforms is the same as in Figure 17. In case of fault, the phase voltages of the U and W phases are larger than that of the V phase, but the line-to-line voltage for UV, VW, and WU is shown as three-phase equilibrium. This results

in a three-phase equilibrium between the load voltage. The load current will also have three-phase equilibrium flowing through it.

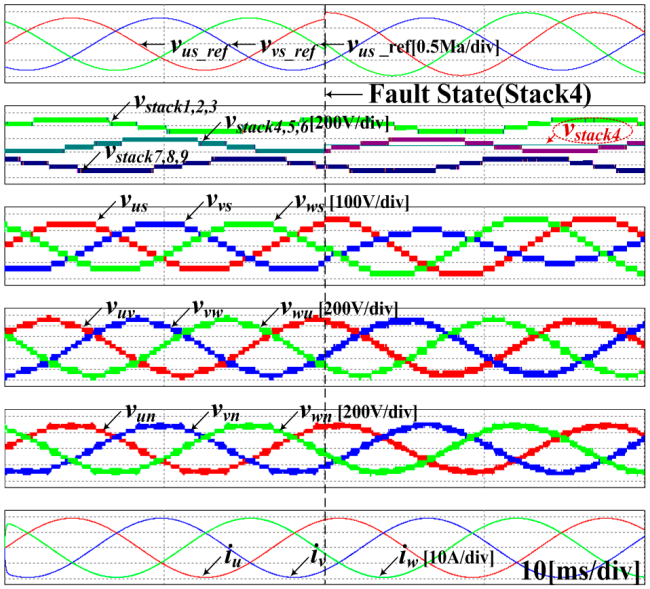

Figure 18. Simulation waveform when V phase fourth stack fails in applying the conventional neutral-point voltage-shifting control.

However, when using the conventional neutral-point voltage-shifting control, an output power imbalance occurs between the individual stacks, as shown in Figure 19. The RMS values of the average power and reference voltage are summarized in Table 2 when using the conventional neutral-point voltage-shifting control shown in Figure 19.

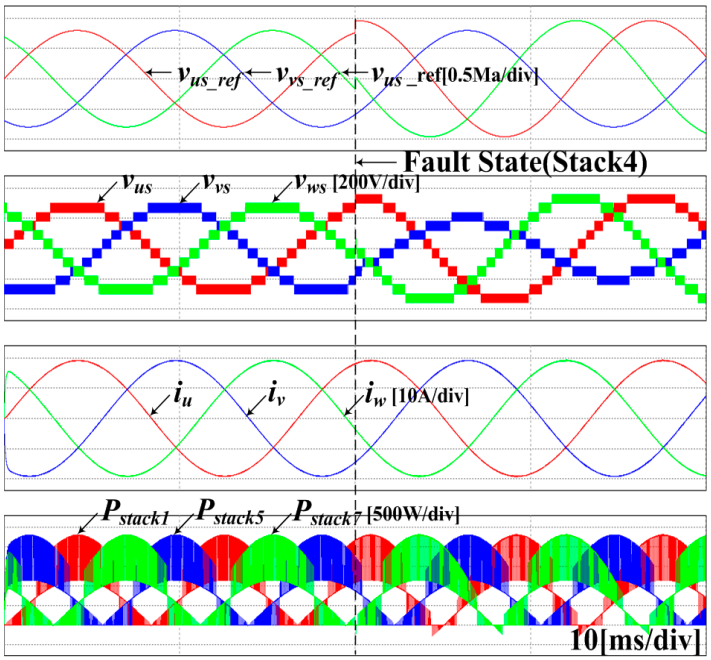

Figure 19. Simulation waveform of individual stack power when V phase fourth stack fails in applying the conventional neutral-point voltage-shifting control.

Table 2. Comparison of RMS values of average output power and reference voltage when fourth stack fails in applying the conventional neutral-point voltage-shifting control.

Unit	Stack 1 (U Phase)	Stack 5 (V Phase)	Stack 7 (W Phase)
Average output power [W]	1018.57	930.84	1121.055
Reference voltage [V]	0.665	0.57	0.694

Figure 20 shows the simulation waveform of the proposed neutral-point voltage-shifting control for V phase fourth stack failure. The order of the simulation waveform is the same as those in Figures 17 and 18. In the case of the proposed control, the reference voltage for the neutral-point voltage-shifting control is formed while the RMS value of the reference voltage is kept the same.

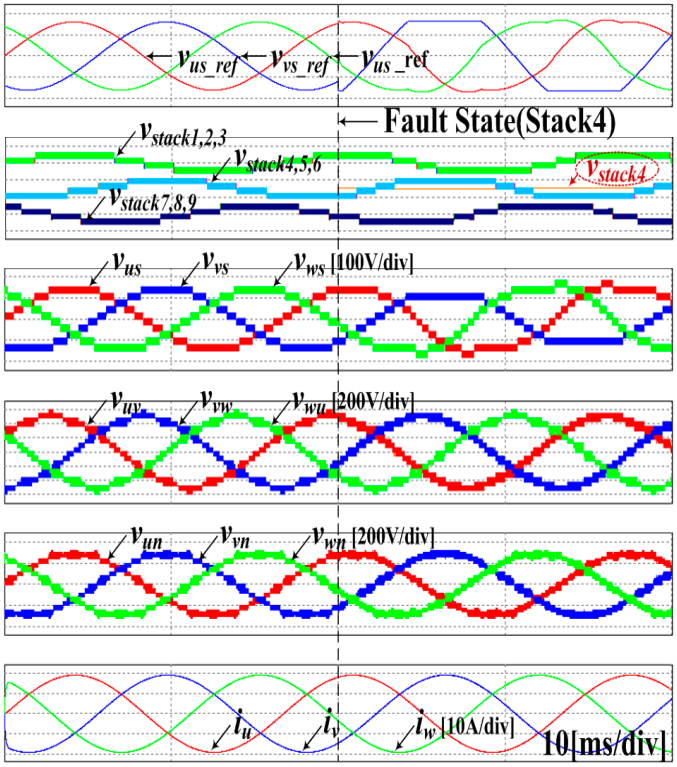

Figure 20. Simulation waveform when V phase fourth stack fails in applying the proposed neutral-point voltage-shifting control.

Figure 21 shows the simulation waveform including the individual stack power when using the proposed neutral-point voltage-shifting control. In the proposed control, the faulty stack increases the Ma value to increase the RMS value, and there is a section that maintains the DC type reference voltage like the blue line of the first waveform in Figure 21 while passing through the limit function. The reference voltage and the phase voltage are modulated while the U and W phase reference voltages perform the neutral-point voltage-shifting control by this interval.

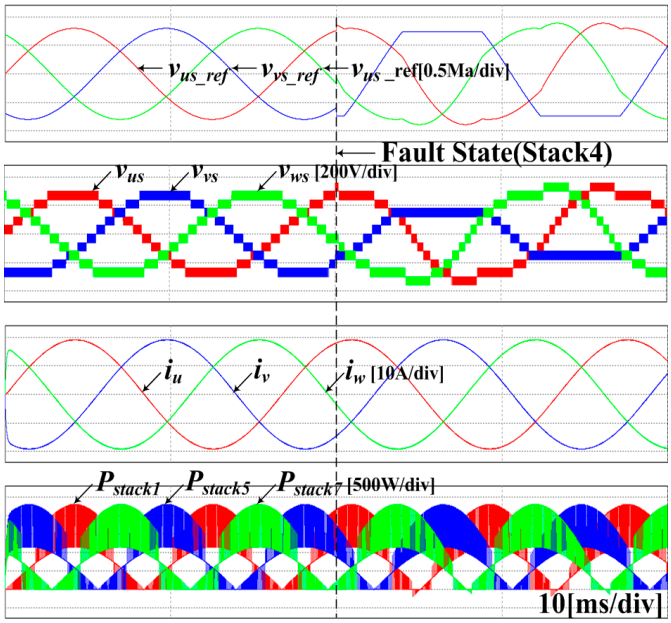

Figure 21. Simulation waveform of individual stack power when V phase fourth stack fails in applying the proposed neutral-point voltage-shifting control.

As a result of the selective neutral-point voltage-shifting control, the three-phase balance of the load current is maintained, and the RMS values of the average output power and the reference voltage are shown in Table 3. In addition, the phase current THD of the proposed method is compared with that of the conventional method, as shown in Table 4.

Table 3. Comparison of RMS value of average output power and reference voltage when fourth stack fails in applying the proposed neutral-point voltage-shifting control.

Unit	Stack 1 (U Phase)	Stack 5 (V Phase)	Stack 7 (W Phase)
Average output power [W]	1002.17	1013.2	1079.85
Reference voltage [V]	0.651	0.641	0.669

Table 4. Phase current THD comparison of conventional and proposed neutral-point voltage-shifting control when fourth stack fails.

Unit	Stack 1 (U Phase)	Stack 5 (V Phase)	Stack 7 (W Phase)
Conventional method phase current THD [%]	0.373	0.425	0.373
Proposed method phase current THD [%]	0.331	0.426	0.332

5. Experiment Results

An experiment was performed to verify the feasibility of the proposed control method applied in a cascaded NPC/H-bridge inverter. The configurations of the experimental system and power stacks were as shown in Figures 22–25, and the experimental parameters as in Table 1.

The controller was implemented on TMS320F28377s, and that of the floating point microcontroller unit at 200 MHz rate frequency. The switching and sampling frequency was 10 kHz. The power was supplied to the cascaded NPC/H-bridge inverter through the cascaded NPC/H-bridge converter.

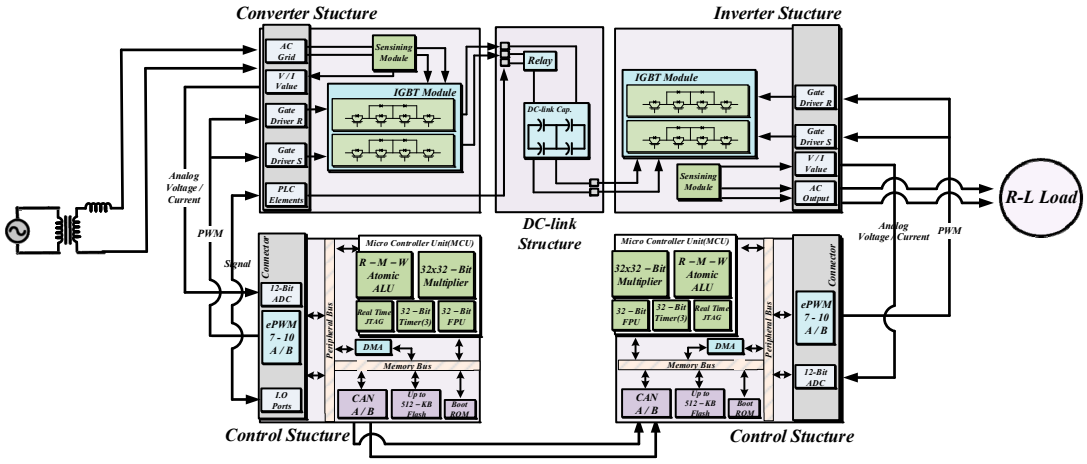

Figure 22. Configuration of the experiment system.

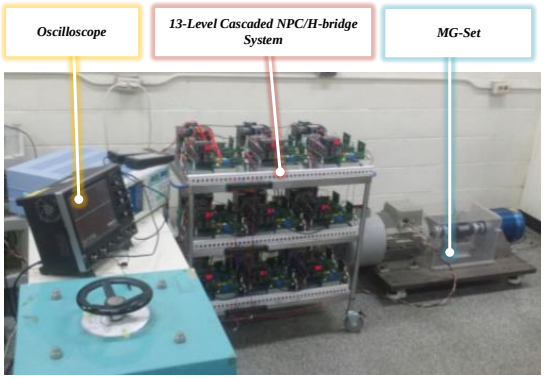

Figure 23. Experimental setup 1 of the 13-level cascaded NPC/H-bridge system.

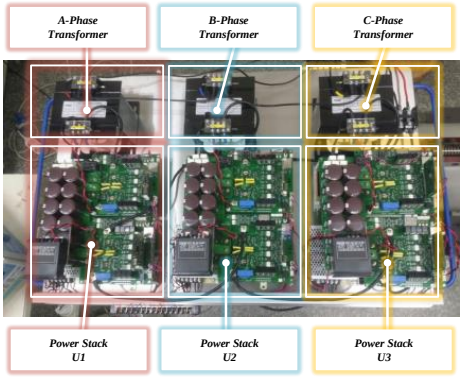

Figure 24. Experimental setup 2 of the 13-level cascaded NPC/H-bridge system.

Figure 26 shows the waveform of the phase voltage of each phase when applying the conventional neutral-point voltage-shifting control. The experiment involves an experimental waveform for the individual phase voltage and fault flags for any faults during inverter operation. Fault is generated in the first stack of the U phase, so that the voltage of the U phase is lowered and the output voltages of the V and W phases are increased.

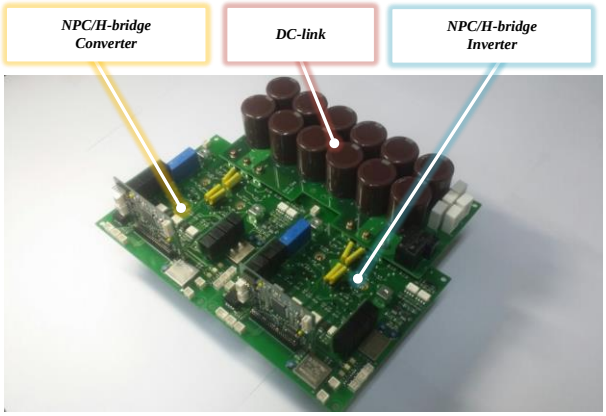

Figure 25. Experimental setup 3 of the one-stack NPC/H-bridge.

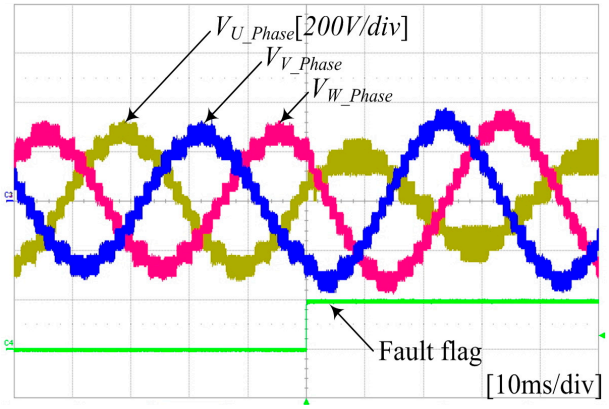

Figure 26. Experimental waveform of phase voltage applying conventional neutral-point voltage-shifting control.

Figure 27 shows the line-to-line voltage and fault flag waveform when using the conventional neutral-point voltage-shifting control. As shown in the figure, the line-to-line voltage waveform shows the characteristics of the three-phase equilibrium even in the fault situation. The phase current on the load side is shown in Figure 28.

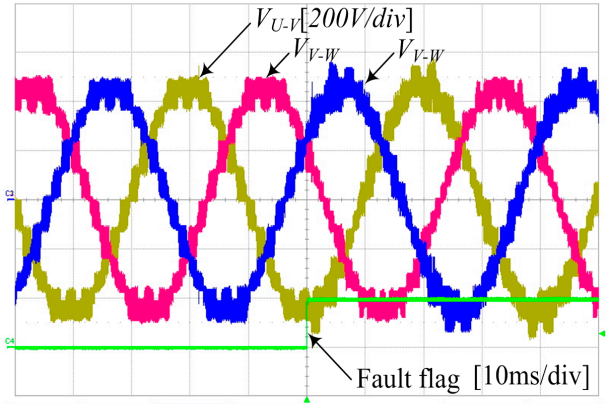

Figure 27. Experimental waveform of line-to-line voltage applying conventional neutral-point voltage-shifting control.

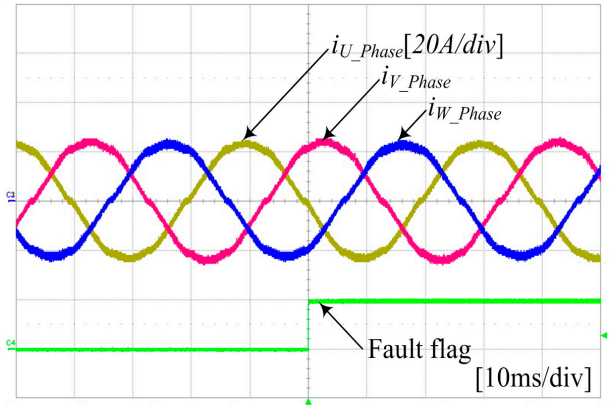

Figure 28. Experimental waveform of phase current applying conventional neutral-point voltage-shifting control.

Even if one stack fails, as shown in Figure 28, the waveform of the phase current also appears as a three-phase equilibrium when three-phase equilibrium of the line-to-line voltage is obtained through the use of the neutral-point voltage-shifting control.

Figure 29 shows the individual stack output power waveform when applying the conventional neutral-point voltage-shifting control. When the first stack of the U phase fails, as shown in Figure 29, the output power of the second stack on the U phase and the output power of the fourth stack on the V phase are different from each other.

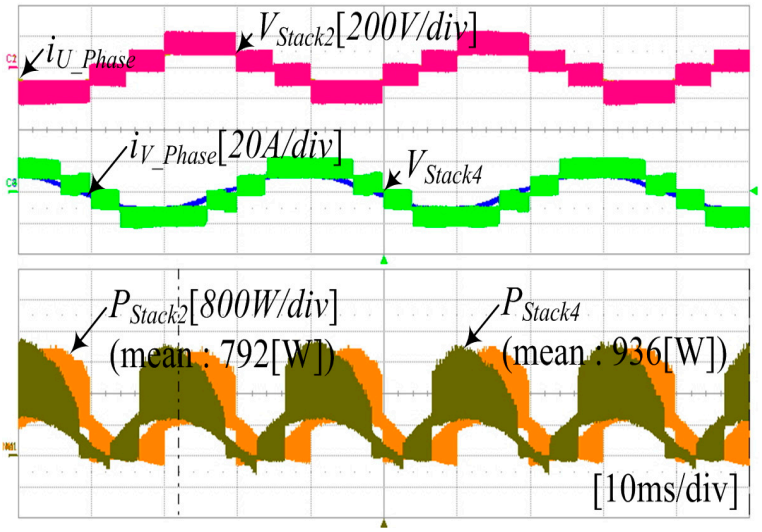

Figure 29. Experimental waveform of output voltage, phase current, and output power of second and fourth stacks applying the conventional neutral-point voltage-shifting control.

As a result, the V phase provides 18.2% more output power than the failed stack. This result is similar to the result of the simulation that output 20.4% more power.

Figure 30 shows the phase voltage and the fault flag waveform when the proposed neutral-point voltage-shifting control is applied. In the case of a fault situation, the proposed control is also applied so as to instantly convert the phase voltage modulation, and thus the neutral-point voltage-shifting control can be seen.

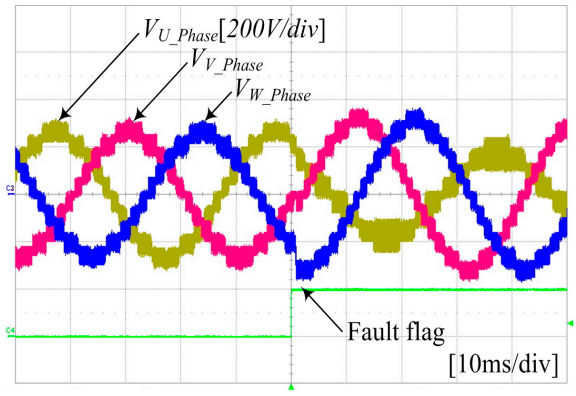

Figure 30. Experimental waveform of phase voltage applying proposed neutral-point voltage-shifting control.

Figure 31 shows the line voltage waveform when using the proposed neutral-point voltage-shifting control. Similar to the conventional neutral-point voltage-shifting control, three-phase equilibrium is established for the line-to-line voltage even in the fault situation. In addition, the line-to-line voltage waveform is similar to the simulation.

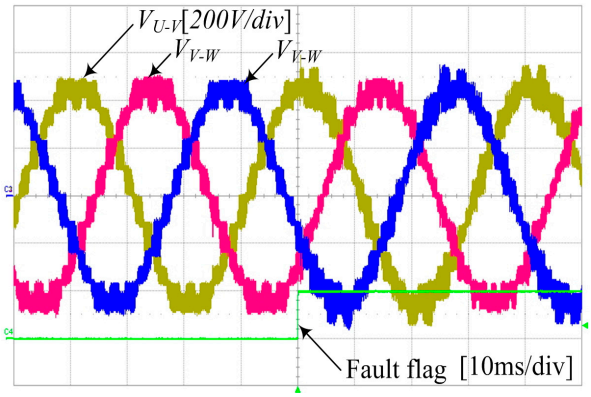

Figure 31. Experimental waveform of line-to-line voltage applying proposed neutral-point voltage-shifting control.

Figure 32 shows the phase current waveform applying the proposed neutral-point voltage-shifting control. In the case of applying the conventional neutral-point voltage-shifting control, the phase current maintains three-phase equilibrium in the same way as shown in Figure 28.

Figure 33 shows the experimental waveforms of the output voltages, phase currents, and output powers of the second and fourth stacks applying the proposed neutral-point voltage-shifting control. When the proposed control is applied, the experimental results show that the output power is only about 5% different from the conventional neutral-point voltage-shifting control. In that way, it is confirmed that the power difference of about 18.7% is reduced to about 7.4% through the simulation, and the power difference of about 16.6% is reduced to about 5.1% by the experiment. Therefore, the effectiveness and feasibility of the proposed neutral-point voltage-shifting control can be verified.

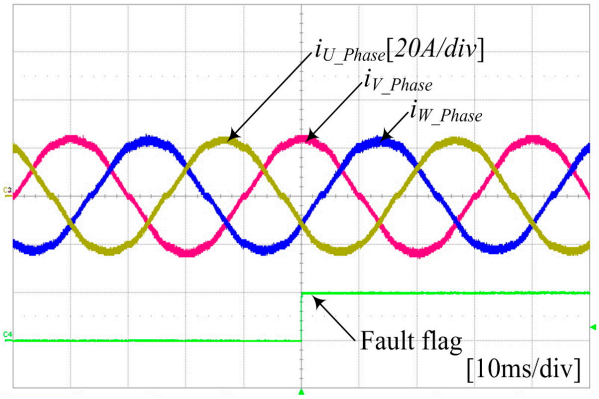

Figure 32. Experimental waveform of phase current applying proposed neutral-point voltage-shifting control.

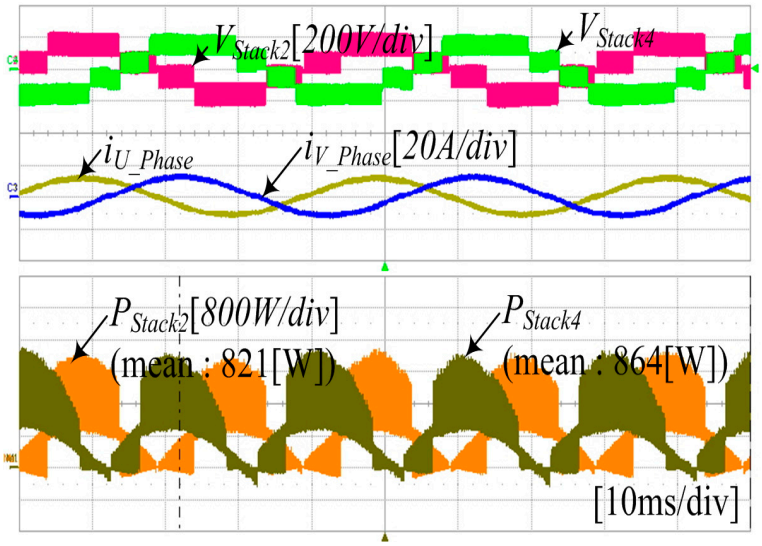

Figure 33. Experimental waveform of output voltages, phase currents, and output powers of the second and fourth stacks applying the proposed neutral-point voltage-shifting control.

6. Conclusions

This paper proposes a novel neutral-point voltage-shifting control that improves the output power imbalance of individual modules caused by conventional neutral-point voltage-shifting control among the fault-tolerant control methods of cascaded NPC/H-bridge inverters. The conventional neutral-point voltage-shifting control caused a power imbalance between stacks as the RMS values of the individual stack reference voltages differed. To improve these imbalances, a control was proposed to perform a selective neutral-point voltage-shifting control according to the area of reference voltage and the limit selection criteria for each stack reference voltage was proposed to be the same as the RMS value.

In this paper, simulation and experiment were performed and presented to verify the proposed neutral-point voltage-shifting control method as well as its feasibility. By applying the proposed control, the power deviation between stacks decreased from about 190 W, which used the conventional control, to about 77 W, and the THD of the phase current also decreased from 0.39 to 0.36.

Given the results, it is expected that the proposed neutral-point voltage-shifting control method is a good candidate for multilevel cascaded NPC/H-bridge inverters.

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