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Structure of All-Digital Frequency Synthesiser for IoT and IoV Applications

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Abstract: In recent years number of Internet of Things (IoT) services and devices is growing and Internet of Vehicles (IoV) technologies are emerging. Multiband transceiver with high performance frequency synthesisers should be used to support a multitude of existing and developing wireless standards. In this paper noise sources of an all-digital frequency synthesiser are discussed through *s*-domain model of frequency synthesisers, and the impact of noise induced by main blocks of synthesisers to the overall phase noise of frequency synthesisers is analysed. Requirements for time to digital converter (TDC), digitally controlled oscillator (DCO) and digital filter suitable for all-digital frequency synthesiser for IoT and IoV applications are defined. The structure of frequency synthesisers, which allows us to meet defined requirements, is presented. Its main parts are 2D Vernier TDC based on gated ring oscillators, which can achieve resolution close to 1 ps; multi core LC-tank DCO, whose tuning range is 4.3–5.4 GHz when two cores are used and phase noise is −116.4 dBc/Hz at 1 MHz offset from 5.44 GHz carrier; digital filter made of proportional and integral gain stages and additional infinite impulse response filter stages. Such a structure allows us to achieve a synthesiser's in-band phase noise lower than −100 dBc/Hz, out-of-band phase noise equal to −134.0 dBc/Hz and allows us to set a synthesiser to type-I or type-II and change its order from first to sixth.

Keywords: CMOS; integrated circuit; frequency synthesiser; time to digital converter; digitally controlled oscillator

1. Introduction

Wireless technologies and services based on these technologies have been spreading rapidly in recent years: coverage of 4G networks increases, 5G technologies are being developed, local area networks are advancing and wireless network at home, workplace and public places is a necessity. The number of Internet of Things (IoT) devices and personal wireless gadgets is rapidly growing. Also, Internet of Vehicles (IoV) and intelligent transport system technologies are emerging. As reports show, wireless standards for IoT and IoV applications, similarly to most of other current and developing wireless standards, are using frequency bands, which are spread from hundreds of megahertzes up to 6 GHz [1–4].

In order to support the multitude of these frequency bands and standards in a single device, integrated circuits (IC) of multiband wireless transceivers are used. Such transceivers are also used in software defined radio, which is becoming more popular in the light of fast developing wireless technologies due to one of its main ideas—the usage of the same hardware for the implementation of different wireless standards, which enables a fast adaptation of the existing equipment to new and developing technologies while reducing the price of the system [3].

One of the main blocks of a multiband transceiver is a high tuning range frequency synthesiser, used as local high frequency signal oscillator. Phase locked loop is usually used as a frequency synthesiser and there are two main classes of phase-locked loops: conventional (charge-pump) phase locked loop and all-digital phase-locked loop.

To save power, chip area and cost, newer integrated circuit manufacturing technologies are being used. But the implementation of the conventional frequency synthesiser, which is analog in most part, in nanometric technologies is becoming more complicated because it is difficult to ensure the parameters of the synthesiser for wireless applications (e.g. operating frequency, frequency tuning range, phase noise level) due to decreasing supply voltage, increasing leakage currents as complementary metal–oxide–semiconductor (CMOS) technology step decreases. Therefore, integrated circuits of all-digital frequency synthesisers are gaining more attention, because these synthesisers, due to their digital nature, don't have the flaws typical of conventional synthesisers.

However, some of the currently most advanced integrated circuits of multiband transceivers are still using conventional frequency synthesisers [5–8] and are implemented in technologies no smaller than 65 nm. New commercial transceivers have been introduced in 28–7 nm technologies [9], but due to the small amount of publicly available technical data, it can only be concluded that they have a limited application scope and have a smaller frequency tuning range, compared to transceivers, which are implemented in more mature technology nodes. This shows that structures of the all-digital frequency synthesiser, their constituting blocks and their models are not sufficiently researched and described. Also, there is a lack of research regarding parameter estimations of all-digital frequency synthesisers and their main blocks, especially for applications in the fields of IoT and IoV.

Therefore, the aim of this work is to present a structure of the all-digital frequency synthesiser for multiband transceiver for IoT and IoV applications that is suitable for implementation in nanometric and submicron technology nodes: the model of *s*-domain all-digital synthesiser is discussed, noise sources of the frequency synthesiser and contribution of main blocks to overall phase noise level of the synthesiser are analysed, requirements for main blocks are defined and a structure of synthesisers, which meets defined requirements, is proposed.

2. Phase Noise in All-Digital Frequency Synthesisers

The main parameter of the frequency synthesiser is phase noise, which describes the spectral purity of an output signal. Therefore, requirements for main blocks of frequency synthesiser will be defined based on phase noise requirements. In this chapter noise sources of all-digital frequency synthesiser will be discussed through the *s*-domain model.

A model of an all-digital frequency synthesiser with included noise sources in the *s*-domain is shown in Figure 1 [10,11]. The main blocks are a phase detector, digitally controlled oscillator (DCO) and filter. The main part of phase detector is a time to digital converter (TDC), which measures time intervals between edges of reference and DCO signals.

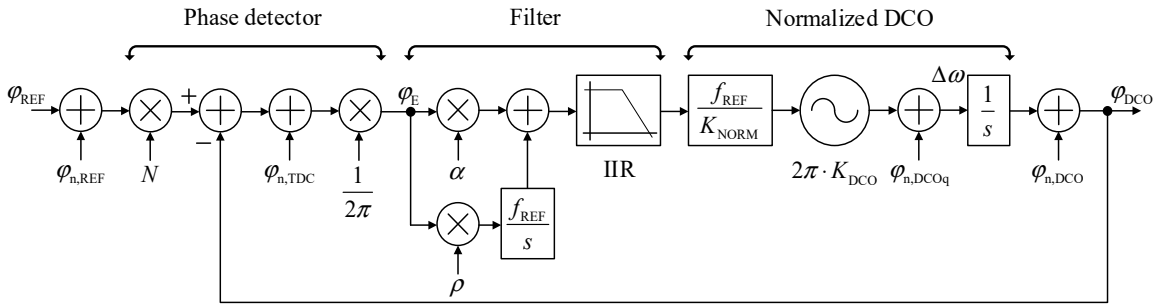


Figure 1. *s*-domain model of a higher order type-II all digital frequency synthesiser with noise sources.

There are two integrators (DCO and integrating path in the filter) and there are additional stages of infinite impulse response (IIR) filters in this model. Therefore, it is a type-II higher order frequency

synthesiser. The main advantage of a type-II structure over type-I is better noise filtering capabilities, but it has worse dynamic characteristics than type-I. Therefore, there should be an ability to change the type of the synthesiser: type-I should be used for fast initial frequency acquisition and type-II is used for precise phase (and frequency) tracking. Type-I structure can be made by eliminating the integrator—setting the filter's proportional gain coefficient ρ to 0.

There are three main phase noise sources: the noise of the reference signal ($\varphi_{\mathrm{n,REF}}$ in Figure 1), TDC ($\varphi_{\mathrm{n,TDC}}$ in Figure 1) and DCO. Noise induced by DCO has two components: quantisation noise ($\varphi_{\mathrm{n,DCOq}}$ in Figure 1) and oscillator's noise ($\varphi_{\mathrm{n,DCO}}$ in Figure 1).

TDC creates quantization noise, which depends on the TDC's resolution t_{res}, DCO's frequency f_{DCO} and the frequency of reference signal f_{REF}. Its single-sided power spectral density is shown in (1) equation [12].

$$\mathcal{L}_{\mathrm{TDC}} = \frac{(2\pi)^2}{12} \cdot \frac{(t_{\mathrm{res}} f_{\mathrm{DCO}})^2}{f_{\mathrm{REF}}}, \tag{1}$$

Spectral density of noise of reference signal and oscillator's component of DCO's noise can be defined by the common equation of oscillator's phase noise [13]:

$$\mathcal{L}_{\mathrm{Osc}}(f) = \frac{k_3}{f^3} + \frac{k_2}{f^2} + \frac{k_1}{f} + k_0, \tag{2}$$

where k_0, k_1, k_2, k_3, k_4 are coefficients, describing the individual oscillator and f—frequency offset from carrier.

Quantization component of noise induced by DCO usually is reduced by using $\Delta\Sigma$ dithering and noise shaping techniques. Single sided power spectral density of DCO's quantisation noise after $\Delta\Sigma$ shaping is [14]:

$$\begin{aligned} \mathcal{L}_{\Delta\Sigma}(f) &= \mathcal{L}_{\mathrm{q}}(f)\big|_{\Delta f_{\mathrm{res}} = \frac{\Delta f_{\mathrm{res}}}{2^{W_{\Delta\Sigma}}}} + \mathcal{L}_{\Delta\Sigma\mathrm{s}}(f)\big|_{\Delta f_{\mathrm{res}} = \Delta f_{\mathrm{res}}} = \\ &= \frac{1}{12} \cdot \left(\frac{\Delta f_{\mathrm{res}} / 2^{W_{\Delta\Sigma}}}{f} \right)^2 \cdot d_{\frac{1}{f_{\mathrm{REF}}}} \cdot \left(\mathrm{sinc} \frac{f}{f_{\mathrm{REF}}} \right)^2 + \\ &+ \frac{1}{12} \cdot \left(\frac{\Delta f_{\mathrm{res}}}{f} \right)^2 \cdot \frac{1}{f_{\Delta\Sigma}} \cdot \left(2 \cdot \sin \frac{\pi f}{f_{\Delta\Sigma}} \right)^{2n}, \end{aligned} \tag{3}$$

here $\mathcal{L}_{\mathrm{q}}(f)$ is the quantization noise component, $\mathcal{L}_{\Delta\Sigma\mathrm{s}}(f)$ is the $\Delta\Sigma$ noise shaping component, Δf_{RES}—the tuning step of DCO's frequency, f_{REF}—frequency of reference signal, $f_{\Delta\Sigma}$—frequency of $\Delta\Sigma$ dithering, f—frequency offset from carrier, $W_{\Delta\Sigma}$—bit count of $\Delta\Sigma$ modulator, and n—order of $\Delta\Sigma$ modulator.

As is seen from Equations (1) and (3), the quantization noise of TDC and DCO decreases with increased reference frequency and $\Delta\Sigma$ dithering frequency (in case of DCO). But increasing these frequencies will also increase power consumption of the system, which is undesirable in IoT and IoV applications. Therefore, there is present a classical task of searching for compromise between quantization noise and power consumption.

Total frequency synthesiser's phase noise can be defined as [11]:

$$\mathcal{L}_{\mathrm{FS}} = \mathcal{L}_{\mathrm{Osc,REF}}(f) \cdot |H_{\mathrm{cl,REF}}(f)|^2 + \mathcal{L}_{\mathrm{TDC}} \cdot |H_{\mathrm{cl,TDC}}(f)|^2 + \mathcal{L}_{\mathrm{Osc,DCO}}(f) \cdot |H_{\mathrm{cl,DCO}}(f)|^2 + \mathcal{L}_{\Delta\Sigma}(f), \tag{4}$$

where $H_{\mathrm{cl,REF}}$, $H_{\mathrm{cl,TDC}}$, $H_{\mathrm{cl,DCO}}$, are respectively closed-loop transfer functions of reference signal noise, TDC quantization noise and oscillator's component of DCO noise, whose s-domain representations are shown in Equations (5)–(7) [15]. Expression of $\Delta\Sigma$ quantization noise, shown in Equation (3) takes into account its noise transfer function, therefore it is not multiplied by the power transfer function in Equation (4).

$$H_{\mathrm{cl,REF}}(s) = N \frac{H_{\mathrm{ol}}(s)}{1 + H_{\mathrm{ol}}(s)}, \tag{5}$$

$$H_{\mathrm{cl,DCO}}(s) = \frac{1}{1 + H_{\mathrm{ol}}(s)}, \tag{6}$$

$$H_{\mathrm{cl,TDC}}(s) = \frac{H_{\mathrm{ol}}(s)}{1 + H_{\mathrm{ol}}(s)}. \tag{7}$$

H_{ol} in Equations (5)–(7) are open loop transfer functions of the type-II higher order frequency synthesiser. If four additional IIR filters are used in the structure of the synthesiser, it is defined by Equation (8).

$$H_{\mathrm{ol}}(s) = \frac{\rho f_{\mathrm{REF}}^2}{s} \cdot \frac{1 + s/(\rho f_{\mathrm{REF}}/\alpha)}{s} \cdot \prod_{i=0}^{3} \frac{1 + s/f_{REF}}{1 + s/\lambda_i f_{REF}}, \tag{8}$$

here α and ρ are respectively proportional and integral gain of the synthesiser's filter and λ_{i} is the transfer coefficient of each IIR filter stage.

Transition from s-domain to linear frequency can be made by using $s = j2\pi f$ substitution.

3. Requirements for Blocks of All-Digital Multiband Frequency Synthesiser

In order to evaluate the impact of main blocks on noise performance of the frequency synthesiser, the total phase noise of the synthesiser will be calculated by using (4) equation.

Calculation results of phase noise and its components of type-II frequency synthesiser are shown in Figure 2. Total phase noise of frequency synthesiser is marked as $\mathcal{L}_{\mathrm{FS}}(f)$, phase noise induced by reference signal is marked as $\mathcal{L}_{\mathrm{REF}}(f)$, phase noise induced by TDC is marked as $\mathcal{L}_{\mathrm{TDC}}(f)$, the oscillator's component of DCO's phase noise is marked as $\mathcal{L}_{\mathrm{DCO}}(f)$, DCO's quantization and $\Delta\Sigma$ shaping noise is marked as $\mathcal{L}_{\mathrm{DCO}\Delta\Sigma}(f)$. Parameters provided in references [16,17] were used to carry out these calculations: the operating frequency of the DCO is equal to 5.38 GHz, the frequency of the reference signal is 48 MHz, the frequency tuning step is 26 kHz, the $\Delta\Sigma$ modulator controls 9 bits. The $\Delta\Sigma$ dithering frequency and order of $\Delta\Sigma$ modulator are not provided, therefore we assume that the $\Delta\Sigma$ dithering frequency is equal to the DCO's frequency divided by 4, and the order of the $\Delta\Sigma$ modulator is 2nd. Phase noise of the reference signal and oscillator's component of DCO's noise are approximated respectively by Equations (9) and (10).

$$\mathcal{L}_{\mathrm{Osc,REF}}(f) = \frac{10^{-4.8}}{f^3} + \frac{10^{-8.3}}{f^2} + \frac{10^{-10.3}}{f} + 10^{-14.7}, \tag{9}$$

$$\mathcal{L}_{\mathrm{Osc,DCO}}(f) = \frac{10^{-0.2}}{f^2} + 10^{-13.8}. \tag{10}$$

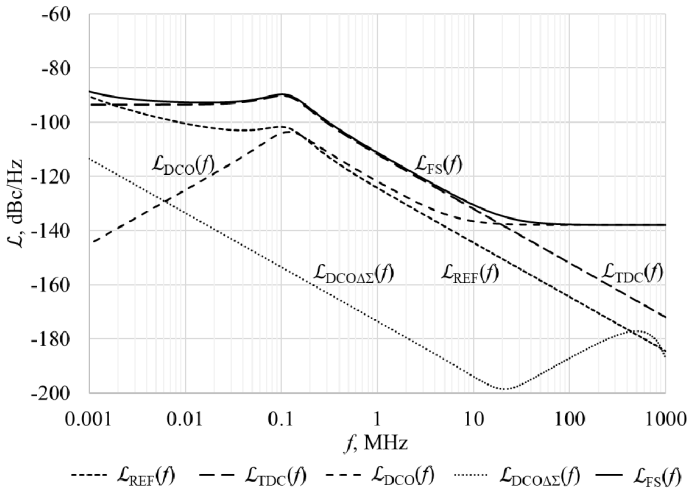
Configuration of the filter is not provided in reference [16], therefore two configurations of the filter were considered. First configuration is made of only proportional and integral parts, with proportional and integral coefficients respectively set to $\alpha = 2^{-6}$ and $\rho = 2^{-12}$. This corresponds to the filter's configuration for a type-II frequency synthesiser. Results of calculations for this configuration are shown in Figure 2a. For the second configuration it is assumed that the filter is composed of proportional and integral gain paths and four first-order stages of IIR filter. Such configuration corresponds to filter's structure for the type-II higher order frequency synthesiser. Coefficients of proportional and integral paths are set respectively to $\alpha = 2^{-6}$ and $\rho = 2^{-10}$. Transfer coefficients of all stages of IIR filters are equal and set to $\lambda_1 = \lambda_2 = \lambda_3 = \lambda_4 = 2^{-5}$. Results of calculations for the second configuration of the filter is shown in Figure 2b.

It is seen from both cases shown in Figure 2 that noise induced by TDC dominates at low frequency offsets from the carrier (in-band) and noise induced by DCO dominates at high frequency offsets from the carrier (out-of-band). Also, it is seen that the higher order synthesiser's filter enables more precise control of the synthesiser's passband and has better noise-filtering capabilities: in the case of the first configuration (Figure 2a), noise induced by TDC has a high impact on total phase noise up to 10 MHz frequency offset, while in the second configuration (Figure 2b), noise of reference signal and noise of

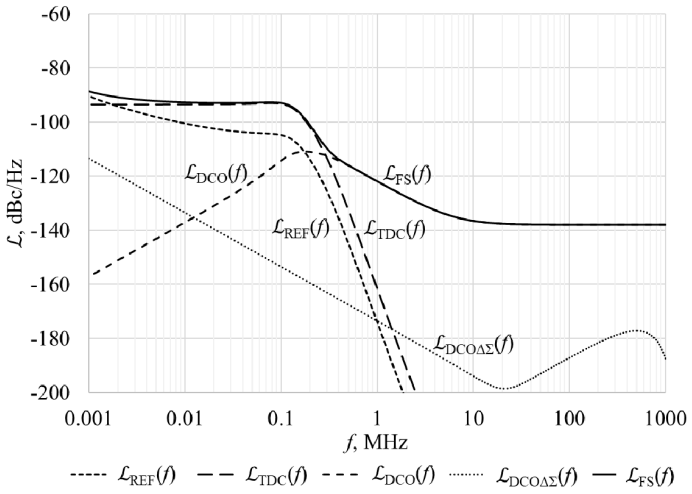
TDC is highly attenuated outside of the synthesiser's passband and DCO's noise clearly dominates out-of-band. Therefore, it is important to have a reprogrammable filter, to control the synthesiser's frequency response and noise filtering capabilities.

Since noise induced by TDC and DCO's noise have separate dominance ranges, the requirements of phase noise performance for the frequency synthesiser can be transformed to the requirements for TDC and DCO.

As mentioned in the first chapter, reports and analysis of current and developing standards, which are used for IoT, IoV and other wireless applications, use frequency bands from hundreds of megahertz up to 6 GHz. Also, from the technical documentation of some of most the advanced multiband transceivers presently available [5–8], it is seen that in-band phase noise should be better than −90 dBc/Hz and out-of-band phase noise should be better than −120 dBc/Hz.



(**a**)



(**b**)

Figure 2. Calculated phase noise and its components of an all digital frequency synthesiser, when f_{DCO} = 5.38 GHz, f_{REF} = 48 MHz, $f_{\Delta\Sigma} = f_{DCO}/4$, Δf_{RES} = 26 kHz, W = 9, n = 2 with two filter configurations: (**a**) $\alpha = 2^{-6}$, $\rho = 2^{-12}$; (**b**) $\alpha = 2^{-6}$, $\rho = 2^{-10}$, $\lambda_1 = \lambda_2 = \lambda_3 = \lambda_4 = 2^{-5}$.

From Equation (1) it is seen that noise induced by TDC depends on the resolution of TDC, operating frequency of DCO and frequency of the reference signal. It deteriorates with a higher frequency of DCO, therefore, for theoretical calculations, the highest needed frequency should be used,

i.e., 6 GHz. Calculated noise, induced by TDC, when frequency of digitally controlled oscillator is 6 GHz, frequency of reference signal ranges from 10 MHz to 100 MHz and resolution of TDC ranges from 2 ps to 50 ps is shown in Figure 3. As can be seen, the resolution of TDC has to be better than 12 ps to satisfy the in-band noise requirement of −90 dBc/Hz. If resolution of TDC is 4 ps, a better than −100 dBc/Hz in-band noise can be achieved.

Oscillator's component of the DCO's noise depends on properties of the resonant tank. Usually LC tank oscillators are used to achieve low phase noise. LC tank DCOs and the oscillator's component of DCO noise are widely researched and discussed [18–20], therefore, here the focus will be on the quantization component of DCO noise.

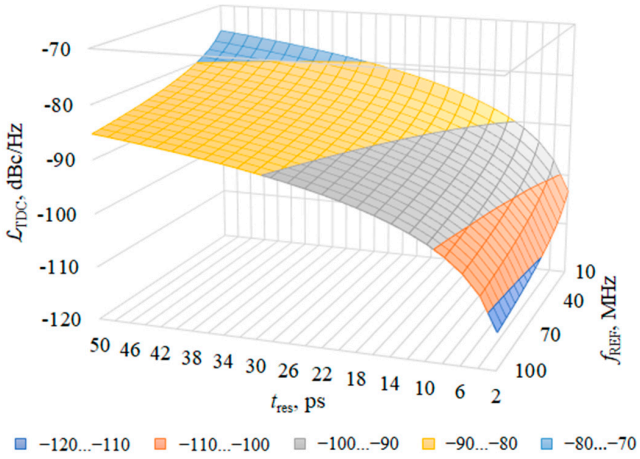


Figure 3. Calculated phase noise induced by time to digital converter, when frequency of digitally controlled oscillator's output signal is 6 GHz, frequency of reference signal is 10–100 MHz, resolution of time to digital converter is 2–50 ps.

Figure 4 shows DCO's quantization and ΔΣ shaping noise and its components, which are calculated by using Equation (3). The following parameters were used: DCO's frequency f_{DCO} is equal to 6 GHz, frequency of reference signal f_{REF} is 40 MHz, ΔΣ dithering frequency $f_{\Delta\Sigma}$ is equal to divided-by-4 DCO's frequency, DCO's frequency tuning step Δf_{RES} is 50 kHz, ΔΣ modulator controls 8 bits and order of ΔΣ modulator is 3. Total DCO's quantization and ΔΣ shaping noise is marked as $\mathcal{L}_{\Delta\Sigma}(f)$, DCO's quantization noise without ΔΣ modulator is marked as $\mathcal{L}_{q}(f)$, DCO's quantization noise with ΔΣ modulator is marked as $\mathcal{L}_{\Delta\Sigma q}(f)$, and ΔΣ noise shaping component is marked as $\mathcal{L}_{\Delta\Sigma s}(f)$.

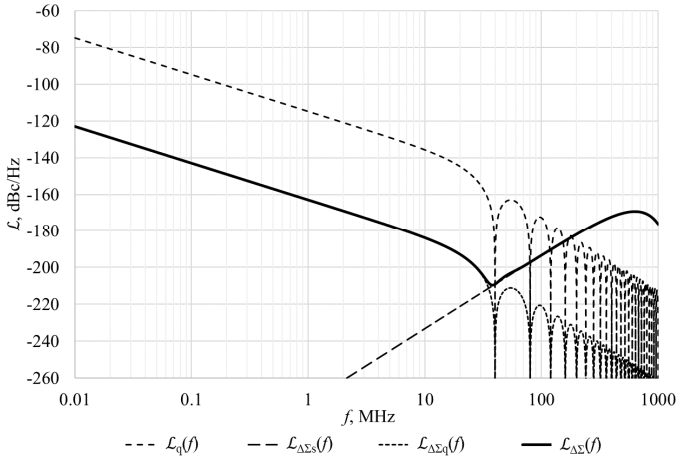


Figure 4. Calculated phase noise and its components, induced by quantization of digitally controlled oscillator, when f_{DCO} = 6 GHz, f_{REF} = 40 MHz, $f_{\Delta\Sigma} = f_{DCO}/4$, Δf_{RES} = 40 kHz, W = 8, n = 3.

It can be seen from Figure 4 that ΔΣ quantization and noise shaping improves DCO's quantization noise by more than 40 dBc/Hz at small frequency offsets from the carrier (in-band). In this range, according to Equation (3), noise depends on the frequency of the reference signal and $\Delta f_{RES}/2^W$ ratio. This ratio shows that increasing the ΔΣ modulator's bit count by one bit corresponds to reduction of frequency tuning step by half. In-band DCO's quantization noise will not be filtered by the synthesiser, therefore it should not exceed the noise induced by TDC. In order for DCO's quantization noise to not exceed −100 dBc/Hz, when frequency of reference signal is 40 MHz, ratio of $\Delta f_{RES}/2^W$ should not exceed 2190 Hz, i.e., equivalent frequency tuning step after ΔΣ quantization should not exceed this value. Such a case, when the raw frequency tuning step (without ΔΣ dithering) is increased to 560.64 kHz and all other parameters are the same as in previous case, is shown in Figure 5. But it should be noted, that even in sub-micron technologies, a frequency tuning step close to 10 kHz is achievable [14,21–23]. Therefore, the requirement of $\Delta f_{RES}/2^W$ ratio is relatively easy to meet.

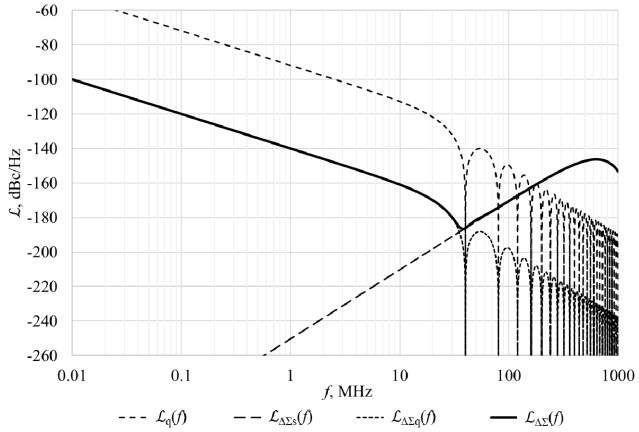


Figure 5. Calculated phase noise and its components, induced by quantization of digitally controlled oscillator, when f_{DCO} = 6 GHz, f_{REF} = 40 MHz, $f_{\Delta\Sigma} = f_{DCO}/4$, Δf_{RES} = 560.64 kHz, W = 8, n = 3.

ΔΣ shaping noise dominates at high frequency offset from the carrier (out-of-band). This noise component increases when the frequency of DCO's output signal decreases, because being together decreases ΔΣ dithering frequency. The case of ΔΣ quantization and shaping noise, when frequency of the DCO signal is decreased to 1 GHz and all other parameters are the same as in first case (shown in Figure 4) is shown in Figure 6. In this case the maximum of ΔΣ shaping noise increased by 23 dB/Hz and this maximum moved towards lower frequency offsets, but it is still out of frequency synthesiser's passband. This noise component has to be lower than the oscillator's component of DCO's noise.

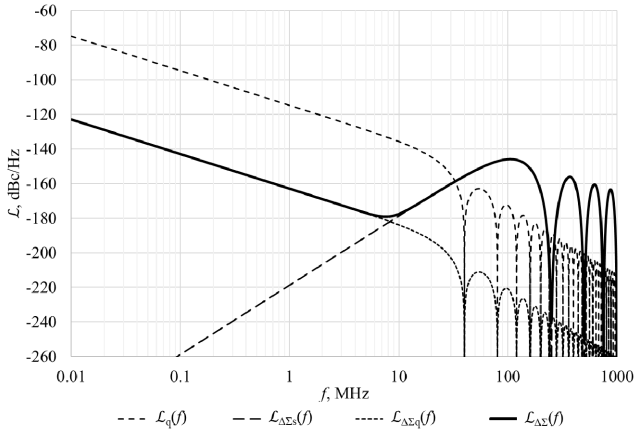


Figure 6. Calculated phase noise and its components, induced by quantization of digitally controlled oscillator, when f_{DCO} = 1 GHz, f_{REF} = 40 MHz, $f_{\Delta\Sigma} = f_{DCO}/4$, Δf_{RES} = 40 kHz, W = 8, n = 3.

Another property of DCO for multiband frequency synthesiser for IoT and IoV applications, besides phase noise performance, is the tuning range. As mentioned above, the frequency of synthesisers output signal has to range from hundreds of megahertzes up to 6 GHz. But frequency of the DCO does not have to be tuneable in whole range—frequency range can be extended by using frequency dividers, such as in reference [24]. Therefore, we will assume that for multiband applications, the tuning range of DCO has to be at least 1 GHz.

According to the discussion in this and previous chapters, requirements for main blocks of an all-digital multiband frequency synthesiser for IoT and IoV applications can be defined:

- the resolution of TDC must be better than 12 ps to ensure a phase noise of less than −90 dBc/Hz when frequency of DCO's signal is 6 GHz;
- the out-of-band phase noise of frequency synthesiser is dominated by noise induced by DCO, therefore its phase noise in this region has to be less than −120 dBc/Hz;
- total DCO's quantization and ΔΣ shaping noise has to be lower than noise induced by TDC in synthesiser's passband and oscillator's component of DCO's noise;
- the frequency tuning range of the DCO has to be wide (at least 1 GHz);
- the digital synthesiser's filter should consist of a proportional and integral gain parts and additional IIR filters in order to change the type and order of the frequency synthesiser and be able to precisely control the bandwidth of the synthesiser.

4. All-Digital Frequency Synthesiser for Multiband Transceivers

The structure of all-digital synthesiser for the multiband wireless transceiver, which meets the requirements defined in the previous chapter, is suitable for IoV and IoT applications shown in Figure 7. This structure is based on structure which is presented in reference [25], but is modified for a wide tuning range of output signal and ensures high resolution of TDC.

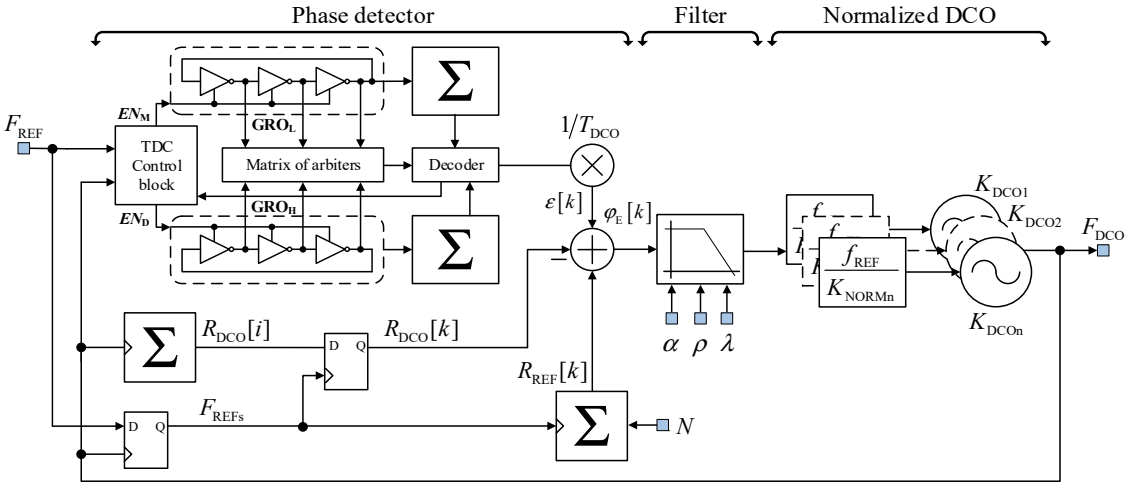


Figure 7. Phase domain model of all digital frequency synthesiser for multiband transceiver.

Wide tuning range is achieved by using multicore DCO. In this structure it is shown as multiple parallel-connected DCOs, because in the general case, there can be n DCO cores used in synthesisers, but simultaneously only one core is operating. Each core has its own normalisation coefficient K_{DCOn}, therefore, general DCO's normalisation coefficient is a set of coefficients of each core $K_{DCO} = \{K_{DCO1}, K_{DCO2}, ..., K_{DCOn}\}$. Each core is normalised individually, therefore there are n normalisation blocks. The purpose of normalisation is to eliminate the transfer coefficient of the DCO (K_{DCO}) and make a tuning of DCO linear—if transfer coefficient of the DCO is estimated correctly (i.e., normalisation transfer coefficient K_{NORM} is equal to K_{DCO} and ratio $K_{DCO}/K_{NORM} = 1$), due to normalisation, change of one bit of integer oscillator tuning word (LSB) changes the output frequency of DCO by f_{REF} hertz.

Physical implementation of multicore DCO in 0.18 µm CMOS technology is presented in our previous work [26] and shown in Figure 8. It made of two LC tank DCO cores, decoupling stage, differential to single ended converter, tri-state buffers and frequency divider. It is a partial case of a multicore oscillator, where two DCO cores are used, but this structure is scalable to use different a number of cores to satisfy operating frequency and tuning range requirements. However, the penalty of adding more cores is a rapidly increasing area of silicon.

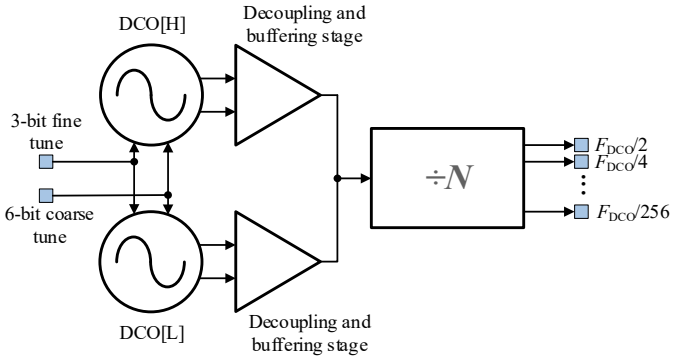


Figure 8. Structure of 5 GHz LC digitally controlled oscillator.

Both cores of LC DCO have the same configuration. Main components of the DCO are a high-quality factor inductor, negative impedance cross-coupled transistor pair and two switched-capacitor arrays. Frequency of DCO is tuned by using 6-bit coarse tuning and 3-bit fine tuning binary words. Together with DCO frequency divider it is used to increase available frequency values. A divider is made of eight divide-by-2 cells connected in a daisy chain, thus division values range from 2 to 256.

In this partial case 4.3–5.4 GHz frequency tuning range of DCO is achieved. When the highest operating frequency is set, phase noise at output of DCO is -116.4 dBc/Hz at 1 MHz offset from 5.44 GHz carrier and -134.0 dBc/Hz at 10 MHz offset from 5.44 GHz carrier. When working at the lowest frequency, phase noise at output of DCO is -117.6 dBc/Hz at 1 MHz offset from 4.3 GHz carrier and -138.0 dBc/Hz at 10 MHz offset from 5.44 GHz carrier.

Oscillator's component of this DCO's phase noise can be approximated by following equation:

$$\mathcal{L}_{\mathrm{Osc,DCO}}(f) = \frac{10^{5.07}}{f^3} + \frac{10^{-0.29}}{f^2} + \frac{10^{-6.7}}{f} + 10^{-16}. \tag{11}$$

Without tuning nonlinearity, mentioned above and alleviated by normalisation of DCO, there are capacitance mismatches in tuning banks, common to all DCOs. Ideally, all unit-weighted capacitors have same capacitance values. But in reality, these values will vary. If the synthesiser is in frequency tracking mode, these capacitors will be constantly switching on/off and due to variation of capacitance, output frequency will also vary—it will be slightly different from expected frequency and will degrade phase noise performance. One of the basic techniques to alleviate such mismatches is dynamic element matching (DEM) [14,15]. The main idea of DEM is to dynamically rearrange (e.g. cyclically shift within switched-capacitor bank) unit-weighted mismatched components, so that averaged in time equivalent values of these components would be equal.

From the discussion in chapters 2 and 3 it is seen that quantisation noise of the TDC depends on delay of the inverter. Actually, delay of the inverter is equal to the resolution of the commonly used TDC, which is based on the inverter delay line. This delay can be reduced by increasing its driving strength, together with increasing its power consumption. Table 1 shows modelling results of inverter's delay (τ_{inv}) in 65 nm CMOS technology at different load capacitance (C_{L}) and ratio of width and length (W_{n}/L) of used transistors. Length of all transistors was set to the minimum value in

current technology (60 nm) and width of NMOS transistors (W_n) was set to 4, 8 and 16 µm. Width of PMOS transistor is always set to double of NMOS, i.e., $W_p = 2W_n$.

Table 1. Modeling results of dependency of inverter's delay time on load capacitance and ratio of width and length of transistors in 65 nm CMOS technology.

C_L, fF	τ_{inv}, ps		
	W_n/L = 66.67	W_n/L = 133.33	W_n/L = 266.67
10	10.49	8.97	8.28
20	12.94	10.26	8.90
30	15.33	11.49	9.59
40	17.69	12.72	10.22
50	20.04	13.91	10.82
60	22.37	15.13	11.46
70	24.63	16.33	12.10
80	26.79	17.50	12.71
90	28.84	18.68	13.30
100	30.76	19.85	13.88

It is seen from Table 1 that even when greatly increasing the driving strength of an inverter, it remains challenging to achieve lower than 12 ps delay of an inverter. It is obvious that other negative results of such an approach are a rapidly increasing used area of silicon. Therefore, the more advanced structure of TDC should be used.

High resolution of TDC is achieved by using 2D Vernier TDC based on gated ring oscillators, which was presented in our previous works [27,28] and shown in Figure 9a. Such TDC allows us to measure the time interval, which is lower than delay of the inverter. Main blocks of this TDCs are two gated ring oscillators, which are used as infinite delay lines, lap and edge counters of both oscillators, matrix of arbiters, control block and output decoder. The resolution of such TDC is defined as difference of delay of stages from which two oscillators are made. To have the ability to control the resolution of TDC, stage delay of oscillator (and its corresponding oscillation frequency) should also be controllable. For this reason, each oscillator is made of parallel-connected oscillator sections, as shown in Figure 9b. Stage delay is decreasing when additional sections of the oscillator are enabled.

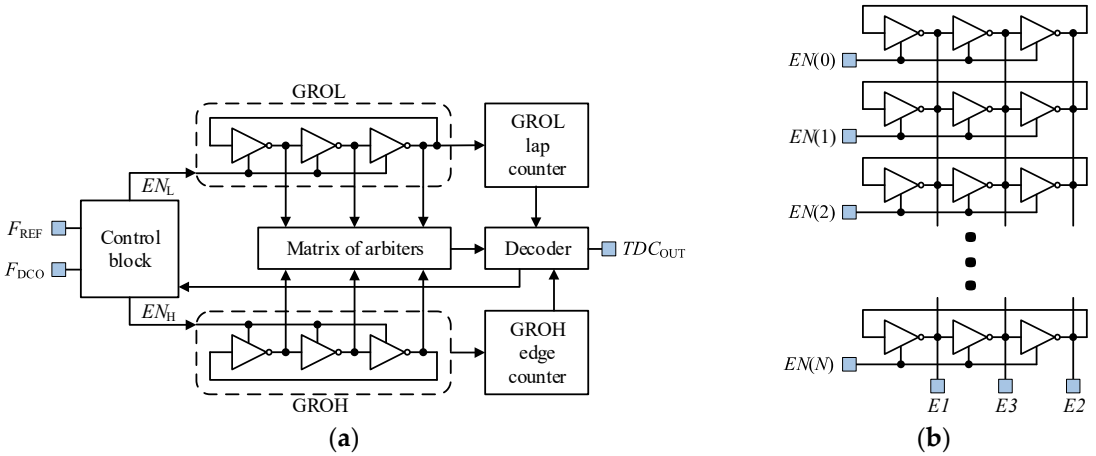


Figure 9. (**a**) Structure of proposed 2D Vernier time to digital converter based on gated ring oscillators. GROL—lower frequency oscillator, GROH—higher frequency oscillator; (**b**) Structure of gated ring oscillators used in TDC.

At the beginning of the measurement, TDC is waiting for the rising edge of the reference signal. When it is received, the lower frequency gated ring oscillator and its lap counter are started. After that

TDC is waiting for the rising edge of the DCO signal. When it is received, the state of lower frequency oscillator is saved, and the higher frequency oscillator and its edge counter are started. When both oscillators are started, the output signals of arbiters are monitored. When the output of any arbiter changes to a high level, it means that the higher frequency oscillator has caught up with the lower frequency oscillator. The position of that arbiter is located and depending on that position, the output signal of TDC is decoded. After that, all counters are reset and the TDC waits for another pair of the input signals for a new measurement.

As shown in reference [28], a TDC employing such a structure can be synthesised in various technology nodes. It was implemented in 65 nm and 0.13 µm CMOS technologies and resolutions close to 1 ps can be achieved in both technologies, which exceeds our requirements by 12 times. However, to achieve resolutions close to 1 ps, more stages of the gated ring oscillator should be turned on, which increases power consumption. Therefore, high resolution should be used only when it is needed.

Similar mismatches to those in the DCO's tuning banks occur in the synthesised ring oscillators which are used in TDC. All delay cells (tri-state inverters), which are used to compose ring oscillators, are the same. However, due to their irregular location and wiring after automatic place and route, these cells have different effective driving strengths, which results in different stage delays.

However, despite the mismatch in stage delay, ring oscillator periods, which are utilized in calculations of the TDC's output, are consistent during measurement. Also, the resolution of such TDC depends on the difference between stage-delay of higher and lower frequency oscillators and not on absolute value of stage delay (delay mismatch usually is much lower than stage-delay). Therefore, this structure is less susceptible to delay mismatch compared to TDC based on delay lines.

Although these mismatches in TDC stage delay are generally undesirable, they can be used to fine tune resolution of TDC based on ring oscillators. A TDC calibration technique which takes advantage of the place and route irregularity is presented in reference [29]. This mechanism sorts used delay elements by driving strength and uses this information to achieve a different oscillation frequency (and corresponding stage delay) with same number of enabled sections of ring oscillators, i.e., same number of the parallel-connected sections will result in a different stage delay, depending on the position in chip layout of the sections.

As mentioned earlier, the filter of frequency synthesiser has the important role of controlling the synthesiser's dynamic characteristics and noise filtering. However, it gets little attention in publications related to frequency synthesisers [30–32]. Often it is only stated that there is a filter in the structure, without further elaboration. Filters, suitable for IoT and IoV applications in multiband frequency synthesisers can be based on structure from references [33,34]. Its main proportional-integral part is shown in Figure 10. Additional cascaded IIR filter stages can be used to form a higher order filter.

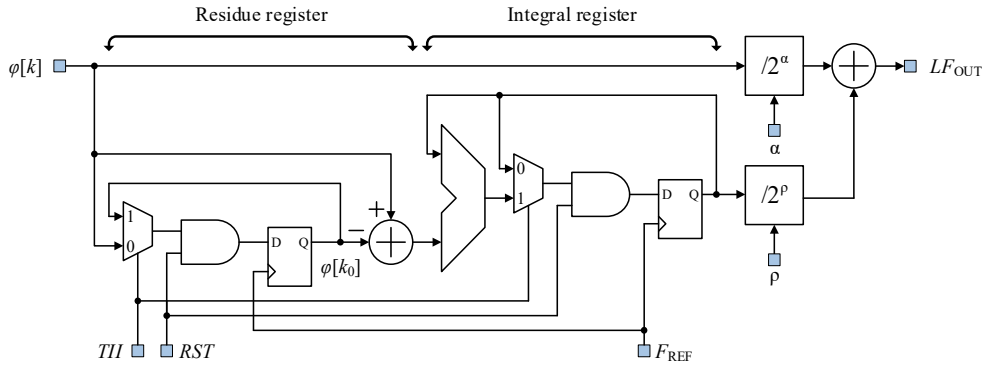


Figure 10. Structure of filter for type-II frequency synthesiser.

Proportional and integral paths can be reconfigured by changing their gain coefficients, respectively α and ρ. Gain stages are implemented as right-shift registers. The type of synthesiser (from type-I to type-II and vice versa) that is controlled by signal *TII*—integral paths activates only

when it is set to a high logic level. If four additional IIR filter stages are used, such a filter enables changing the synthesiser order from first to sixth.

The most power-hungry blocks in a proposed structure of frequency synthesiser are DCO and TDC. Power consumption of the presented DCO core is 18 mW, while the power consumption of TDC is 3,6 mW. All other circuitry is low-power and operates at a relatively low reference frequency. Therefore, we will estimate 50% of sum of DCO and TDC power consumption i.e., 10.8 mW. Total power consumption is 32.4 mW.

Calculated achievable phase noise and its components of all digital frequency synthesiser, when presented time to digital converter and digitally controlled oscillator are used is shown in Figure 11. The maximal frequency of designed DCO, which is equal to 5.44 GHz, was used for calculations. Also, it is assumed that frequency tuning step is 50 kHz, frequency of reference signal is 40 MHz, ΔΣ dithering frequency is equal to divided-by-4 DCO's frequency, ΔΣ modulator controls 8 bits and order of ΔΣ modulator is 2. Also, the resolution of TDC is set to 4 ps and filter's coefficients are $\alpha = 2^{-7}$, $\rho = 2^{-10}$, $\lambda_0 = \lambda_1 = \lambda_2 = \lambda_3 = 2^{-5}$.

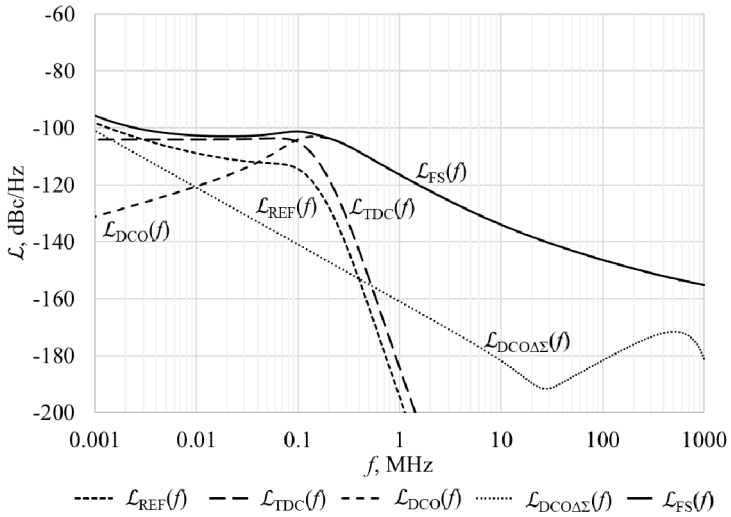


Figure 11. Calculated achievable phase noise and its components of frequency synthesiser, when presented time to digital converter, digitally controlled oscillator and synthesiser's filter are used.

Noise of reference signal was approximated by following equation, derived from data of crystal oscillator [35]:

$$\mathcal{L}_{\mathrm{Osc,REF}}(f) = \frac{10^{-6.72}}{f^3} + \frac{10^{-8.52}}{f^2} + \frac{10^{-11.33}}{f} + 10^{-15.71}. \quad (12)$$

It is seen from Figure 11 that the synthesiser's in-band phase noise is lower than −100 dBc/Hz. Out-of-band phase noise corresponds to the oscillator's component of the DCO's phase noise and is equal to −116.4 dBc/Hz and −134.0 dBc/Hz respectively at 1 MHz and 10 MHz offset from 5.44 GHz carrier. Out-of-band ΔΣ dithering noise is about 20 dBc/Hz lower than the DCO's noise. As can be seen, the presented blocks of the synthesiser meet the defined requirements.

Comparison of calculated parameters of frequency synthesisers to other works is shown in Table 2. Here F_{min}, F_{max}—maximum and minimum operating frequency, F_{off}, F_{c}—frequency offset and carrier frequency at which phase noise is provided, $\mathcal{L}\{F_{\mathrm{off}}\}$—phase noise, P—power consumption.

Table 2. Comparison of calculated parameters of frequency synthesisers to other works.

Reference	Technology	F_{min}, GHz	F_{max}, GHz	F_{off}, MHz	F_c, GHz	$\mathcal{L}\{F_{off}\}$, dBc/Hz	P, mW
[36]	28 nm	1.48	2.13	1	2.09	−108.0	11.6
[37]	40 nm	0.10	3.00	1	1.00	−94.0	9.1
[16]	65 nm	4.90	6.90	1	5.37	−114.2	22.0
[38]	65 nm	4.70	6.10	1	3.87	−114.9	42.6
[39]	65 nm	2.80	3.50	1	3.50	−126.0	15.6
[40]	90 nm	39.13	42.21	1 10	40.00	−83.9 −103.9	46.0
[41]	0.13 µm	2.10	3.50	1	2.40	−102.5	12.0
This Work	65 nm–0.18 µm	4.30	5.44	1 10	5.44	−116.4 −134.0	32.4

5. Conclusions

There are three main phase noise sources in all-digital frequency synthesisers: noise of reference signal, TDC and DCO. Noise induced by DCO has two components: quantisation noise and oscillator's noise.

Noise induced by TDC and DCO's noise have separate dominance ranges—noise induced by TDC dominates at low frequency offsets from the carrier (in-band) and noise induced by DCO dominates at high frequency offsets from the carrier (out-of-band). Therefore, requirements of phase noise performance for frequency synthesisers can be transformed into the requirements for TDC and DCO.

The structure of the all-digital frequency synthesiser for wireless transceivers for IoT and IoV applications, suitable for implementation in nanometric and submicron CMOS technologies, has to be made of TDC whose resolution has to be lower than 12 ps to ensure a lower than −90 dBc/Hz in-band phase noise when the frequency of the DCO's signal is 6 GHz; DCO whose frequency tuning range is at least 1 GHz and its out-of-band phase noise is lower than −120 dBc/Hz; and digital filter which enables to change the type and order of frequency synthesiser to be able to precisely control the bandwidth of the synthesiser.

A wide tuning range is achieved by using multicore DCO, which is made of multiple LC tank DCO cores, decoupling stages, differential to single ended converter, tri-state buffers and frequency dividers. Such a structure is scalable and different number of cores can be used to satisfy operating frequency and tuning range requirements. However, the penalty of adding more cores is a rapidly increasing area of silicon. With partial case in 0.18 µm CMOS technology, when only two DCO cores are used, the tuning range is 4.3–5.4 GHz and the phase noise is −116.4 dBc/Hz and −134 dBc/Hz at respectively 1 MHz and 10 MHz offset from the 5.44 GHz carrier.

High resolution of TDC is achieved by using 2D Vernier TDC based on gated ring oscillators, which can measure time interval, with a lower delay than inverters. The main blocks of this TDCs are two gated ring oscillators, which are used as infinite delay lines, lap and edge counters of both oscillators, matrix of arbiters, control block and output decoder. Close to 1 ps resolution of such TDC can be achieved when it is synthesised in 65 nm and 0.13 µm CMOS technologies.

Digital filters made of a proportional and integral gain parts and additional IIR filters should be used in multiband synthesisers for IoT and IoV applications. If four stages of IIR filter are used, such a filter allows us to set a synthesiser to type-I or type-II and change its order from first to sixth.

The proposed structure with presented blocks of frequency synthesiser allows us to achieve a synthesiser's in-band phase noise of lower than −100 dBc/Hz, an out-of-band phase noise equal to −134.0 dBc/Hz, allows us to set a synthesiser to type-I or type-II, and to change its order from first to sixth.

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