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Design of Voltage Mode Electronically Tunable First Order All Pass Filter in ±0.7 V 16 nm CNFET Technology

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Abstract: A novel voltage mode first order active only tuneable all pass filter (AOTAPF) circuit configuration is presented. The AOTAPF has been designed using ±0.7 V, 16 nm carbon nanotube field effect transistor (CNFET) Technology. The circuit uses CNFET based varactor and unity gain inverting amplifier (UGIA). The presented AOTAPF is realized with three N-type CNFETs and without any external passive components. It is to be noted that the realized circuit uses only two CNFETs between its supply-rails and thus, suitable for low-voltage operation. The electronic tunability is achieved by varying the voltage controlled capacitance of the employed CNFET varactor. By altering the varactor tuning voltage, a wide tunable range of pole frequency between 34.2 GHz to 56.9 GHz is achieved. The proposed circuit does not need any matching constraint and is suitable for multi-GHz frequency applications. The presented AOTAPF performance is substantiated with HSPICE simulation program for 16 nm technology-node, using the well-known Stanford CNFET model. AOTAPF simulation results verify the theory for a wide frequency-range.

Keywords: APF; CNFET; pole-frequency; chirality; phase angle; tuning

1. Introduction

First order active all pass filter (APF) is an important analog signal processing (ASP) module. It is used for design of multiphase oscillators, phase-equalizers and high-quality-factor frequency-selective circuits. Several first order voltage mode (VM) single-ended (SE) APF circuit realizations have been reported in technical literature [1–8]. These APF circuits use a variety of efficient active-building-blocks (ABBs). However, these realized APFs are based on passive elements and large number of transistors count, which result in larger chip-area, lower slew rate, higher power dissipation and limitations to higher frequency operations. Few such APF configurations with low active and passive component counts are also available in the technical literature [9–18]. Some of these APF circuits also employ one or more ideal DC current-sources for biasing, which further increase the transistor count [15,17,18].

From the integrated circuit point of view, the active only filters (AOFs) provide several attractive advantages like capability of operating at much higher frequencies, lesser chip area, low power dissipations and electronic tunabilty. As a result, few first order AOTAPFs are reported in the technical literature [19–21]. These AOTAPFs use the MOSFETs transconductance and intrinsic gate to source parasitic capacitance as filter design components; still, the frequency of operations falls with in MHz range. Moreover, these reported AOTAPF circuits also contain a large number of transistors.

The APF circuits proposed in the technical literature [1–21] are based on bulk-semiconductor-technology. This technology faces serious challenges due to the persistent focus on transistor-scaling in nano meter regime for further continuation of Moore's law. These obstacles contain scattering-effect, decreased gate control, parasitic-capacitance, drain to source tunneling, channel mobility, threshold-voltage-variability [22,23]. It has been proven experimentally that below 65 nm-node, high-frequency analog circuit performance of silicon based semiconductor CMOS-technology is seriously degraded [24,25]. These emerging difficulties led the integrated-circuits industry to explore alternative materials and devices for below 65 nm-node that work equally well for future high-frequency ASP applications and more than Moore's technologies devised by ITRS recently [26]. These include double gate FETs, FinFETs and carbon nanotube field effect transistors (CNFETs) etc. [22].

Among these new devices, CNFETs are self-evident frontrunners for future continuation of downscaling the feature length to further extend the saturated Moore's law in nanometer-regime in the case of CMOS-technology [23,25,27]. CNFET has potential to minimize the serious emerging problems of current CMOS-based technology due to its near ballistic-charge-conduction, smaller feature size, fast switching-speed, lower power-dissipation, higher cutoff frequency, lower parasitic capacitances and larger drive-current [26,27]. These outstanding features make the CNFET a potential candidate for future high-frequency analog circuit applications. Since CNFET introduction as an alternative to MOSFET, limited studies on CNFET-based analog filter design have been carried out [28–36].

In this paper, a new VM SE CNFET-only APF is proposed. The realized APF has a very compact circuit structure and it is free from external passive capacitors and resistors. The proposed AOTAPF employs only three N-type CNFETs instead of massive ABBs. Moreover, the proposed topology is tuneable over a wide frequency range. In addition, the proposed circuit is free from any matching constraint and it is a potential candidate for low power, low voltage and high-frequency applications. The AOTAPF circuit is substantiated with HSPICE-simulation using the Stanford-CNFET-model.

The rest of this paper is organized as follows. Section 2 describes a brief overview of CNFET. The unity gain inverting amplifier (UGIA) with its equivalent parasitic model is discussed in Section 3. Section 4, illustrates the proposed CNFET-based VM AOTAPF. The performance and simulation results of the proposed AOTAPF are given in Section 5. Comparison of the proposed circuit with other compact topologies of APFs in the technical literature is presented in Section 6. Finally, Section 7 concludes the work.

2. Carbon Nano-Tube Field Effect Transistor

Carbon nanotubes (CNTs) are graphite-cylindrical-sheets (GCSs), which are considered as the most promising material for future nano-electronic devices and applications, due to their exceptional electronic, mechanical, chemical and thermal properties. CNTs are classified as single-wall CNTs and multi-wall CNTs. Single-wall CNT is based on single GCS while multi-wall CNT consists of more than one GCS. The properties of single-wall CNT are dependent on the chirality-vector (C_h) [28,29]. The C_h is defined by vector indices n_1 and n_2, which are positive-integers. The arrangement-angle of carbon atoms along the CNT is determined by C_h. The single-wall CNT can be of metallic or semiconducting behavior depending on the vector indices n_1 and n_2. If $\mid n_1 - n_2 \mid$ is an integer-multiple of three or $n_1 = n_2$, the single-wall CNT behaves as metallic, otherwise it behaves as semiconductor. The C_h, diameter (D_T) and threshold-voltage (V_{th}) of a CNT are related by the following equations.

$$C_h = a\sqrt{n_1^2 + n_2^2 + n_1 n_2} \tag{1}$$

$$D_T = C_h/\pi \tag{2}$$

$$V_{th} = aV_\pi/\sqrt{3}eD_T \tag{3}$$

where, e is the unit-electron-charge and a is the graphene-lattice-constant with a value of $2.49A^{\circ}$. V_{π} is the π to π bond-energy in tight-bonding-model with a value of 3.033 eV [30]. CNFET is one of the most attractive applications of CNT, which is obtained by replacing the MOSFET channel with one or more single-wall semiconducting CNTs as a channel material, as shown in Figure 1. Like conventional-MOSFET, CNFET is also a voltage-controlled-device and the current through the CNT based channel is controlled via gate voltage. CNFET gate is coupled capacitively with the beneath channel that consists of one or more narrow CNT. A single-CNT provides a limited amount of current. To enhance the channel current significantly, multiple parallel CNTs are incorporated in the channel. As compared to CMOS, where the design is dependent on the aspect ratio of transistors, a CNFET is usually optimized in terms of D_T, number of CNTs (N_T) and inter-CNT pitch (S_T). The S_T is basically the distance between the centers of two adjacent CNTs under the same gate. The width of the CNFET gate (W_g) is determined by the following equation [35]:

$$W_g = min(W_{min}, (N_T - 1)S_T + D_T) \tag{4}$$

where, W_{min} is the minimum gate width. The CNFET gate capacitance (C_g), is one of the key device features and it significantly affects the performance, especially at high-frequencies. The C_g is composed of three different capacitive components; coupling capacitance among the gate and adjacent contacts (C_{gtg-t}), gate outer-fringe capacitance (C_{fr-t}) and gate to channel capacitance (C_{gc-t}). The C_{gc-t} is further composed of two capacitances C_{gc-m} and C_{gc-e}, which are capacitances of single-wall CNTs located in the middle and edge of CNFET respectively. The C_{gc-t} components are shown in Figure 2. The CNFET gate capacitance parameters are:

$$C_{gtg-t} = W_g C_{gtg} \tag{5}$$

$$C_{fr-t} = L_s C_{fr} \tag{6}$$

$$C_{gc-t} = L_g C_{gc} \tag{7}$$

where, W_g and L_g are the CNFET channel-width and channel-length respectively. L_s is the length of doped source-side extension region. C_{gtg} is the gate-coupling capacitance per unit gate-width, C_{gc} is the gate to channel capacitance per unit channel-length and C_{fr} is the gate outer-fringe capacitance per unit CNT length. Comparatively to C_{gc} and C_{gtg}, the C_{fr} capacitance magnitude is quite smaller and thus its effect can be ignored [35]. The C_g thus can be approximated as:

$$C_g \approx (C_{gtg} * W_g) + (C_{gc} * L_g) \tag{8}$$

The drain/source capacitance $(C_{d/s})$ can be determined by following relation.

$$C_{d/s} \approx (C_{sub}/C_{ox} + 1) + (C_{gd/gs}) \tag{9}$$

where, C_{sub} is the capacitance between the CNFET channel and substrate, C_{ox} is the capacitance between the CNFET gate and channel and $C_{gd/gs}$ is the capacitance of the CNFET gate to the drain/source contact. The ratio C_{sub}/C_{ox} is only important when CNFET substrate drive (switches) the gate. To assess the potential performance of CNFET, an accurate and efficient device-model is required, which incorporates typical non-idealities of CNFET device. Most available models of CNFETs in recent literature bear the drawback of ideal modeling, resulting in ignoring numerous important effects [36,37]. The Stanford CNFET model overcomes shortcomings of previous models by including several non-idealities like drain to source series resistance, interconnect wiring capacitance, finite scattering mean free path, inter CNT charge-screening-effect, effect of drain-source extension region

and many more [38]. The Stanford CNFET model has been experimentally validated and it efficiently predicts the dynamic and transient performance with more than 90% accuracy [34].

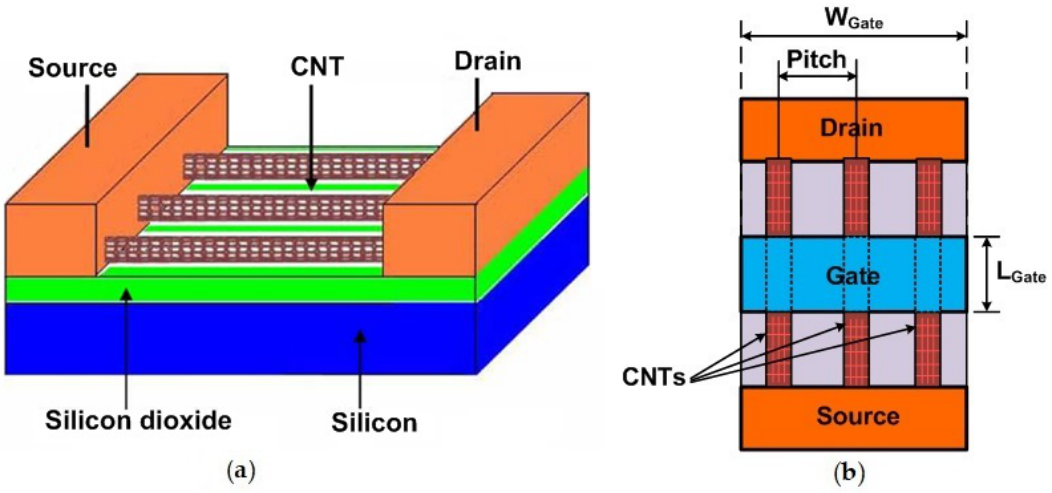

Figure 1. Carbon nanotube field effect transistor (CNFET) (**a**) Schematic; (**b**) Top-View.

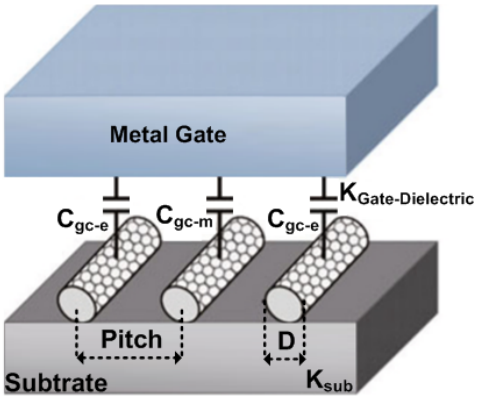

Figure 2. CNFET gate to channel capacitance.

Some important Stanford CNFET-model parameters are shown in Table 1.

Table 1. The Stanford CNFET model parameters.

Parameter	Description	Value
V	Power-supply	0.7 V
L_g	Physical-channel-length	16 nm
S_T	CNTs-pitch	10 nm
(n_1, n_2)	CNTs-chirality	(19, 0)
Lceff	Mean free-path in intrinsic-CNT	200 nm
V_{fbn}	N-type CNFET flatband-voltage	0
High-K_{ox}	Dielectric material of top-gate	HfO_2 (16)
L_s	Source-side length of doped-CNT	16 nm
L_d	Drain-side length of doped-CNT	16 nm
T_{ox}	Oxide-thickness	4 nm
K_{sub}	Dielectric constant	SiO_2 (4)
Leff	Mean free-path in doped-CNT	15 nm
E_{fo}	Fermi-level of n+ doped drain/source CNT-region	0.6 eV
N_T	Total number of CNT used per CNFET	∼

∼: Variable parameter.

3. CNFET Based UGIA

The UGIA is one of the simplest types of ABB, which employs two N-type CNFETs as shown in Figure 3a [16] and its symbol is shown in Figure 3b. Its transfer gain can be expressed as follows.

$$\frac{V_o}{V_i} = -\frac{g_{m2}}{g_{m1}} \tag{10}$$

where, g_{m1} and g_{m2} are the transconductance gains of the CNFETs T_1 and T_2 respectively. With symmetrical T_1 and T_2 on the same die, the $g_{m1} = g_{m2}$, the Equation (10) reduces to

$$\frac{V_o}{V_i} = -1 \tag{11}$$

Thus, the circuit of Figure 3a, realizes an unity gain inverting amplifier (UGIA). The UGIA equivalent parasitic-model is shown in Figure 3c. Its input and output port resistances can be expressed as

$$r_i = r_g \tag{12}$$

$$r_o = r_{ds1} || r_{ds2} \tag{13}$$

where, r_g represents the gate-resistance of transistor T_2 and r_{ds1}, r_{ds2} are the channel-resistances of transistors T_1 and T_2 respectively. The UGIA input port has very high-resistance. The UGIA output port, being the voltage source, exhibits small resistance.

The impact of increasing CNTs (N_T) of both the CNFETs of the UGIA on its performance is studied using HSPICE simulation tool. In the simulations, the Stanford CNFET model is used for the CNFETs with transistor parameters of Table 1. Figure 4 demonstrates the impact of N_T on r_o, C_i, C_o, power dissipation and -3 dB bandwidth of the UGIA. A single CNT carries approximately a constant current of 20 µA [28]. The increase of N_T of transistors increase the overall current drive capability and hence the transconductance [29]. The impact of increasing N_T on UGIA r_o is shown in Figure 4a. It is seen that by increasing N_T, the output resistance r_o decreases. Since an increase in N_T is equivalent to an increase in channel width of the CNFETs, r_o decreases with the increase of N_T. The effects of increasing N_T on input and output parasitic capacitances C_i and C_o of the UGIA, are shown in Figure 4b. It is observed that by increasing N_T, both the parasitic capacitances C_i and C_o increase. Figure 4c demonstrates the effect of increasing N_T on the UGIA power dissipation. The power dissipation of UGIA increases as N_T increases. The current drive capability of employed CNFETs increases with an increase of N_T, which leads to an increase in power dissipation. Figure 4d demonstrates the effect of increasing N_T, on UGIA -3 dB bandwidth. It is observed that by increasing N_T, the -3 dB bandwidth of UGIA increases.

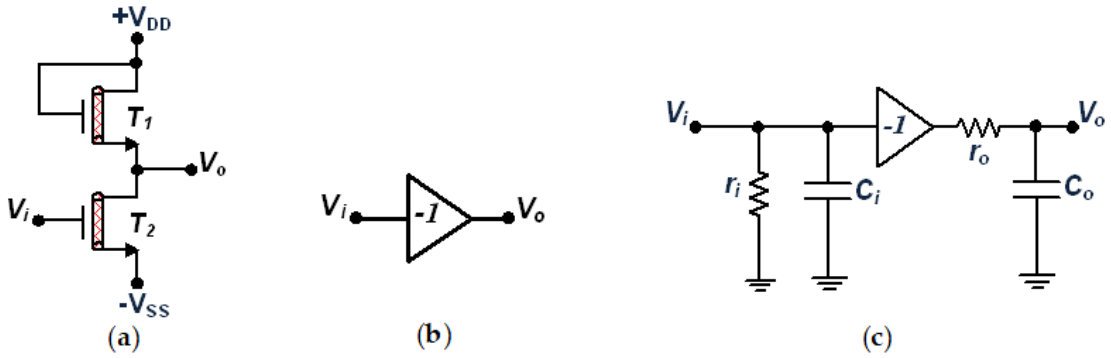

Figure 3. CNFET based UGIA: (**a**) Transistor-level realization; (**b**) Symbol; (**c**) Parasitic model.

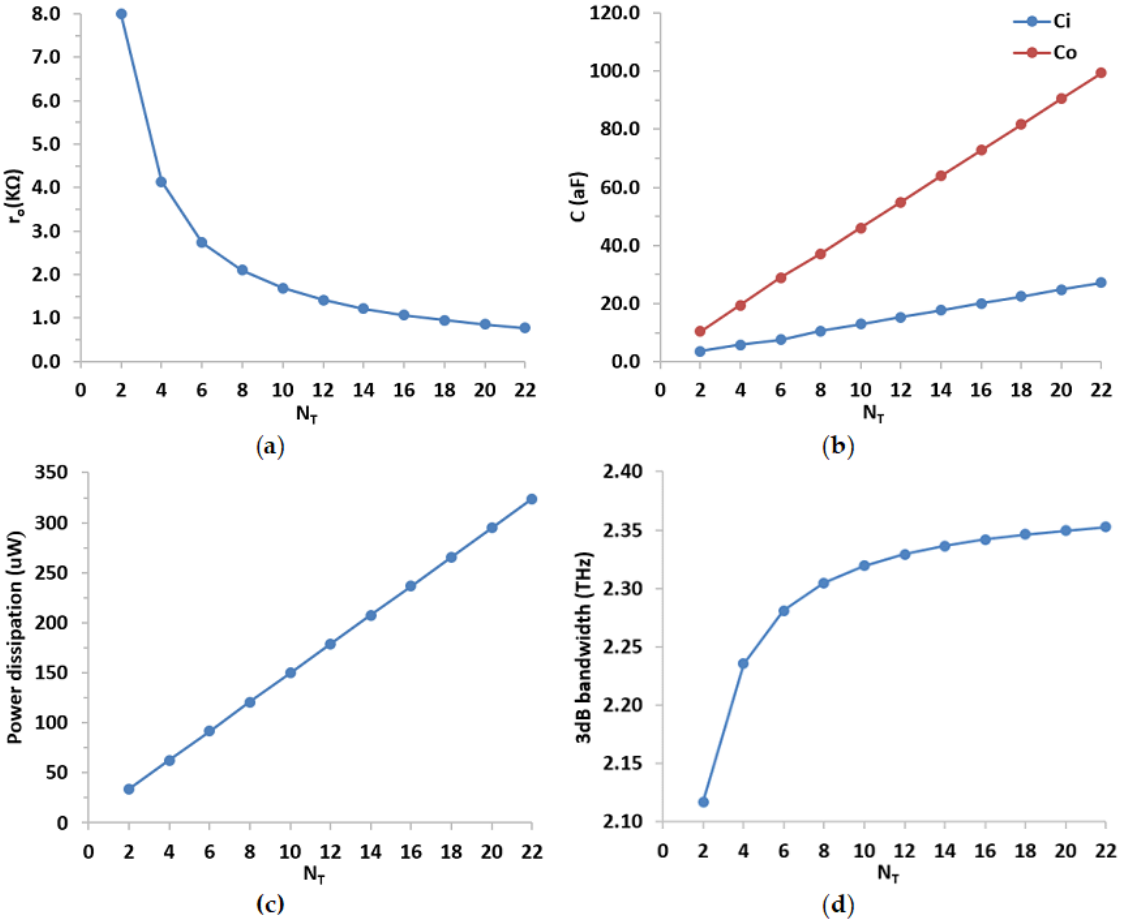

Figure 4. Effect of variation of N_T on unity gain inverting amplifier (UGIA): (**a**) r_o; (**b**) C_i and C_o; (**c**) Power dissipation; (**d**) −3 dB bandwidth.

The transient and AC-analysis were performed with CNFET parameters of Table 1, with $N_T = 2$. Figure 5a shows the transient-response of UGIA input and output voltage at 50 GHz. Figure 5b displays the UGIA AC simulation results of voltage-gain (V_o/V_i). It is seen that the obtained voltage-gain magnitude is unity over a wide range of frequency. The −3 dB frequency of employed UGIA voltage-gain is 2.1172 THz. This massive value of −3 dB cutoff frequency makes the UGIA a potential candidate for the design of high frequency ASP modules.

The UGIA parasitic capacitance C_i and resistance r_i are found as 3.54 aF and 1 TΩ respectively. Figure 5c displays the frequency response of UGIA output port resistance (r_o), which is constant at r_o = 7.9921 kΩ over wide frequency-range. The −3 dB cutoff frequency of the UGIA output-impedance is obtained as 1.9017 THz. The UGIA output parasitic-capacitance, C_o is found as 10.472 aF, which is nearly insignificant for frequency-range up to several GHz. The total-harmonic-distortion (THD) of UGIA is determined by applying a 50 GHz sinusoidal-signal to input with different voltage amplitudes. Simulation results are presented in Figure 6a. It can be seen that THD is less than 1% for sinsoidal signal with amplitude of 200 mV. Monte Carlo simulation results of the UGIA were performed for 30-trials with transient and AC-sweep environment to see the influence of process-variations. Figure 6b,c illustrate the results of Monte Carlo analysis for UGIA transient and AC-sweep respectively.

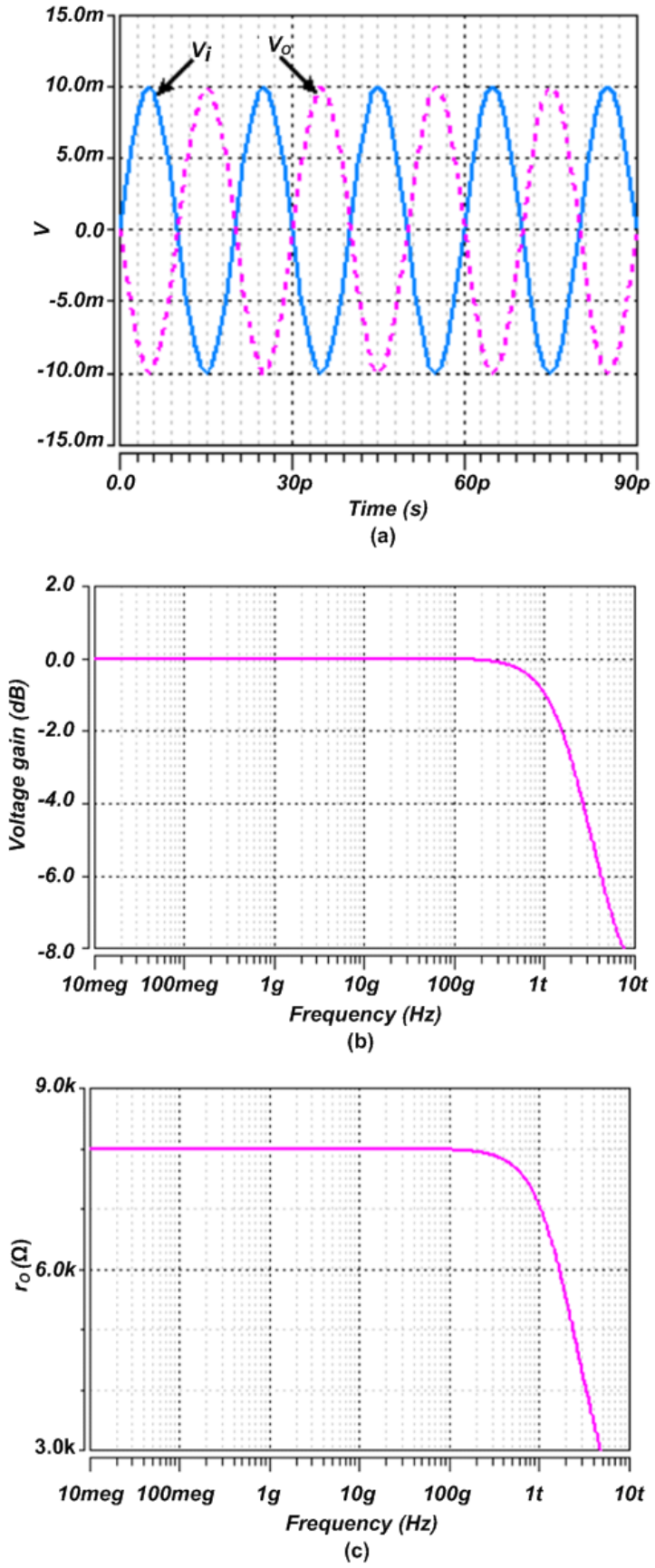

Figure 5. The UGIA: (**a**) Transient-response; (**b**) Frequency-response of Voltage-gain (V_o/V_i); (**c**) Frequency-response of Output-impedance.

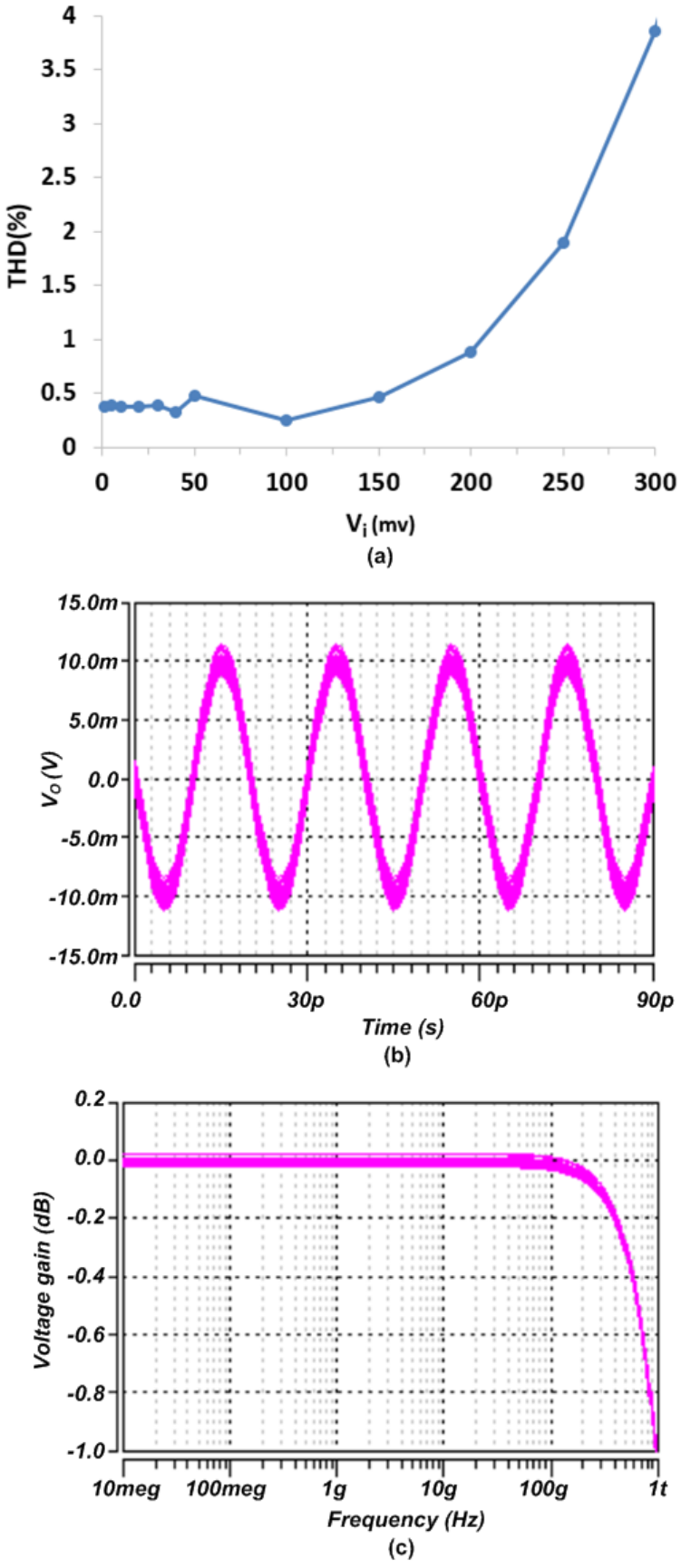

Figure 6. The UGIA: (**a**) THD Vs input voltage at 50 GHz; (**b**) Monte Carlo simulations for V_o in time domain; (**c**) Monte Carlo simulations for voltage gain in frequency domain.

4. AOTAPF Circuit Description

The basic scheme for first order APF section is given in Figure 7a. Its transfer function can be expressed as follows.

$$\frac{V_o}{V_i} = \frac{s-a}{s+a} \tag{14}$$

Its equivalent RC circuit along with a unity gain inverting amplifier is shown in Figure 7b, where pole frequency $\omega_o = a = 1/RC$. The CNFET version of Figure 7b is given in Figure 7c, where the unity gain inverting amplifier is replaced with UGIA of Figure 3a and the capacitor C is replaced with a CNFET based varactor capacitance C_{var} between input and output. The N-Type CNFET based varactor used in Figure 7c is given in Figure 8a. Its equivalent symbol is shown in Figure 8b. The varactor CNFET source and drain are tied together and connected to the tuning control voltage (V_{tune}) to form one capacitor terminal (x), while the gate form the other terminal (y). The varactor capacitance (C_{var}) can be controlled by varying V_{tune}. The output resistance r_o of UGIA is utilized to the benefit, to replace resistor R of Figure 7b. The circuit of Figure 7c results in an active only tunable all pass filter (AOTAPF).

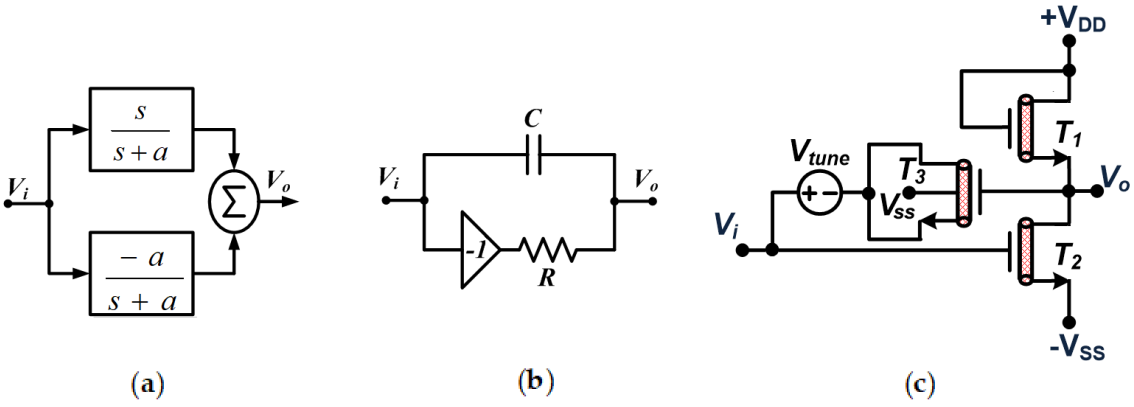

Figure 7. First order APF: (**a**) Basic scheme; (**b**) Equivalent circuit; (**c**) CNFET based implementation.

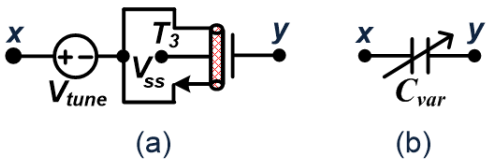

Figure 8. CNFET based varactor: (**a**) Transistor-level realization; (**b**) Symbol.

Ignoring the effect of extremely low valued output capacitance C_o of UGIA, the proposed VM SE AOTAPF circuit shown in Figure 7c results in the following voltage transfer function (VTF).

$$\frac{V_o}{V_i} = \frac{(s - \frac{1}{r_o C_{var}})}{(s + \frac{1}{r_o C_{var}})} \tag{15}$$

From Equation (15), the pole-frequency ($\omega_o = \omega_z = \omega_p$) and the phase-angle ($\phi$), can be expressed respectively as:

$$\omega_o = \frac{1}{r_o C_{var}} \tag{16}$$

$$\phi = \pi - 2tan^{-1}(\omega r_o C_{var}) \tag{17}$$

The Proposed AOTAPF pole-frequency incremental sensitivity with respect to the components C_{var} and r_o can be expressed as:

$$S_{C_{var}}^{\omega_o} = S_{r_o}^{\omega_o} = -1 \tag{18}$$

From Equation (18), it is observed that the incremental sensitivities of the pole-frequency (ω_o) with respect to C_{var} and r_o are within unity in magnitude. By considering the UGIA non-ideal voltage-gain (α) and parasitic resistance (r_s) of tuning control voltage (V_{tune}) into consideration, the VTF of Equation (15) can be expressed as follows.

$$\frac{V_o}{V_i} = \frac{(s(1-\frac{r_s}{r_o}) - \frac{\alpha}{r_o C_{var}})}{(s(1+\frac{r_s}{r_o}) + \frac{1}{r_o C_{var}})} \tag{19}$$

From Equation (19) it is seen that the AOTAPF gain and pole-frequency (ω_p) is insensitive to α. However, the zero-frequency (ω_z) is affected slightly due to α. Moreover, the impact of source resistance (r_s) on the performance of APF is negligible due to the presence of high valued output resistance (r_o) of the UGIA ($r_o \gg r_s$). Thus, the effect of r_s can be ignored. By considering α into account, the non-ideal phase-angle for the realized filter can be expressed as follows.

$$\phi = \pi - tan^{-1}(\frac{\omega r_o C_{var}}{\alpha}) - tan^{-1}(\omega r_o C_{var}) \tag{20}$$

Thus, it is seen from Equation (20) that the phase-angle is slightly affected by α. To examine the high-frequency performance of the realized AOTAPF, the UGIA parasitic impedances must be evaluated. By considering the α and non-ideal parasitic impedances of UGIA, the ideal VTF of the realized AOTAPF as illustrated by Equation (15) turns out to be

$$\frac{V_o}{V_i} = \frac{C_{var}}{C_{var}+C_o} * \frac{(s - \frac{\alpha}{r_o C_{var}})}{(s + \frac{1}{r_o(C_{var}+C_o)})} \tag{21}$$

From Equation (21), the ω_z and ω_p can be written as

$$\omega_z = \frac{\alpha}{r_o C_{var}} \tag{22}$$

$$\omega_p = \frac{1}{r_o(C_{var}+C_o)} \tag{23}$$

It is evident from Equation (22) that the non-ideal factor α sightly affects the zero-frequency. In addition, it can be noticed from Equation (23) that UGIA parasitic capacitance C_o affects the pole-frequency. The influence of the C_o on the performance of the AOTAPF can be minimized by making $C_{var} \gg C_o$.

5. Design and Verification

To verify the proposed AOTAPF circuit, it is designed and simulated using HSPICE simulation tool with the Stanford CNFET model parameters of Table 1. Based on Equation (21), the value of the varactor capacitance (C_{var}) is to be set sufficiently higher than the parasitic capacitance (C_o), to evade the mismatch between zero and pole frequencies as well as non-unity gain for higher frequencies design. Figure 9 shows the capacitance tuning characteristics (C-V curves) of the realized CNFET varactor of Figure 8a, with different values of N_T. It has been observed that by increasing N_T, the capacitance spread ($C_{max} - C_{min}$), increases, which ultimately determines the frequency tuning range of AOTAPF. The C-V relationship approximated by polynomial curve fitting is given in Appendix A. For instance, with $N_T = 100$ and by setting $V_{tune} = -0.32$ V for CNFET T_3, the observed C_{var} is 0.40423 fF. Thus, with r_o = 7.9921 kΩ, Equation (16) yields the pole frequency f_o = 49.26 GHz.

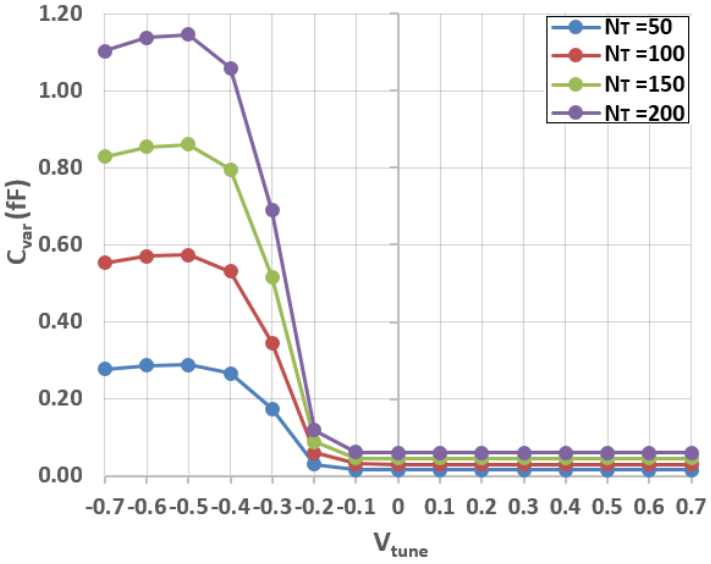

Figure 9. CV characteristics of varactor with different N_T.

The designed circuit was simulated with a sinusoidal input signal of 10 mV peak. The results thus obtained are given in Figures 10–12. The transient response at the designed frequency of f_o = 49.26 GHz is shown in Figure 10, where a phase shift of 90° is evident. Figure 11a,b show the ideal and simulated magnitude and phase responses respectively. The proposed AOTAPF power dissipation is found to be 33.76 µW. It is noticed that the realized APF dissipates very small power, even at very high frequency of operation. Figure 12 shows the equivalent input and output noises against the frequency. It is noticed that the equivalent input noise and output noise for the realized AOTAPF at a designed pole-frequency of 49.26 GHz are found as 6.822 nv/Hz and 6.761 nv/Hz respectively, which are satisfactorily low values. Monte Carlo simulation results of AOTAPF were performed for 30-trials with transient and AC-sweep environment to see the influence of process-variations. Figure 13a–c illustrate the results of the AOTAPF Monte Carlo analysis for transient, voltage gain and phase responses respectively. Here, it is observed from Figure 13 that there are no considerable variations of the filter performance characteristics.

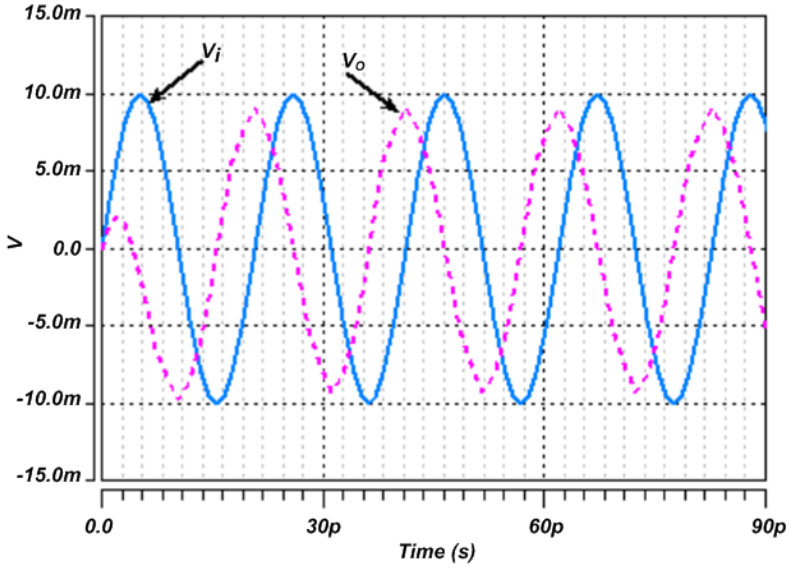

Figure 10. Transient-response of AOTAPF at pole-f_o = 49.26 GHz and $V_{tune} = -0.32$ V.

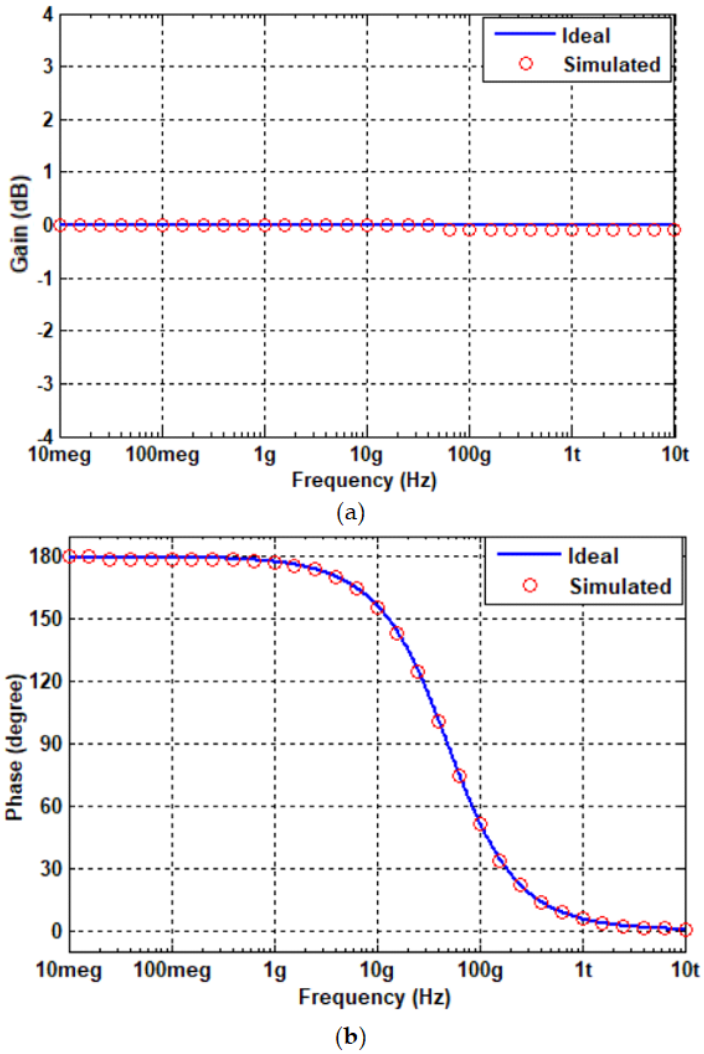

Figure 11. Ideal and simulated frequency-response of AOTAPF at $V_{tune} = -0.32$ V: (**a**) Voltage gain; (**b**) Phase.

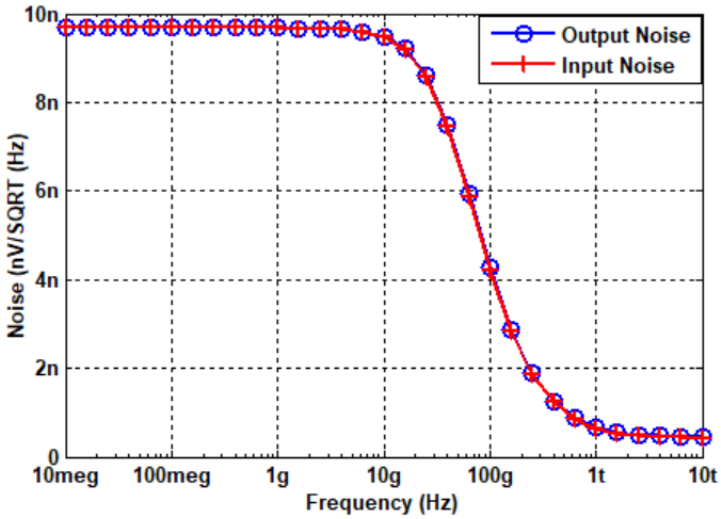

Figure 12. Frequency-response of input and output noise of AOTAPF at $V_{tune} = -0.32$ V.

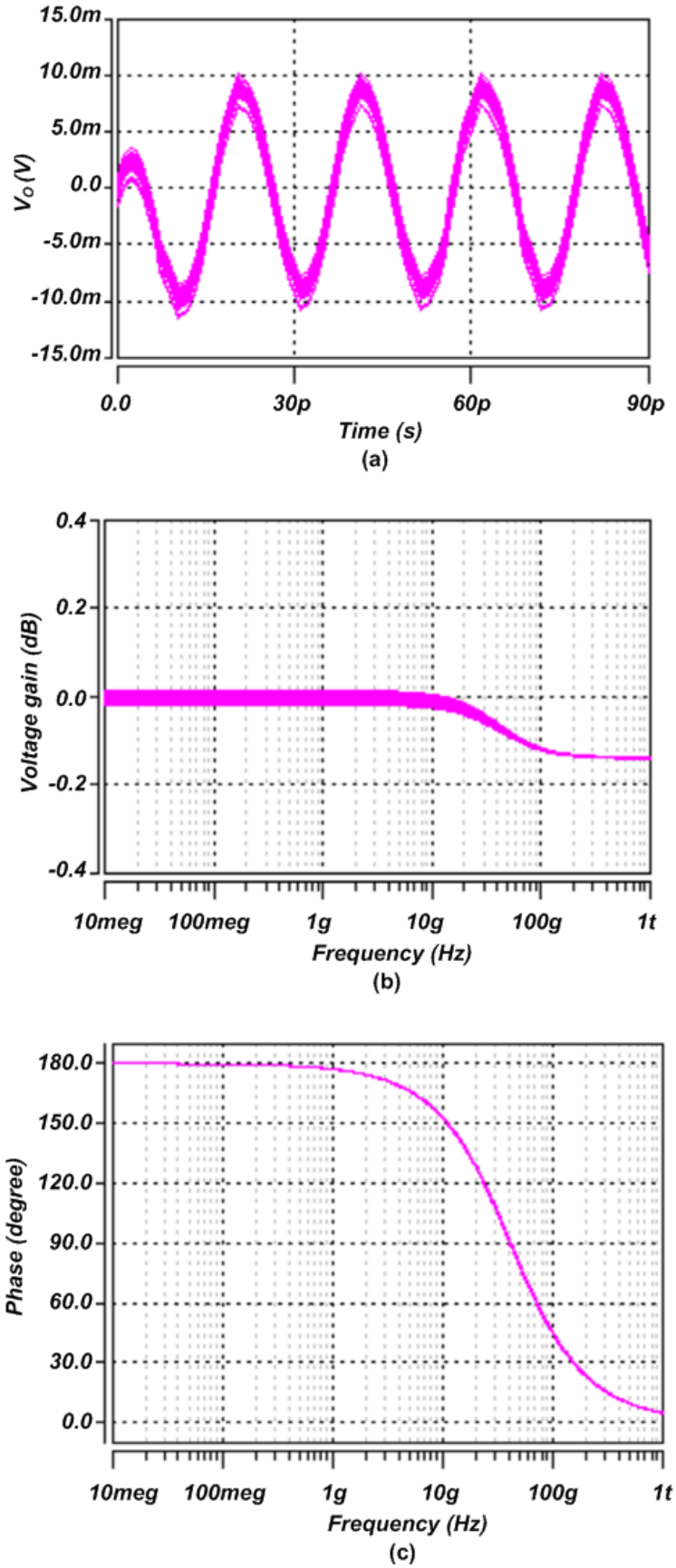

Figure 13. Monte Carlo simulations of AOTAPF for: (**a**) Time domain; (**b**) Voltage-gain (V_o/V_i); (**c**) Phase.

Next, to demonstrate the proposed circuit tunabilty feature, different tuning voltages (V_{tune}) are applied to the varactor. By varying the V_{tune} from −0.5 V to −0.3 V the varactor capacitance (C_{var}) varies in the range of 0.574 fF to 0.346 fF respectively. Figure 14a,b demonstrate the magnitude and phase responses respectively of the realized AOTAPF, at different values of V_{tune}. It is noticed from Figure 14b that by varying the V_{tune} from −0.5 V to −0.3 V, the pole frequency of the proposed filter varies in the range of 34.2 GHz to 56.9 GHz. This wide range of pole frequency by adjusting V_{tune} makes the proposed circuit as a potential candidate for multi GHz applications. The transient responses of the proposed filter for different tune voltages are shown in Figure 15. A phase shift of 90° is noticed for each pole frequency. The THD variations are found as 3.81%, 2.6% and 1.72% for V_{tune} equal to −0.30 V, −0.33 V and −0.50 V respectively. Thus, all the simulation results on the proposed AOTAPF support the theory.

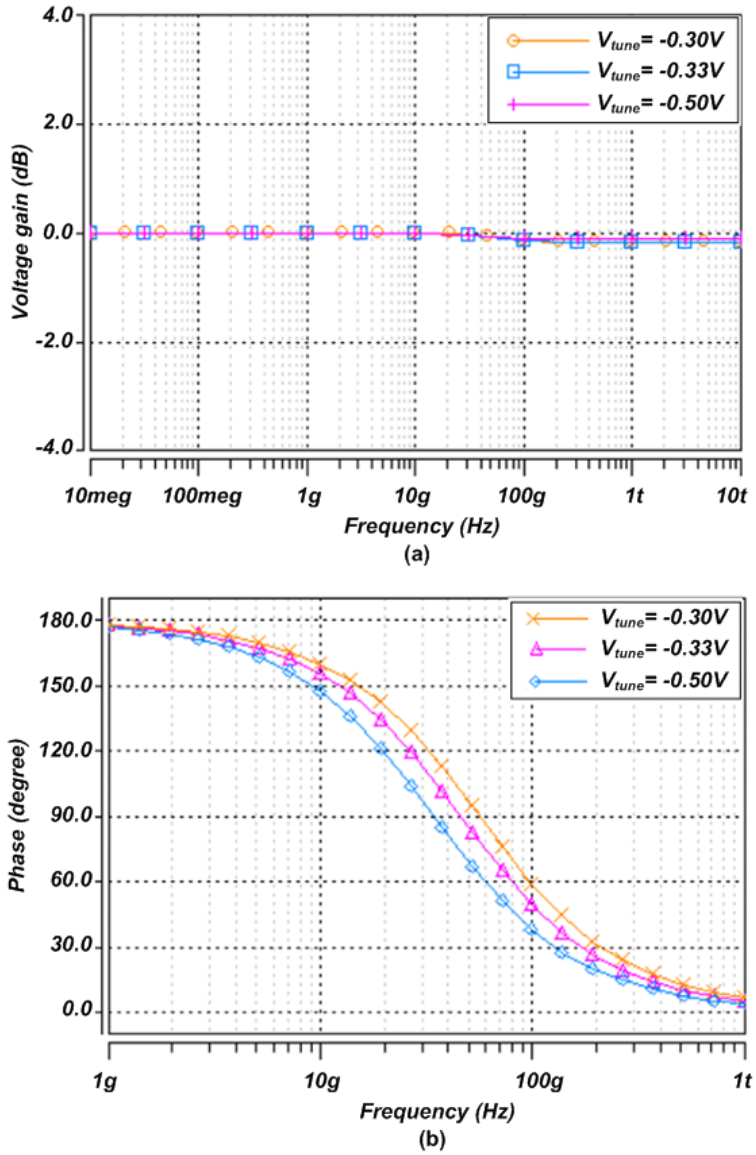

Figure 14. Frequency-response of AOTAPF at different values of V_{tune}: (**a**) Voltage gain; (**b**) Phase.

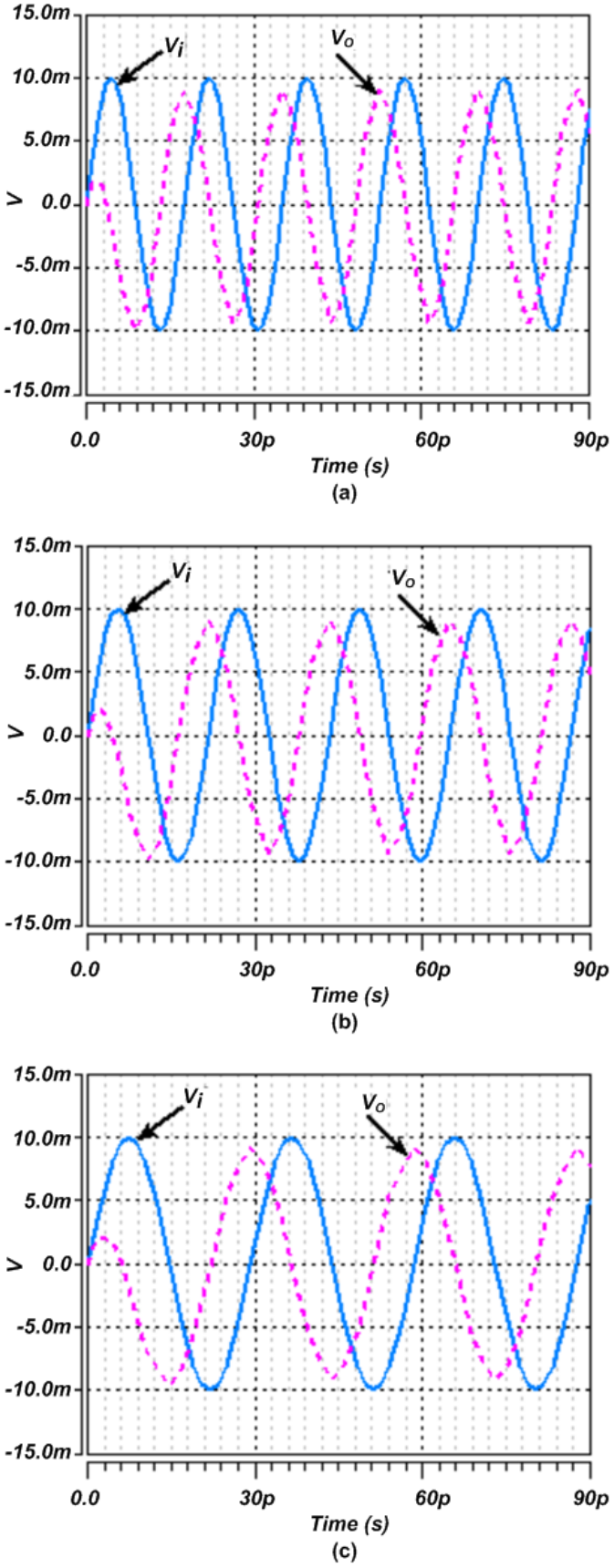

Figure 15. Transient-response of AOTAPF at different values of V_{tune}: (**a**) −0.30 V; (**b**) −0.33 V; (**c**) −0.50 V.

6. Performance Comparison of the Proposed APF

A brief comparison of the proposed AOTAPF with other available VM SE tunable APF circuit configurations is given in the Table 2. For comparison, only APFs realized with not more than 10 transistors are chosen. The APFs of [12–18] employ one or more external passive components, which result in occupying larger chip area and also suffer from slew rate limitations as well as wide tolerance. However, the proposed AOTAPF is free from any external passive component. The APFs presented in [15,17–21] utilize one or more DC current sources for tunability of pole frequency via altering biasing current. However, additional transistors need to be employed for realization of these DC current supplies and thus the transistor count will further increase. It is to be noted like previously presented APFs of [14,15], that the proposed AOTAPF is also suitable for low voltage operation as it employs only two active devices between its supply rails. The proposed AOTAPF circuit configuration is based on only three transistors, while the realized AOTAPF circuits of [19–21] use several transistors as they utilize ideal current sources. Although, the previously presented APF circuits of [14,18] are also based on three transistors like the proposed AOTAPF, but they use one or more external passive components. In addition, the reported APF of [18] uses an ideal DC current source which will ultimately increase the transistor count. Table 2 shows that the CMOS-based APF circuit configurations are limited to MHz range while the proposed circuit operates in several GHz ranges.

Table 2. Comparison of AOTAPF with other reported APFs.

Ref	Ideal Current Source Used	Number of Transistors	Number of External R/C	Technology (nm)	Supply Voltage	Tuning Range (Hz)	Power Dissipation (mW)
[12]	No	4	2/1	180	±0.9	544.8 K to 2.9 M	20.4
[13]	No	9	2/1	350	±1.5	10 K to 56 K	-
[14]	No	3	2/1	90	±0.45	103 K to 18.3 M	0.418
[15]	Yes	5	0/1	350	±1.5	-	-
[16]	No	5	0/1	180	±0.9	3.48 M to 26.1 M	-
[17]	Yes	6	0/1	180	±0.9	1.07 M to 9.44 M	10.5
[18]	Yes	3	0/1	130	±0.75	-	20.6
[19]	Yes	4	0/0	350	±1.65	105 M to 205 M	-
[20]	Yes	8	0/0	350	-	-	-
[21]	Yes	4	0/0	350	±1.5	-	-
Proposed	No	3	0/0	16	±0.7	34.2 G to 56.9 G	0.0337

-: Not Available.

7. Conclusions

In this paper, a new single ended voltage mode first order all pass filter using CNFET based unity gain inverting amplifier and a varactor is presented. The proposed circuit is constructed with only three N-type CNFETs and thus it consumes very little area on chip. Since there are only two CNFETs stacked between the power-supply rails, it is able to work equally well at low voltages. The realized all pass filter circuit is free from external passive components and thus it is suitable for integrated circuit implementation. The proposed AOTAPF circuit non-ideal performance is also evaluated. The filter circuit is designed and verified with HSPICE, using the well-known Stanford CNFET model.

Initially, the CNFET-based unity gain inverting amplifier is studied for different numbers of CNTs. It was observed that with only two CNTs, the unity gain inverting amplifier yields optimal performance. Afterward, the CNFET-based varactor is simulated for different CNTs and variable DC voltages. This study enables the designer to choose the number of CNTs for the desired frequency range of operation. Then the realized AOTAPF circuit is studied in detail including gain, phase, and transient performance. The Monte Carlo analysis for process variations as well as THD simulation studies were also performed. The simulation results show a very good gain and phase characteristics at high frequencies with tunable pole-frequency range from 34.2 GHz to 56.9 GHz. This makes the proposed topology a potential contestant for high frequency applications. It will be interesting to substantiate the all pass filter simulation results experimentally; however, due to the current non-availability of

needed resources, experimental authentication is not performed. Physical realization of the presented AOTAPF may be a vital-direction for future extension of the proposed work.

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Abbreviations

The following abbreviations are used in this manuscript:

APF	All pass filter
AOTAPF	Active only tuneable all pass filter
ASP	Analog signal processing
CNFET	Carbon Nanotube Field Effect Transistor
GCSs	Graphite-cylindrical-sheets
SE	Single-ended
THD	Total-harmonic-distortion
UGIA	Unity gain inverting amplifier
VTF	Voltage transfer function
ω_o	Pole-frequency
ω_z	Zero-frequency
C_{var}	varactor capacitance

Appendix A

The capacitance tuning characteristics (C-V curves) of the realized CNFET varactor of Figure 8a, are obtained by sweeping the V_{tune} from -0.7 V to +0.7 V for different N_{Ts} using HSPICE simualtion tool. The analytical relationship between the capacitance C_{var} and the control voltage V_{tune} can be obtained by polynomial curve fitting for fixed N_T. For $N_T = 100$, the C-V relationship is approximated by following 2nd order polynomial expression:

$$C_{var} = (-6.0601V_{tune}^2 - 5.9693V_{tune} - 0.8934)\ fF \quad \text{(A1)}$$

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