The P-Type Module with Virtual DC Links to Increase Levels in Multilevel Inverters

Emad Samadaei [1,*]**, Mohammad Kaviani** [2]**, Mina Iranian** [3] **and Edris Pouresmaeil** [4,*]

[1] Department of Electromobility, Volvo Truck Group Technology, SE- 417 15 Gothenburg, Sweden
[2] Department of Engineering, Mazandaran University of Science and Technology, Babol 47166-85635, Iran; mohammad.kaviani70@gmail.com
[3] Department of Engineering, Atlas Danesh Co, Ghaemshahr 47658-37449, Iran; iranian_mina@yahoo.com
[4] Department of Electrical Engineering and Automation, Aalto University, 00076 Aalto, Finland
[*] Correspondence: emad.samadaei@volvo.com (E.S.); edris.pouresmaeil@aalto.fi (E.P.); Tel.: +358-50-598-4479 (E.P.)

Abstract: There has been an active interest in the evolution of newer multilevel inverter topologies in which the highest operation of DC sources become an important subject. In the paper, a new structure module presented a seventeen levels asymmetrical multilevel inverter by using two unequal DC sources (with the ratio 3:1). The configuration was focused on creating virtual DC links by two chargeable capacitors. The module had a simple inherent charging for capacitors without any additional circuit. The proposed multilevel inverter could produce higher voltage levels by a lower number of components; therefore, it is suitable for a wide range of applications. Also, the cascade connection of the module led to a modular topology with more voltage levels at higher voltages. The capability of the inherent negative voltage was involved. The simulation results obtained in MATLAB/Simulink, as well as the experimental results, verified the proposed topology.

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1. Introduction

Multilevel inverters (MLIs) have obtained more attention in recent years against two-level inverters because of their abilities in medium to high power applications, such as wind turbine [1], HVDC (High Voltage Direct Current) for transmission line [2,3], photovoltaic systems [4], drives systems [5,6], active power filer [7], power grid [8], and electrical vehicle [9]. MLIs synthesize the desired stepped output waveform from several DC voltage sources by the proper arrangement of the semiconductor switches. One of the important advantages of MLIs is using fewer components to create higher levels of the output voltage. Besides increasing the number of output voltage levels, high resolution on the output voltage and low harmonic components will be expected. Also, scalability, modularity, and lower switches stress are some of the other MLIs outstanding features due to the ability of cascade connection. Various topologies are introduced for MLIs. They can be categorized in three main types: NPC (Neutral Point Clamps) [10], FC (Flying Capacitor) [11], CHB (Cascade H-Bridge) [12]. Some disadvantages in NPC and FC, such as bulky capacitors, unbalanced DC links, and high switch stress, make CHB topologies more interesting. CHB has some comparable aspects: the number of semiconductors and DC sources and levels; total standing voltage (TSV) on switches; the inherent polarity levels, etc. Some conventional and vanguard topologies for the last decade were investigated in [13–16]. In [17], the module generated each level from one DC source by two switches. A series connection of the module can create more levels. The module can only generate positive polarity, and

it requires an extra circuit for negative polarity. Full-bridge was added to the series module in [18] to create both negative and positive levels. By adding full-bridge circuits, negative voltage polarity is generated by the penalty of high switching stress on the semiconductors in the additional circuit and increasing the number of components. The enhancement of multilevel inverters' performances depends on creating higher output voltage levels by using a lower number of switches and DC voltage sources. Recently, asymmetric multilevel inverters with unequal DC sources have been addressed to increase the output levels without any complexity to the power circuit. Modules are designed based on the optimal combination of DC links and semiconductors. On another side, unequal DC links in asymmetric multilevel inverters may influence the stress on switches. The stress on switches is indexed with total standing voltage (TSV), which is the sum of the highest voltage stress on each switch. In [19,20], crossing switches were introduced as a solution to dividing of stress on switches and generating more levels. [21,22] presented extended H-bridge with different amounts of DC links. As the number of voltage levels increases, H-bridge switches tolerate higher stress. So, these topologies need higher rate semiconductors. Another kind of MLIs was proposed in [23] that is well-known as hybrid type topologies, although stress on switches is still obvious. Using full-bridge for negative voltages increases stress on switching and total standing voltages (TSV) on semiconductors. [24,25] introduced modules with inherent negative levels based on the maximum levels of achievement with four DC sources and low semiconductors to overcome these disadvantages. Different energy sources or storage elements, such as capacitors, can be applied instead of some DC sources to form a sinusoidal waveform in various multilevel inverter structures [26]. As a result, output voltage levels are increased with the same number of DC sources. [27–29] redesigned the structure of [11,19] to replace capacitors with some DC sources. In order to decrease the number of sources, [30–33] used a single source. In these configurations, they needed more semiconductors for the charging/discharging of capacitors. Some stair modular configurations with diverse DC sources and capacitors were proposed in [34–36], although full-bridge was applied in the circuits for producing the negative levels.

In the proposed inverter module, a new arrangement of semiconductors was introduced, which used only two DC sources. Two DC sources were unequal with $1 \times V_{DC}$ and $3 \times V_{DC}$ (one/three times scale of base voltage, respectively). The proposed inverter generated 17 output voltage levels. On the other hand, the proposed asymmetric multilevel module could produce eight positive levels, eight negative levels, and zero level (total 17 levels). Also, it did not need any extra circuit (such as a full-bridge) for negative voltage levels. The cascade connections of the module were described to create more levels for high voltage applications. The proposed multilevel inverter was illustrated in Section 2. Module introduction, switching patterns, charging and discharging of capacitors, cascade connection, and comparison study were included in this section. In Section 3, the nearest level control (NLC) scheme as a switching modulation was described. The voltage ripple on capacitors was investigated in Section 4. Finally, simulation and experimental results were presented in Sections 5 and 6, respectively.

2. Proposed Module

Figure 1 illustrates a general concept diagram of the proposed multilevel inverter with two DC sources. In order to achieve maximum output levels from sources, capacitors could be added to the configurations. Some extra DC links were created by capacitors to get more levels with the same DC sources. As shown in Figure 1, two DC sources with ratio 3:1 ($V_{DC1} = 3V_{DC2}$) could create nine voltage levels; and it could be redesigned with two capacitors and suitable arrangements to create seventeen voltage levels in output. The charging paths of capacitors should be considered as well. The charging paths of capacitors could be provided by a suitable designing of semiconductors arrangement to achieve the output levels paths without using an additional circuit.
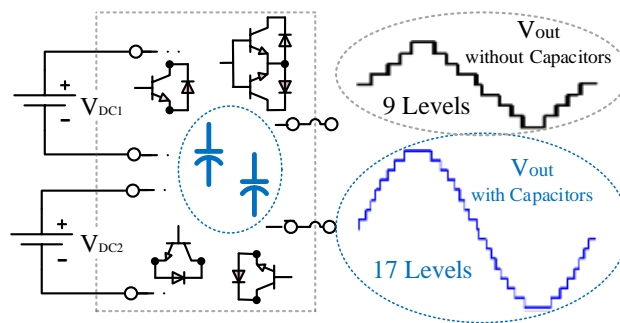
Figure 1. The general concept diagram of the proposed multilevel inverter (MLI) with capacitors.

2.1. Module Configuration

Asymmetric multilevel inverters could produce a different number of output voltage levels by using a fewer number of semiconductors in which it caused lower harmonic components as well. This promotion could be achieved by using two DC sources with different amounts as $1\text{x}V_{DC}$ and $3\text{x}V_{DC}$. It means the amount of one source was three times greater than the other one, and they were rewritten as $1V_{DC}$ and $3V_{DC}$ to simplify for the rest of the paper. In order to increase the number of DC links without any change in the number of DC sources, capacitors could be used. This idea gave four DC links involving 2 DC sources and 2 capacitors. Figure 2 shows the proposed module with a new arrangement of the components that contained 18 switches (8 unidirectional switches and 5 bidirectional switches) and 18 diodes in combination with 2 unequal DC sources and 2 capacitors. This configuration produced 17 levels of voltage at the output, including eight positive levels, eight negative levels, and zero level. This means that this module had an inherent negative level ability by connecting each DC link to other ones through different paths from different sides of a DC link. The structure of the proposed topology was figured to polygon, so it is named "P-Type" (Polygon-Type). The proper designing of the proposed module made that DC source with $1V_{DC}$ to charge the capacitor with $1V_{DC}$, and DC source with $3V_{DC}$ to charge the capacitor with $3V_{DC}$ without any additional circuit. Figure 3 draws the switching paths of all output voltage levels in the presented structure, and the state of switches in each level is listed in Table 1. The proposed module and their switching paths were designed accurately, as well as the positive terminals of DC links were not connected to the anode of diodes to cause the shortcuts. On the other hand, it was protected from short currents in which Figure 3 shows that the switching paths did not form any closed loop for DC links. Thus, diodes and bidirectional switches guaranteed that short-circuiting would not occur in the module.
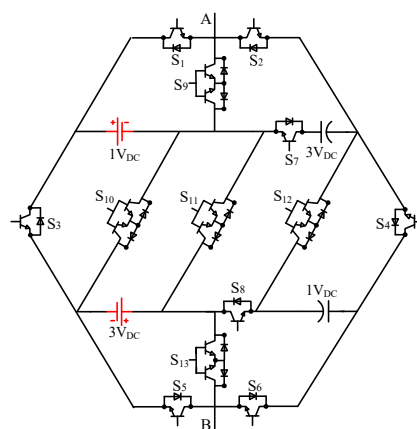

Figure 2. The proposed module (P-Type, Polygon-Type) for the multilevel inverter.
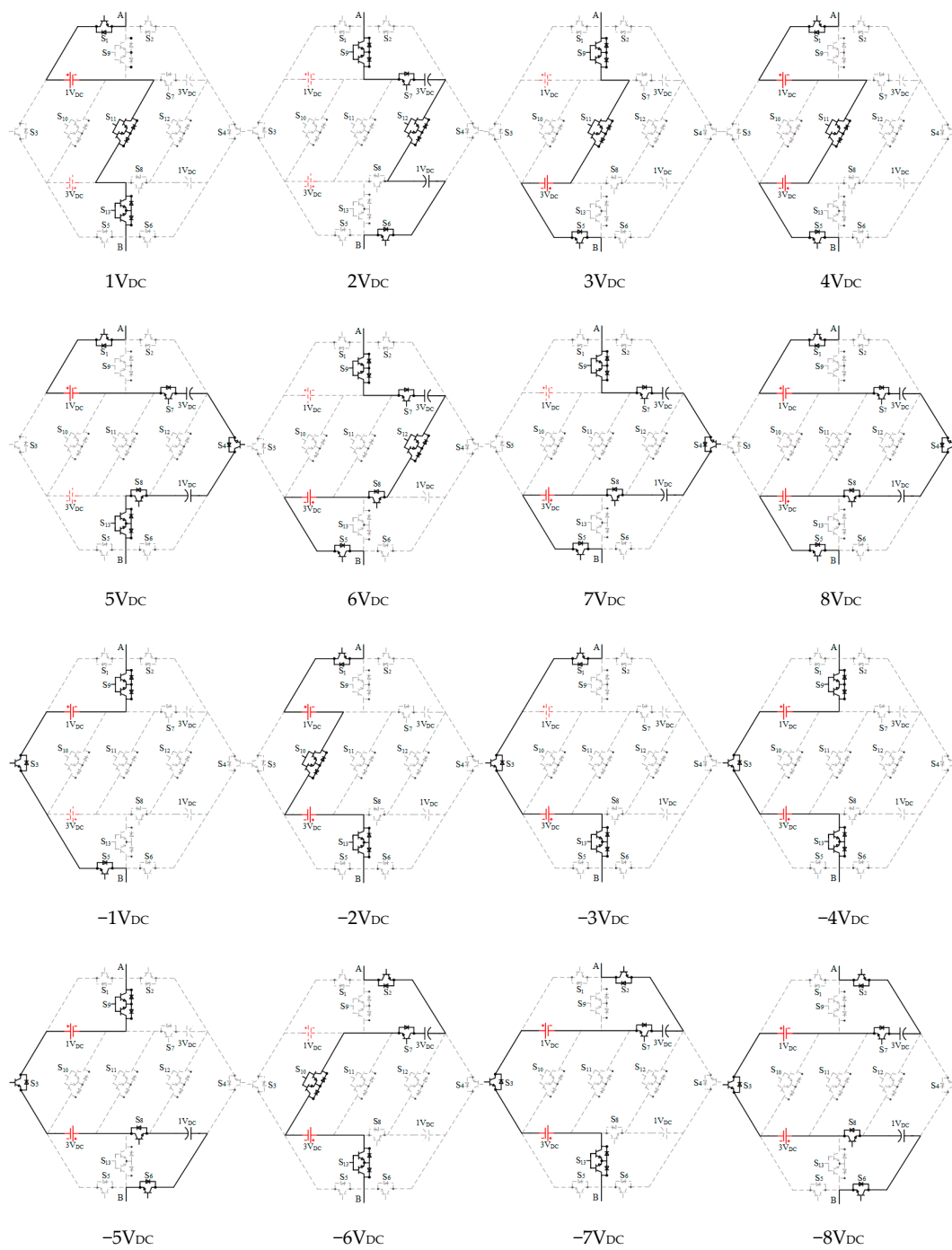
Figure 3. The switching paths of the proposed module.

Table 1. Sweating table.

		S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}	S_{12}	S_{13}
Positive level	$8V_{DC}$	1	0	0	1	1	0	1	1	0	0	0	0	0
	$7V_{DC}$	0	0	0	1	1	0	1	1	1	0	0	0	0
	$6V_{DC}$	0	0	0	0	1	0	1	1	1	0	0	1	0
	$5V_{DC}$	1	0	0	1	0	0	1	1	0	0	0	0	1
	$4V_{DC}$	1	0	0	0	1	0	0	0	0	0	1	0	0
	$3V_{DC}$	0	0	0	0	1	0	0	0	1	0	1	0	0
	$2V_{DC}$	0	0	0	0	0	1	1	0	1	0	0	1	0
	$1V_{DC}$	1	0	0	0	0	0	0	0	0	0	1	0	1
Negative level	$-1V_{DC}$	0	0	1	0	1	0	0	0	1	0	0	0	0
	$-2V_{DC}$	1	0	0	0	0	0	0	0	0	1	0	0	1
	$-3V_{DC}$	1	0	1	0	0	0	0	0	0	0	0	0	1
	$-4V_{DC}$	0	0	1	0	0	0	0	0	1	0	0	0	1
	$-5V_{DC}$	0	0	1	0	0	1	0	1	1	0	0	0	0
	$-6V_{DC}$	0	1	0	0	0	0	1	0	0	1	0	0	1
	$-7V_{DC}$	0	1	1	0	0	0	1	0	0	0	0	0	1
	$-8V_{DC}$	0	1	1	0	0	1	1	1	0	0	0	0	0
Num. of turning on per 1-cycle		6	2	5	4	4	6	5	5	7	4	4	4	6

Table 1 shows the on and off states of the switches at each level. It was clear that some pair switches could not be turned on simultaneously, such as (S_1, S_9); otherwise, the short circuit on DC sources was expectable. Additionally, the number of turning on per one cycle for each switch is shown in Table 1. As can be seen in the last row of Table 1, all switches had low operation frequency. In order to show this fact, S_2 and S_9 were selected as the switches with the lowest and highest number of turning on in one cycle to calculate the operation frequency. According to Table 1, S_2 and S_9 would be turning on 2 and 7 times in one cycle, respectively. By considering the fundamental frequency as 50 Hz, the operation frequency of a microprocessor for 32 steps would be calculated 1600 Hz. However, the operation frequency of S_2 and S_9 in one cycle was 100 Hz and 350 Hz, respectively. It was clear that these switches worked even lower than the overall microprocessor frequency (1600 Hz). It proved that all switches in the proposed module tolerated low-frequency stress.

Schematic output voltage levels associated with different switching states of the proposed module in one cycle are illustrated in Figure 4. Figure 4 also shows the schedule of the DC sources and capacitors, which were used for each level. Consequently, the proposed multilevel inverters, along with two unequal DC sources, could create 17-levels.
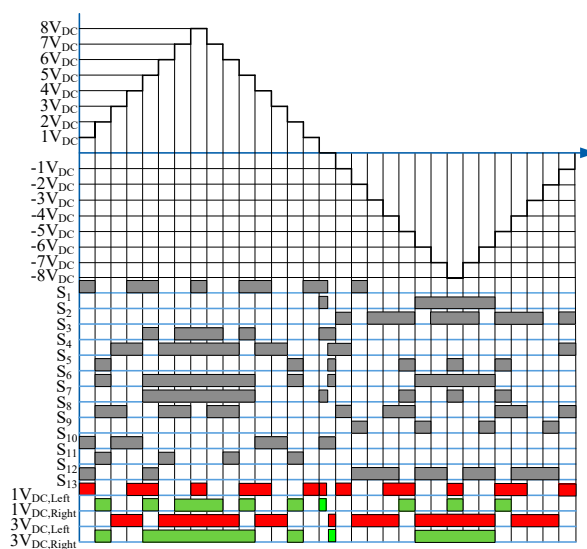
Figure 4. Switching pattern/schedule of DC links for the proposed inverter in one-cycle.

This module did not require any additional circuit to charge capacitors. According to Figure 4, capacitors were charged at level "zero". The module was designed based on the charging paths consisting of two loops for the charging of DC links that are shown in Figure 5. DC source with $1V_{DC}$ was charging 1Vc (Figure 5a), and DC source with $3V_{DC}$ was charging 3Vc (Figure 5b).
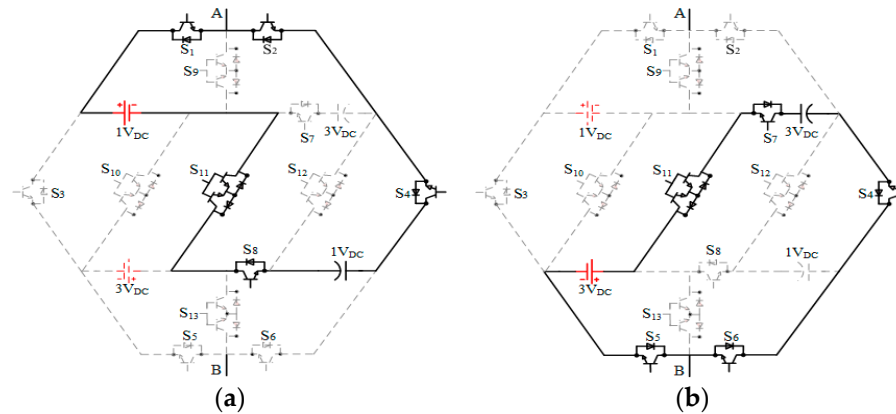

(a)   (b)

Figure 5. The charging paths of capacitors in the P-Type module, (**a**) charging for 1Vc; (**b**) charging for 3Vc.

Table 2 shows the equations of the module. The number of the semiconductor, DC sources, capacitors, drivers, and TSV (total standing voltages) based on the number of module units (n) were determined in the middle column and the number of output levels (NL), according to the mentioned variable parameters, were calculated in the last column. The symbol "[]" represents floor function.

Table 2. The equations of the proposed module.

	Based on the Number of Module Units	Based on the Number of Desired Levels
Levels	16n+1	N_L
Number of Switches	18n	$18\left[\frac{N_L-2}{16}+1\right]$
Number of Diodes	18n	$18\left[\frac{N_L-2}{16}+1\right]$
Driver	13n	$13\left[\frac{N_L-2}{16}+1\right]$
DC sources	2n	$13\left[\frac{N_L-2}{16}+1\right]$
Capacitors	2n	$2\left[\frac{N_L-2}{16}+1\right]$
TSV	57n	$57\left[\frac{N_L-2}{16}+1\right]$

According to Figure 3, the maximum magnitude of the blocking voltage was considered for each power switch. The total of all switch blocking voltages was introduced as TSV. The voltage standing on the switches in each level and the circuit study are presented in Figures 6 and 7, respectively. For each level, the voltage standing on each switch was separated by different colors, as shown in Figure 6. Low purple parts in Figure 6 confirms that the voltage stresses on switches were rare, and most of the area had low switch stress in the levels. Figure 7 demonstrates the voltage of switches on the circle graph, showing that the voltage standing in comparison with the total standing voltages was low in S_1, S_2, S_5, S_6, S_7, S_8, S_9, S_{11}, S_{12}, and S_{13}.
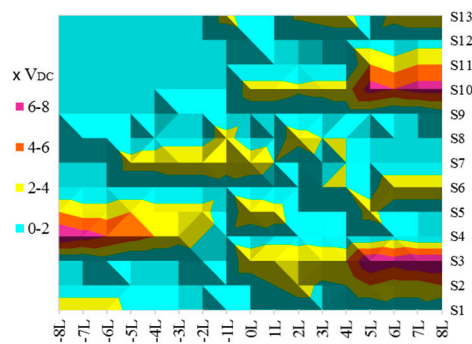
Figure 6. The surface graph of the voltage restrictions on the circuit for each level.
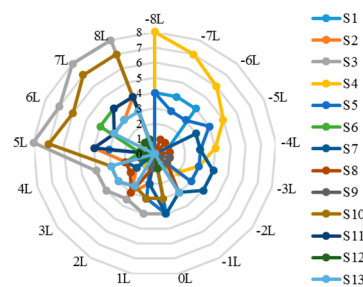

Figure 7. The circle graph of the voltage restrictions on each switch.

2.2. Module Extension

The modularity of the proposed model led to achieving more voltage levels. The cascade configuration was attractive for the medium and high voltage applications with cumulative DC links, such as solar Photovoltaic farms. The cascade connection of the two sequential units is shown in Figure 8. In this configuration, the unit produced 0, $\pm 1V_{DC}$, $\pm 2V_{DC}$, $\pm 3V_{DC}$, $\pm 4V_{DC}$, $\pm 5V_{DC}$, $\pm 6V_{DC}$, $\pm 7V_{DC}$, and $\pm 8V_{DC}$.
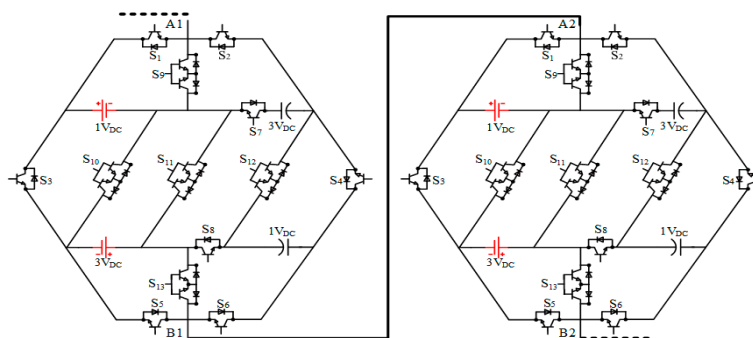

Figure 8. The cascade connection of the modular proposed multilevel.

Table 3 demonstrates that the combination of unit 1 and unit 2 created 16 positive levels, 16 negative levels, and zero level (total 33 levels). In Table 3, $u1 = \frac{V_{A1B1}}{V_{DC}}$, $u2 = \frac{V_{A2B2}}{V_{DC}}$. The extending of the proposed module as several units in series could make some redundant paths.

Table 3. Output levels for two modules to create 33 levels.

u2= \ u1=	−8	−7	−6	−5	−4	−3	−2	−1	0	1	2	3	4	5	6	7	8
−8	−16	−15	−14	−13	−12	−11	−10	−9	−8	−7	−6	−5	−4	−3	−2	−1	0
−7	−15	−14	−13	−12	−11	−10	−9	−8	−7	−6	−5	−4	−3	−2	−1	0	1
−6	−14	−13	−12	−11	−10	−9	−8	−7	−6	−5	−4	−3	−2	−1	0	1	2
−5	−13	−12	−11	−10	−9	−8	−7	−6	−5	−4	−3	−2	−1	0	1	2	3
−4	−12	−11	−10	−9	−8	−7	−6	−5	−4	−3	−2	−1	0	1	2	3	4
−3	−11	−10	−9	−8	−7	−6	−5	−4	−3	−2	−1	0	1	2	3	4	5
−2	−10	−9	−8	−7	−6	−5	−4	−3	−2	−1	0	1	2	3	4	5	6
−1	−9	−8	−7	−6	−5	−4	−3	−2	−1	0	1	2	3	4	5	6	7
0	−8	−7	−6	−5	−4	−3	−2	−1	0	1	2	3	4	5	6	7	8
1	−7	−6	−5	−4	−3	−2	−1	0	1	2	3	4	5	6	7	8	9
2	−6	−5	−4	−3	−2	−1	0	1	2	3	4	5	6	7	8	9	10
3	−5	−4	−3	−2	−1	0	1	2	3	4	5	6	7	8	9	10	11
4	−4	−3	−2	−1	0	1	2	3	4	5	6	7	8	9	10	11	12
5	−3	−2	−1	0	1	2	3	4	5	6	7	8	9	10	11	12	13
6	−2	−1	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14
7	−1	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
8	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

2.3. Comparative Study

Getting maximum voltage levels from the two DC sources is the specialty of the P-Type. It should be mentioned that there are few configurations with the exact two sources to be compared with the proposed multilevel inverter. Table 4 shows some similar new multilevel inverter configurations, as well as the proposed module in case of producing 17 output voltage levels. Some of these configurations could create the same levels with the only use of DC sources without any capacitors [12,18,24,25,35,36], and the presented module in [34] with two DC sources and some capacitors had a close configuration to the P-Type.

Table 4. Comparison of some modular multilevel inverter topologies.

	CHB [12]	[18]	[34]	[35]	[36]	[24]	[25]	Proposed Module
Number of Switches	$4\left[\frac{N_L-2}{2}+1\right]$	$8\left[\frac{N_L-2}{4}+1\right]$	$22\left[\frac{N_L-3}{16}+1\right]$	$9\left[\frac{N_L-2}{6}+1\right]$	$8\left[\frac{N_L-2}{8}+1\right]$	$10\left[\frac{N_L-2}{12}+1\right]$	$12\left[\frac{N_L-3}{16}+1\right]$	$18\left[\frac{N_L-2}{16}+1\right]$
Number of Diodes	$4\left[\frac{N_L-2}{2}+1\right]$	$8\left[\frac{N_L-2}{4}+1\right]$	$28\left[\frac{N_L-3}{16}+1\right]$	$11\left[\frac{N_L-2}{6}+1\right]$	$14\left[\frac{N_L-2}{8}+1\right]$	$10\left[\frac{N_L-2}{12}+1\right]$	$12\left[\frac{N_L-3}{16}+1\right]$	$18\left[\frac{N_L-2}{16}+1\right]$
Number of DC sources	$\left[\frac{N_L-2}{2}+1\right]$	$\left[\frac{N_L-2}{4}+1\right]$	$2\left[\frac{N_L-3}{16}+1\right]$	$\left[\frac{N_L-2}{6}+1\right]$	$\left[\frac{N_L-2}{8}+1\right]$	$4\left[\frac{N_L-2}{12}+1\right]$	$4\left[\frac{N_L-3}{16}+1\right]$	$2\left[\frac{N_L-2}{16}+1\right]$
Number of capacitors	-	$2\left[\frac{N_L-2}{4}+1\right]$	$6\left[\frac{N_L-3}{16}+1\right]$	$2\left[\frac{N_L-2}{6}+1\right]$	$3\left[\frac{N_L-2}{8}+1\right]$	-	-	$2\left[\frac{N_L-2}{16}+1\right]$
TSV [1] (xV_{DC})	$\left[\frac{N_L-2}{2}+1\right]$	$12\left[\frac{N_L-2}{4}+1\right]$	$88\left[\frac{N_L-3}{16}+1\right]$	$17\left[\frac{N_L-2}{6}+1\right]$	$17\left[\frac{N_L-2}{8}+1\right]$	$28\left[\frac{N_L-2}{12}+1\right]$	$39\left[\frac{N_L-3}{16}+1\right]$	$57\left[\frac{N_L-2}{16}+1\right]$
Negative level	With H-Bridge	With H-Bridge	With H-Bridge	With H-Bridge	With H-Bridge	Inherent	Inherent	Inherent

[1] Total standing voltages.

As shown in Table 4, to make a suitable comparison, various aspects, such as the number of DC sources, the number of semiconductors, the number of capacitors, the ability to generate negative voltage level, and TSV, were considered in terms of a number of voltage levels (NL). The formula for the other configuration is referred to from [37].

Figure 9 depicts the parameters, as mentioned in Table 4, versus voltage levels in different topologies. It was noticeable that one module generated some ranges of levels with the constant components. If more levels were required, it should be a connected module with the module in cascade connection. This is why Figure 9 was a staircase form. According to Figure 9a,b, it was prominent that the proposed module could attain maximum voltage levels from two DC sources with a lower number of semiconductors. The number of switches versus voltage levels is an important factor for MLIs. As a comparison only in the case of a number of semiconductors, [24,25,36] required a lesser number of

switches/diodes, but the number of DC sources should be considered. It was observed that the P-Type had significantly fewer semiconductors than [34] with the same number of DC sources. One of the promising advantages of the P-Type module was using lower DC sources except for the single source configurations (Figure 9c).
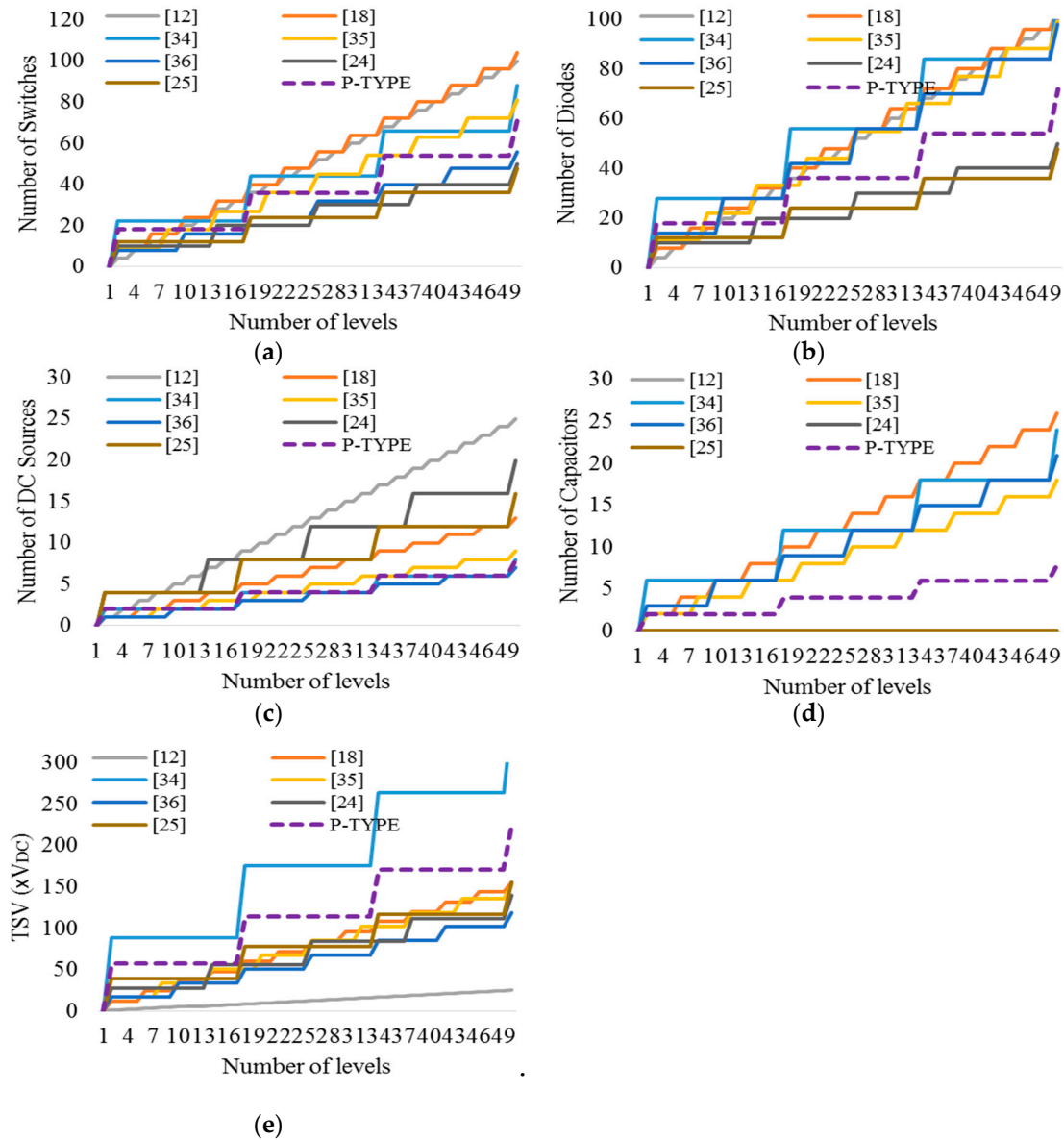

(a)

(b)

(c)

(d)

(e)

Figure 9. Comparative studies: The number of switches (**a**); The number of diodes (**b**); The number of sources (**c**); The number of capacitors (**d**); and TSV (**e**) in terms of the number of levels.

It is good to mention that P-Type needed the lowest number of capacitors in comparison with the module that used a capacitor as DC links (see Figure 9d). As shown in Figure 9e, the proposed module had a reasonable range of TSV. It could be referred to as Figure 6, which described the most of switches in the most of levels tolerating low switch stress (at the end of Section 2.1). It is noticeable that the presented topology and [24,25] had an inherent ability to generate negative voltage levels without any additional circuit. [12,18,34–36] could not have produced it without using full-bridge. This ability, along with lower components and switch stress, proved that the presented inverter could perform high in comparison with the other existing ones.

3. Nearest Level Control (NLC) Modulation Method

The nearest level control method (NLC) was used as a switching technique in the proposed multilevel [38]. This technique was applied in high voltage level converters to simplify and reduce the calculation of the processor. The modulation scheme and the control diagram are shown in Figure 10.
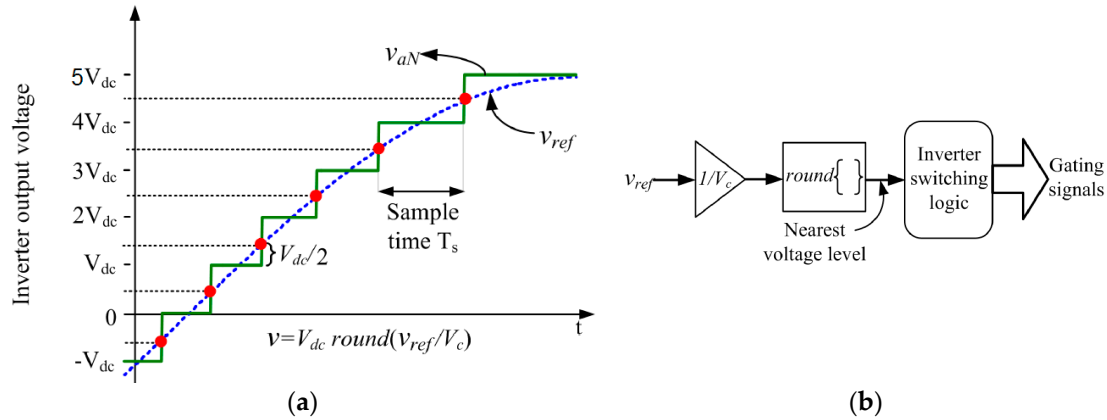

Figure 10. Nearest level control: (**a**) Waveform synthesis; (**b**) Control diagram.

According to Figure 10a, the controller sampled a point from the reference voltage (V_{ref}) and then rounded it to the nearest of the voltage level (V_{aN}). Each voltage level had a switching logic according to the switching table to change switches status (Figure 10b). The sampling was repeated for each sample time (T_s).

4. The Analysis of Capacitors Ripple

The capacitor voltage balancing is necessary to having constant voltage DC links in multilevel converters, which use capacitors as DC links. Since the capacitor voltage is kept constant, feeding the electrical load by MLIs would be guaranteed. Due to this fact, the voltage ripple of capacitors should be considered. To clarify this issue, ripple factor (RF) and figure factor (FF), as the main parameters in the ripple analysis of capacitors, are given by:

$$RF = \frac{V_{ac}}{V_{dc}} \tag{1}$$

$$FF = \frac{V_{rms}}{V_{dc}} \tag{2}$$

and,

$$V_{ac} = \sqrt{V_{rms}^2 - V_{dc}^2} \tag{3}$$

The ripple waveform is estimated to a sinusoidal waveform eight times bigger than the fundamental period. The maximum ripple is allowed to be less than 5% to obey this condition. Thus, the capacitor's drop voltages are not decreased than $0.95V_{max}$. The boundaries of the area of the integral are between 77° and 103°.

$$V_{dc} = \frac{1}{T} \int_{Start\ angle\ of\ ripple}^{End\ angle\ of\ ripple} f(\theta)\, d\theta = \frac{2 \times 1}{2\pi} \int_{77°}^{103°} V_{max} \sin \frac{\theta}{8}\, d\theta \tag{4}$$

$$V_{rms} = \sqrt{\frac{1}{T} \int_{Start\ angle\ of\ ripple}^{End\ angle\ of\ ripple} f^2(\theta)\, d\theta} = \sqrt{\frac{2 \times 1}{2\pi} \int_{77°}^{103°} V_{max}^2 \sin^2 \frac{\theta}{8}\, d\theta} \tag{5}$$

As can be observed from the parallel charging in Figure 5, V_{max} for C_1 was 10 and for C_2 was 30. The following result could be calculated from Equations (1)–(5): Vdc,C_1 = 9.65, Vdc,C_2 = 28.95,

Vrms,C_1 = 9.75, Vrms,C_2 = 29.2, Vac,C_1 = 1.39, Vac,C_2 = 4.17, and therefore: FFC_1 = 1.01, RFC_1 = 0.14 and FFC_2 = 1.01, RFC_2 = 0.14.

The described analysis showed that the voltages of the capacitors were standard to use in the proposed multilevel inverter.

Taking into account that the amounts of capacitors directly depend on load application, the proper determination of the capacitors resulted in having enough energy to supply the load during each periodic cycle on their levels (see Figure 4). First, the typical AC electrical load was assumed to consume 60 Wh (or 0.333 mW for one cycle = 20 millisecond). Based on Figure 4, the C_1 as a DC link supplied levels −5, −8, 2, 5, 7, and 8, meaning 0.062 mW for each one cycle, and levels −8, −7, −6, 2, 5, 6, 7, and 8 were supplied by C_2, meaning 0.094 mW for each one cycle.

On the other hand, to keep the DC link voltages at the constant level, the drop voltage of capacitors must be less than 5%. This requires drop voltage to satisfy $\Delta V_{C1} < 0.5$ and $\Delta V_{C2} < 1.5$.

The energy stored in capacitors can be calculated by the following equation:

$$E_C = \frac{1}{2} C \, \Delta V^2 \tag{6}$$

According to the above equation and mentioned conditions, considering $C_1 \geq 496$ μF and $C_2 \geq 84$ μF would admit that the capacitor values were sufficient to keep their voltages constant with standard ripple.

It is obvious, the values of the capacitors were selected to limit the voltage ripples. Selecting a higher capacitor as a DC link led to a reduction in the voltage ripples correspondingly.

5. Simulation Results

The proposed 17 levels of multilevel inverter had been simulated by MATLAB/SIMULINK. The output voltage of P-Type is shown in Figure 11a. The magnitude of each level (V_{DC}) was 10 volts to create a 50 Hz sinusoidal waveform. Figure 11b despises the harmonics spectrums as well. The THD (Total Harmonic Distribution) was calculated as 3.12% by FFT analysis for the waveform of Figure 11a, which was lower than the acceptable amount in the IEEE519 standard (THD% ≤ 8% and each order ≤ 5%).
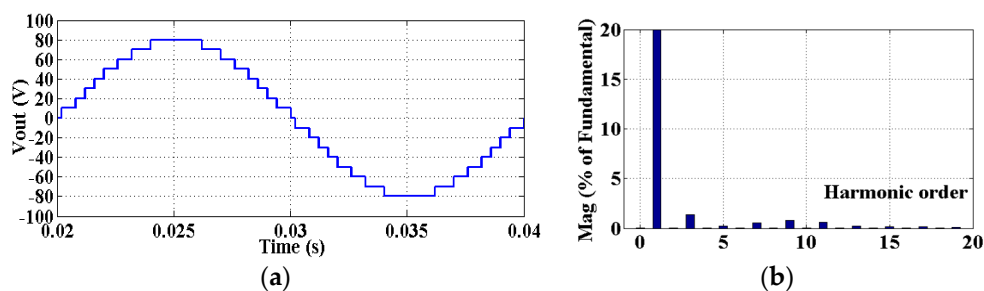

Figure 11. The simulated output voltage waveform of the proposed module: (**a**) Waveform; (**b**) Harmonics spectrums.

In order to indicate the performance of the modular mode, the cascade topology was simulated, and the results are depicted in Figure 12. The illustrated results confirmed the modular ability of proposed topology and its performance for creating 33 levels with THD = 1.54% for the cascade topology. IEEE519 was satisfied, as shown in Figure 12b, showing harmonic spectrums. Simulation results clarified the performance of the proposed module to create maximum output voltage waveforms with low harmonics.
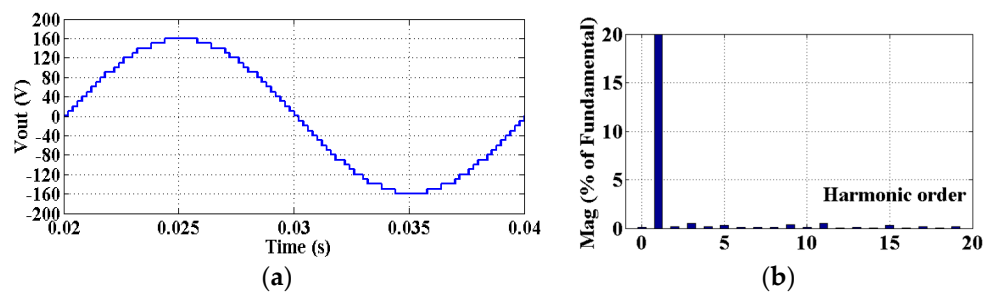
Figure 12. The simulated output voltage waveform of the first cascade topology (33 levels): (**a**) Waveform; (**b**) Harmonic spectrums.

6. Experimental Results

In order to verify the accurate performance of the proposed multilevel inverter and cascade topology connection for generating all output levels, an experimental prototype of the proposed module was built using IGBT12N60A4, Diode RHRP15120. The switching patterns of the different switches were generated by Microcontroller ATMEGA32, which provides on/off pulses for all switches. Based on Tables 1 and 3 and optocoupler-drivers (HCPL3120), the switches (MOSFET23N50E) were driven to create the sinusoidal waveform with a frequency of 50 Hz. Figure 13 depicts the experimental setup in the laboratory.
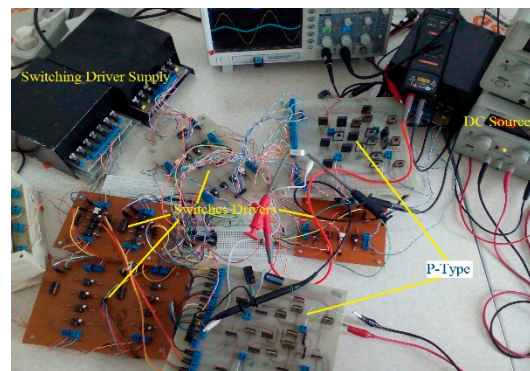
Figure 13. Experimental setup picture in the laboratory.

The experimental test on the setup system was performed, and each step of the voltage was considered 10 volts. Thus, the values of the used DC voltage sources were 10 (V) for $1V_{DC}$ and 30 (V) for $3V_{DC}$ in which $\pm8xV_{DC}$ and $\pm16xV_{DC}$ were generated for one module and cascade connection, respectively. The 17 levels and 33 levels MLI supplied the load with 40 Ω. Figure 14 shows the 50 Hz voltage and current sinusoidal waveforms of the proposed module for 17 levels. It should be mentioned that THD was 3.77% for 17 levels in the experimental test. Figure 15 contains results for 33 levels whose THD was 1.97%. The components were reduced directly affect the manufacturing cost. The new proposed multilevel inverter with a reduced number of DC sources was economical, and the smooth output voltage with low harmonic waveform made P-Type an interesting multilevel.
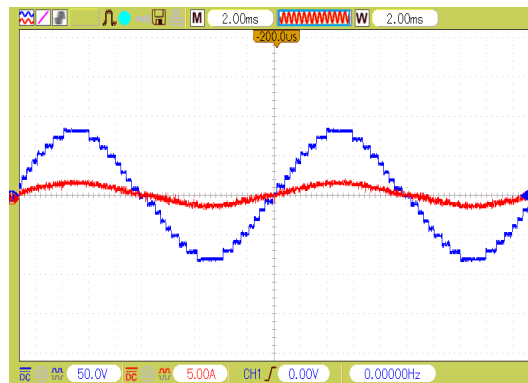
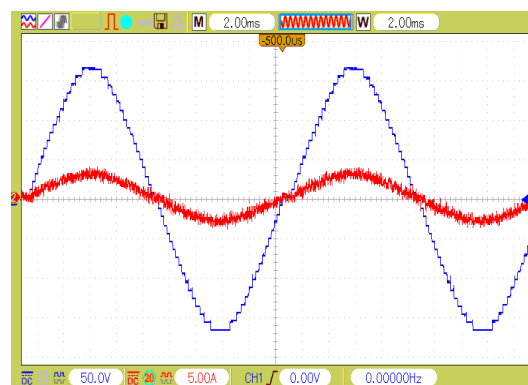**Figure 14.** The output voltage of experimental results for 17 levels (case 1).

Figure 15. The output voltage of experimental results for 33 levels (case 2).

Finally, the voltages of V_{C1} and V_{C2} that were on 10 and 30 volts are demonstrated in Figures 16 and 17, respectively. It was objective that the voltages of the capacitors were constant during the experiment.
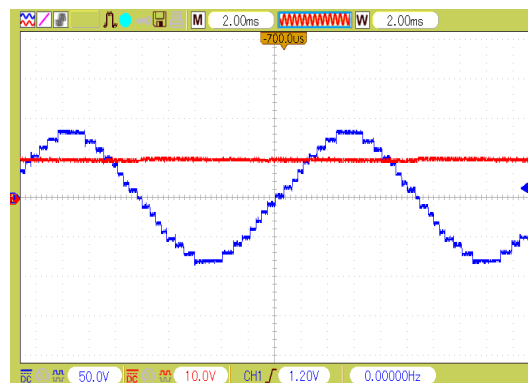

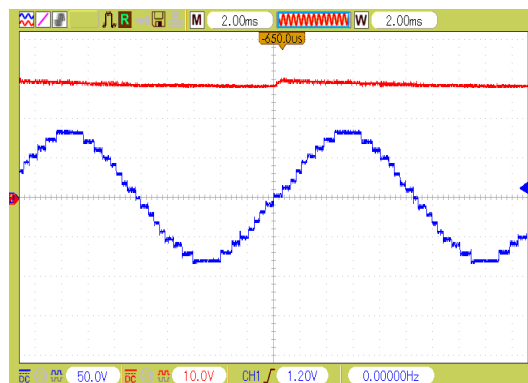**Figure 16.** The voltage of V_{C1} experimental results.

Figure 17. The voltage of V_{C2} experimental results.

7. Conclusions

In this paper, a new asymmetrical multilevel inverter module was introduced that is named P-Type. The configuration of P-Type produced 17 voltage levels by using only four DC links, including two DC sources and two capacitors. As a result, the maximum output voltage levels were produced at the output by the reduction of DC sources. By proper designing of the module, capacitors would be charged/discharged without any extra circuit. Modularity with low stress on semiconductors made the proposed module suitable for high power applications. The inherent negative voltage and low THDv were some main advantages of the proposed module. THDv% for one module was obtained as 3.12% and 3.77% in the simulation and experimental results, respectively, satisfying the harmonics standard (IEEE519). THDv% for cascade connection (two modules) was calculated to be 1.54% in simulation and 1.97% in experimental results. The experimental results proved the validity of the proposed module in producing the maximum output levels with a low amount of harmonics. The illustrated features of P-Type made it acceptable in power applications, which use unequal DC sources with ratio 3:1. The proposed module, with its all features, could be used in some applications with DC sources to supply AC loads. For example, it could be used in the solar farms with photovoltaic systems in which the unequal DC sources are accessible by the suitable connection of solar panels. Also, this system could be applied to other DC sources, such as fuel cells, batteries, etc.

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