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A 7.5–9 GHz GaAs Two-Channel Multi-Function Chip

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Abstract: Based on the 0.5 μm GaAs enhancement/depletion (E/D) Pseudomorphic High Electron Mobility Transistor (pHEMT) process, a 7.5–9 GHz two-channel amplitude phase control multi-function chip (MFC) was developed successfully. The chip was integrated with a 6-bit digital phase shifter, a 6-bit digital attenuator, and a single pole single throw (SPST) switch in each channel. A design for the absorptive SPST switch is deployed to optimize the return loss and control channel array calibration. In the 8 dB and 16 dB attenuation bit, a switched-path-type topology is employed in order to obtain a good flatness of attenuation characteristic and achieve low additive phase shift. A 27-bit serial-to-parallel converter (SPC) was introduced to decrease the control lines and pads of the chip, and the power consumption was less than 70 mW. The measurement result shows that the insertion loss is less than -13 dB and the return loss is better than -19 dB. In both channels, the 64-state root mean square (RMS) errors of the phase shifter is less than 2° and the RMS parasitic amplitude error is less than 0.2 dB. The RMS attenuation error is less than 0.45 dB and the RMS parasitic phase error is less than 2.4° . The size of the chip is $3.5\text{ mm} \times 4.5\text{ mm}$.

Keywords: Multi-function; two-channel; phase shifter; attenuator; absorptive SPST switch; serial-to-parallel converter

1. Introduction

Phased array technologies have been widely applied to satellite communications and defense systems to implement high-performance radar systems [1]. However, phased array radar systems consist of thousands of T/R modules which increase the systems' complexity and cost. By integrating several functions such as phase and gain control, driver amplifiers, and switches on a single multi-function chip [2], the sharp problem can be solved. Packing the multi-function chip (MFC) for compact and low cost T/R modules has already been realized in a phased array system [3]. With the development of advanced 3D integration technology, MFC chips are introduced to further improve the integration density of 3D microsystems in space applications [4].

In recent years, several GaAs multi-function chips have been presented, but higher integration implies a large number of control lines and pads to the chips [5–7]. By combination of serial-to-parallel converter on-chip, the number of control lines and pads can be substantially reduced [8,9]. Meanwhile, integrating multi-channels on one multi-function chip is beneficial as it decreases the system's size and cost. With high performance and high integration, the MFC chips must be promising.

According to actual application demand, a 7.5–9 GHz two-channel amplitude–phase control multi-function chip (MFC) was developed successfully via the 0.5 μm GaAs E/D pHEMT process. The variation of amplitude–phase in channel will influence the performance of T/R modules. Therefore, a single pole single throw (SPST) switch was designed to control array calibration, and an absorptive

topology was selected to optimize the return loss. In order to achieve extended bandwidth, good attenuation flatness, and low additive phase shift, a switched-path-type topology was employed in 8 dB and 16 dB attenuation bit. It is complex and difficult to assemble the T/R modules due to the existence of numerous pads. A 27-bit serial-to-parallel converter was integrated to decrease the control pads, which also reduces the size and cost of T/R modules. To the best of our knowledge, the insertion loss, phase error, attenuation error, and return loss of the presented MFC represent state-of-art performances.

2. Circuit Design

Based on the 0.5 μm GaAs E/D pHEMT process, a multi-function chip (MFC) is designed; the diagram is shown in Figure 1. The MFC comprises two channels (CH); each one consists of a 6-bit digital phase shifter (PHS), a 6-bit digital attenuator (ATT), and a single pole single throw (SPST) switch. The phase and the amplitude of RF signals are controlled by the PHS and ATT. The on–off state of each channel is chosen by an SPST switch. The 26-bit serial-to-parallel converter (SPC) is needed to control RF Field Effect Transistors (FETs) of the PHS, ATT, and SPST switch in two channels, and another bit is used to output differential voltages to control an off-chip switch. In total, a 27-bit serial-to-parallel converter is designed to decrease the control pads of the chip.

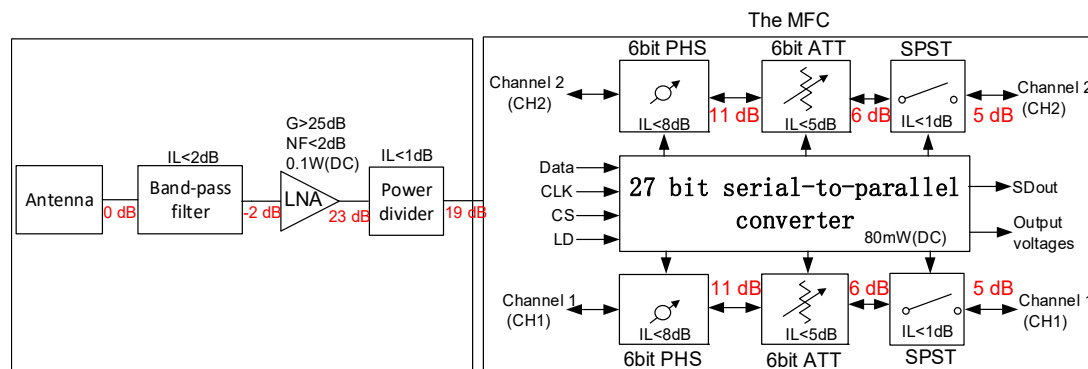


Figure 1. The diagram of the actual application.

The summary of the link budget analysis is also shown in Figure 1. Based on the demand of the actual application, no additional driver amplifiers need to be designed in the MFC. The total gain of the receiving channel is sufficient with the introduction of the Low Noise Amplifier (LNA) at the RF frontend. On the other hand, based on the 0.5 μm GaAs E/D pHEMT process, the noise performance of LNA is no longer competitive, so that the LNA at the RF frontend is not integrated in the MFC and is designed in another process.

2.1. Absorptive SPST Switch Design

In many applications, reflective switches are not suitable due to the significant standing waves introduced between components [10]. In this MFC, an absorptive SPST switch has been designed to control array calibration of channel; the structure is shown in Figure 2. In this design, when V_T is 0 V, the SPST switch is in the on-state. A two-stage series-shunt structure is adopted to achieve high isolation performance. When V_T is -3 V, the SPST switch is in the off-state. Two $50\ \Omega$ absorptive resistors are used to decrease the return loss. A 45 dB isolation and a 19 dB return loss have been achieved in these two ways. The parameters of SPST switch design are shown in Table 1.

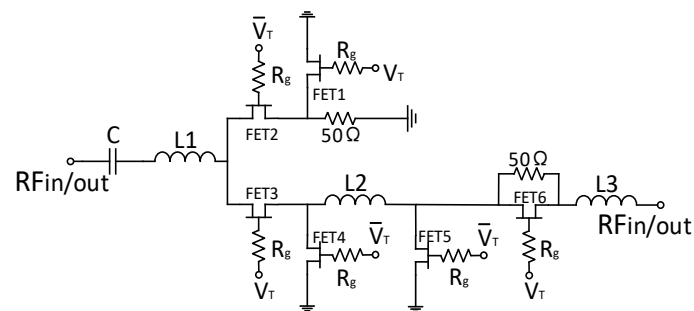


Figure 2. The structure of the absorptive single pole single throw (SPST) switch.

Table 1. The parameters of SPST switch design.

Parameter	Value	Parameter	Value
FET1	$4 \times 45 \mu\text{m}$	FET6	$8 \times 80 \mu\text{m}$
FET2	$6 \times 45 \mu\text{m}$	C	2.59 pF
FET3	$4 \times 80 \mu\text{m}$	L1	632 pH
FET4	$6 \times 45 \mu\text{m}$	L2	605 pH
FET5	$6 \times 65 \mu\text{m}$	L3	571 pH

2.2. Attenuator Design

The attenuator is comprised of six attenuation bits which contain 64 states. The maximum attenuation is 31.5 dB, in 0.5 dB steps. Figure 3 shows the schematic of the attenuator; the order of 6-bit attenuation is ranked by the performance of input and output return loss. The on-state (0 V) and off-state (−3 V) of each FET is controlled by the gate bias voltage that is provided by the serial-to-parallel converter.

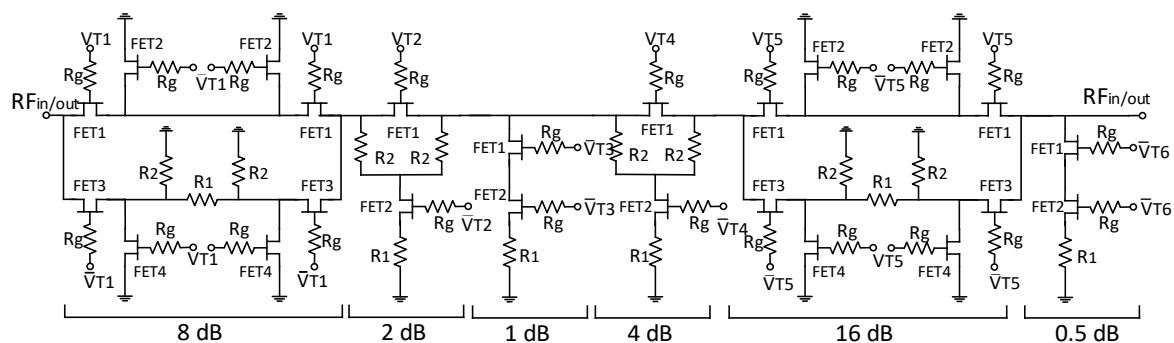


Figure 3. The schematic of the 6-bit digital attenuator.

In the 0.5 dB and 1 dB attenuation bits, a simplified T-type network with series-FETs topology is used; the topology introduces a low insertion loss. Two dB and 4 dB bits adopt the bridge-T-type structure, which has great terminal matching characteristics. For the large attenuation of the 8 dB and 16 dB bits, parasitic parameters of FETs would bring more additive phase shift and deteriorate the flatness of the attenuation characteristic. Therefore, switch-path-type topology is employed. The required attenuation is obtained by switching the signal between a long micro-strip and a pi-type resistor network. By adjusting the length of the micro-strip between the two paths, the additive phase shift can be decreased. Meanwhile, a good flatness of attenuation is achieved by using two single pole double throw (SPDT) switches, which provide high isolation between the reference and attenuation states.

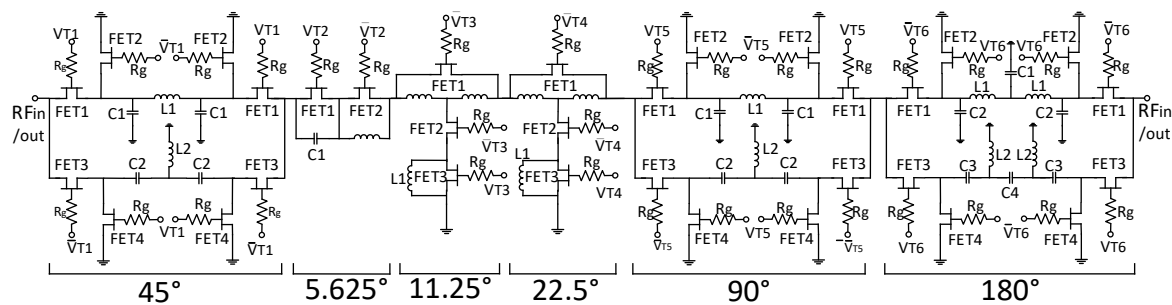
The parameters of attenuator design are shown in Table 2.

Table 2. The parameters of attenuator design.

Unit Cell	Parameter					
	FET1 (μm)	FET2 (μm)	FET3 (μm)	FET4 (μm)	R1 (Ohm)	R2 (Ohm)
0.5 dB	2×50	2×50	-	-	595	-
1 dB	2×50	2×50	-	-	204	-
2 dB	4×80	4×45	-	-	192	7
4 dB	6×50	2×25	-	-	43.5	11.5
8 dB	6×50	4×25	4×45	4×25	76	15
16 dB	6×45	2×50	4×50	4×50	38	16

2.3. Phase Shifter Design

The schematic of the 6-bit phase shifter is illustrated in Figure 4. The 6-bit phase shifter provides 64 states in steps of 5.625° , which corresponds to phase shifts of 45° , 5.625° , 11.25° , 22.5° , 90° , and 180° . The major consideration for the order of the 6-bit phase shifter is the input and output characteristic. Each FET's on-state (0 V) and off-state (-3 V) is controlled by the gate bias voltage, which also is provided by the serial-to-parallel converter.

**Figure 4.** The schematic of the 6-bit digital phase shifter.

Series FETs filter topology is applied in 5.625° bit, which causes low insertion loss. The bridge-T-type topology is selected for the 11.25° and 22.5° bits. The FETs' parasitic parameters are absorbed as phase shift element, and the topology has a good phase shift flatness. For the 45° , 90° , and 180° bits, switched filter topology is implemented. Between two SPDT switches, one path is constructed using a high-pass filter network which causes signal phase lead, and the other path is constructed using a low-pass filter network which makes signal phase lag. The necessary phase shift is obtained by switching the signal between the two paths. Although the use of two SPDT switches introduces higher insertion loss compared to other bits, the implementation of high phase shift values using this topology provides a low amplitude imbalance, good match characteristics, and phase shifter flatness.

The parameters of phase shifter design are shown in Table 3.

Table 3. The parameters of phase shifter design.

Unit Cell	Parameter									
	FET1 (μm)	FET2 (μm)	FET3 (μm)	FET4 (μm)	L1 (nH)	L2 (nH)	C1 (pF)	C2 (pF)	C3 (pF)	C4 (pF)
5.625°	4×80	8×60	-	-	-	-	2.9	-	-	-
11.25°	6×60	6×70	6×20	-	3	-	-	-	-	-
22.5°	8×100	6×55	6×85	-	1.2	-	-	-	-	-
45°	8×45	2×30	8×45	2×20	0.8	1.4	0.04	2	-	-
90°	6×55	2×30	6×55	2×25	1	1.4	0.12	0.9	-	-
180°	6×70	2×15	6×70	2×20	1	1.3	0.265	0.1	1.1	0.42

2.4. Serial-to-Parallel Converter Design

Based on the 0.5 μm GaAs E/D pHEMT process, which has both enhancement/depletion mode pHEMTs on one substrate, a 27-bit serial-to-parallel converter is designed. The depletion mode (D-mode) pHEMT works as a load to constrain the current, while the enhancement mode (E-mode) pHEMT works as a switch to achieve logic function. In contrast to other logic families (e.g., two-phase dynamic FET logic (TDFL), source-coupled FET logic (SCFL), pseudo-complementary FET logic (PCFL), feedback FET logic (FFL), etc.), the direct-coupled FET logic (DCFL) is the most commonly used logic style and is chosen in this design, which has compact topology and low power dissipation [11].

The circuit structures of NO and NAND are shown respectively in Figure 5a,b, which consists of $1 \times 5 \mu\text{m}$ size E/D-mode pHEMT. Shift and hold registers are composed of a D-flipflop, which contain 4 NAND blocks and 4 NO blocks, as shown in Figure 5c.

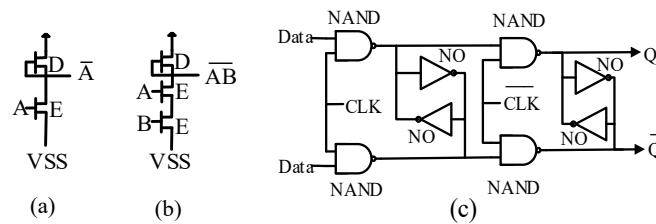


Figure 5. (a) NO circuit structure, (b) NAND circuit structure, (c) D-flipflop circuit structure.

As shown in Figure 6, the serial-to-parallel converter contains 4 TTL-direct-coupled FET logic (DCFL) level shifters, 27 shift registers, 27 hold registers, and 27 output buffers. The level shifter converts the external TTL signals into internal DCFL signals. The shift registers transform the DATA into binary numbers where the 1-state stands for 0 V while the 0-state is -3 V. The shift registers shift the 0/1-state to next shifter register when CLK falling edge comes. When the LD signal arrives, hold registers receive the parallel data from the shifter register and transmit to the output buffers, which provide differential voltages to RF FETs. The power consumption of the 27-bit serial-to-parallel converter is less than 70 mW, while -5 V and 5 V voltages are supplied. The power consumption ratio of level shifts; output buffers, shift registers, and hold registers are around 1:15:35:35. The serial DATA out bit stream (SDout) is available and can be cascaded to a second chip or be used to check the working state of the serial-to-parallel converter. The integration of the serial-to-parallel converter decreases the number of control pads from 54 to 9.

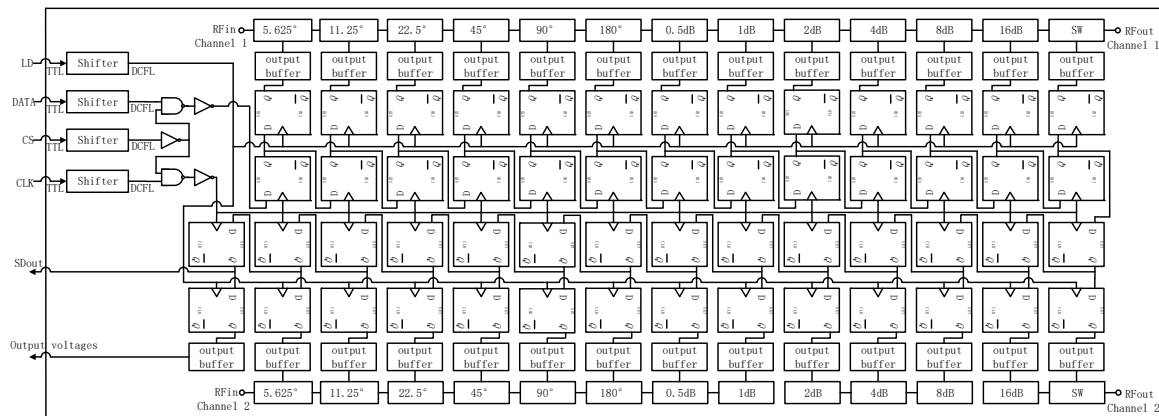


Figure 6. The schematic of the digital circuit.

3. Measurement Results

Figure 7 shows the photograph of the two-channel multi-function chip which is fabricated by the 0.5 μm GaAs E/D pHEMT process. The chip size is 3.5 mm \times 4.5 mm. On-wafer measurements

are carried out for the performance characterization. A signal generator (NI-PXI) is employed to provide appropriate digital input waveform with a clock frequency of 10 MHz. The MFC is tested by vector network analyzer (Agilent PNA 5224A, Agilent Technologies Inc., Santa Clara, USA) using Ground-Signal-Ground (GSG) co-planar microwave probes pitch on probe station [12].

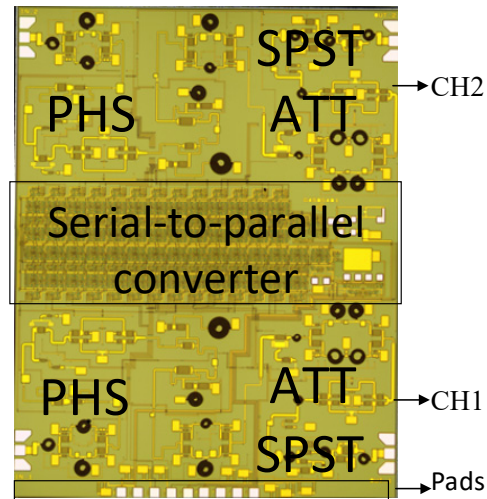


Figure 7. Photograph of the fabricated multi-function chip.

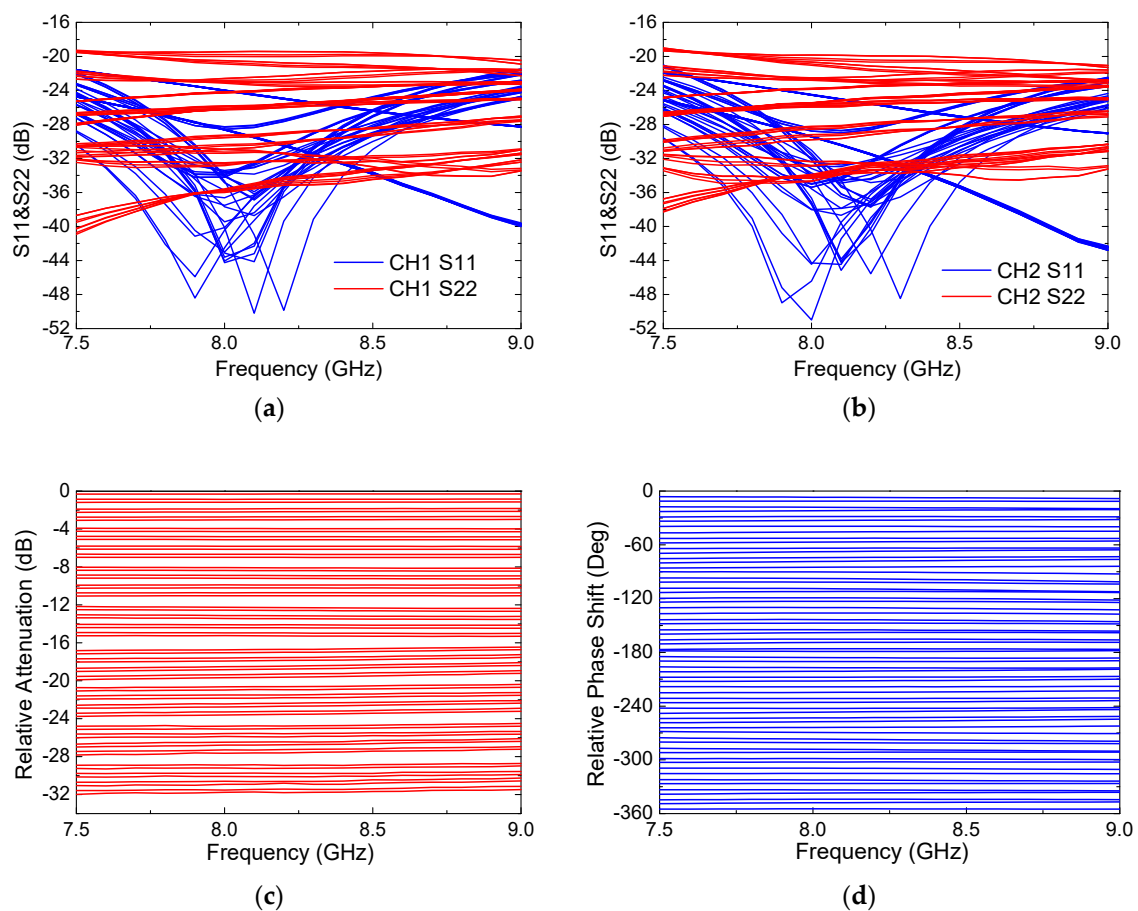


Figure 8. Cont.

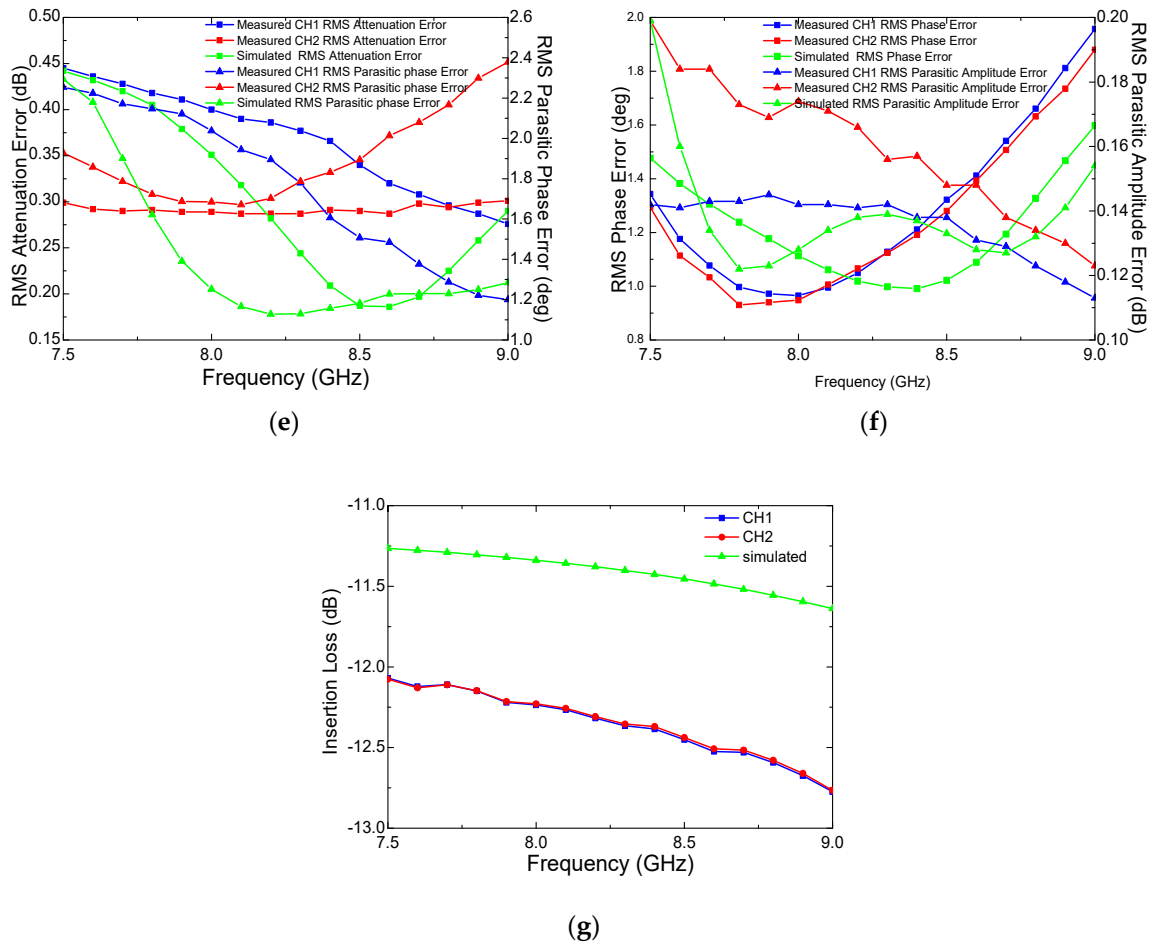


Figure 9. (a) Measured channel 1 (CH1) input and output return loss of all states, (b) measured channel 2 (CH2) input and output return loss of all states, (c) measured relative attenuation of all states, (d) measured relative phase shift of all states, (e) measured and simulated CH1 and CH2 root mean square (RMS) error of attenuation and parasitic phases, (f) measured and simulated CH1 and CH2 RMS error of phase and parasitic amplitude, (g) measured and simulated CH1 and CH2 insertion loss.

As shown in Figure 9a,b, the input and output return losses of MFC are more than 19 dB in both channels. The attenuator and phase shifter exhibit good flatness of relative attenuation and relative phase shift, respectively, in the frequency range from 7.5 to 9 GHz (Figure 9c,d). In Figure 9e, measured root mean square (RMS) attenuation error of <0.45 dB and RMS parasitic phase error of <2.4° is shown at all 64 states. Figure 9f shows <2° RMS phase error and <0.2 dB RMS parasitic amplitude error measured for the phase shifter. The trend of measured results are almost in accord with simulated results for ATT and PHS. In Figure 9g, <13 dB insertion loss is achieved, and the difference between measured and simulated results may be caused by process model accuracy.

Table 4 summarizes the performance comparison of this work with other published MFCs working in close frequency ranges. Characteristics including insertion loss, RMS phase error, RMS attenuation error, and return loss are better than the previous reported MFCs. This work is also integrated with two channels and a serial-to-parallel converter on a single MFC chip, which has the benefit of decreasing the system's size and cost. By applying new technologies like the 0.18 μm GaAs E/D pHEMT process, the size of MFC could reach $4 \times 3.7 \text{ mm}^2$ [8]. However, comparing with the 0.5 μm GaAs E/D pHEMT process, which is commonly used for the MFC designs in X-band, the cost of the 0.18 μm process is much larger. Compared with other published MFCs with the same 0.5 μm process, our design shows higher integration, the size of which is much smaller than the average $4 \times 5 \text{ mm}^2$ [13]. Furthermore, the $3.5 \times 4.5 \text{ mm}^2$ size of our MFC successfully approaches the above $4 \times 3.7 \text{ mm}^2$ fabricated by the

new 0.18 μm technology. The frequency band 7.5–9 GHz of the MFC is chosen for a real application of narrow-band data transmission within 8–8.5 GHz.

Table 4. Performance comparison of relevant multi-function chip (MFC).

Ref.	Process	Frequency (GHz)	PHS/ATT ¹ (number of bits)	IL (dB)	RMS phase error (deg)	RMS ² atten. Error (dB)	RL (dB)	Function	Size (mm ²)
[8]	0.18 μm GaAs pHEMT ³	8.6–10	6/6	NA	<6	<1	>16	with SPC ⁴ two-channel	4.0 \times 3.7
[13]	0.5 μm GaAs pHEMT	8.5–10.5	6/6	<16	<2.5	<0.5	>12	with SPC two-channel	5.5 \times 4.0
[14]	0.13 μm CMOS	7.9–9.6	4/3	NA	<6	<0.5	>10	no SPC two-channel	2.9 \times 3
[15]	0.13 μm CMOS	8.5–10.5	6/5	<13.2	<4.3	<0.33	>11	no SPC one-channel	2.06 \times 0.58
[16]	0.13 μm SiGe BiCMOS	9–11	5/NA	<13	<3.8	NA	>8	no SPC two-channel	5.2 \times 3.0
[17]	65 nm CMOS	8–10.5	6/6	NA	<4	<0.5	>15	no SPC one-channel	3.92 \times 2.44
[18]	0.25 μm GaAs pHEMT	8–11	6/5	NA	<10	NA	>15	with SPC two-channel	4.0 \times 5.0
This work	0.5 μm GaAs pHEMT	7.5–9	6/6	<13	<2	<0.45	>19	with SPC two-channel	3.5 \times 4.5

¹ PHS: Phase shifter; ATT: Attenuator. ² RMS: Root Mean Square. ³ GaAs pHEMT: GaAs Pseudomorphic High Electron Mobility Transistor. ⁴ SPC: Serial-to-Parallel Converter.

4. Conclusions

In this letter, a high-performance 7.5–9 GHz two-channel multi-function chip integrated with a serial-to-parallel converter is presented. A design of the absorptive SPST switch is deployed to optimize the return loss and control channel array calibration. In the 8 dB and 16 dB attenuation bits, a switched-path-type topology is adopted in order to obtain a good flatness of attenuation characteristic and a low additive phase shift. The control pads are reduced from 54 to 9 by integrating the serial-to-parallel converter. The measurement result shows that the two channels of MFC have <13 dB insertion loss at reference state, and >19 dB return loss at all states. An RMS attenuation error of <0.45 dB and an RMS parasitic phase error of >2.4° are obtained for the attenuator. An RMS phase error of <2° and an RMS parasitic amplitude error of <0.2 dB are achieved for the phase shifter. Good return loss, high attenuation, and phase shift accuracy are achieved in this two-channel multi-function chip.

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