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Reduced Active Components Count Electronically Adjustable Fractional-Order Controllers: Two Design Examples

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Abstract: This paper deals with fractional-order controller implementations, which can be constructed by electronically controlled building blocks fully integrated on a single chip. The proposed DC motor controller structure offers 50% reduction of the active components count, compared to the corresponding already published counterpart. The proposed liquid level of the two-interacting-tank controller scheme is the first one in the literature offering the aforementioned features. Simulation results, based on the 0.35 μm Austria Mikro Systeme technology process, confirm the correct operation of both proposed controllers.

Keywords: DC motor; two-tank system; fractional-order controller; tuning; implementation

1. Introduction

In this paper, we present a fully integratable implementation form of the fractional-order controllers and their application to the DC motor control and two-tank system, respectively, using a non-integer calculus technique.

The transfer function of a fractional-order proportional-integral-derivative ($PI^{\lambda}D^{\mu}$) controller, with λ, $\mu > 0$ being the orders of integration and differentiation, is the following:

$$C(s) = K_p + \frac{K_i}{s^{\lambda}} + K_d s^{\mu} = \frac{K_d s^{\mu+\lambda} + K_p s^{\lambda} + K_i}{s^{\lambda}}, \quad (1)$$

where K_p is the proportional gain, K_i is the integration constant, K_d is the differentiation constant, and λ, μ are the orders of integration and differentiation, respectively [1].

Inspecting (1), it is readily obtained that $PI^{\lambda}D^{\mu}$ controllers have five parameters, instead of three parameters offered by their integer-order counterparts (i.e., PID controllers), making them very attractive from the implementation point of view [2]. It must be mentioned at this point that there are many fractional-order controllers/compensators, as for example [3]: fractional-order controller in traditional PID structure, CRONE controller, TID compensator, lead-lag compensator, and so on.

Due to the absence of commercially available fractional-order capacitors [4,5], it is difficult to implement fractional-order controllers through the substitution of conventional capacitors by fractional-order capacitors. Therefore, the implementation of fractional-order controllers can be performed through the utilization of RC networks [6–15], which approximate the behavior of the

fractional-order capacitors. This is an easy design procedure, but the absence of tunability of the characteristics of the approximated fractional-order capacitors limits its employment only in cases where elements with pre-defined characteristics are required [7,10]. Another way for implementing fractional-order controllers is through the approximation of the transfer functions of the required fractional-order differentiation and/or integration stages. This is performed by expressing these transfer functions as rational integer-order transfer functions, which are then implemented using multi-feedback structures [16].

DC motor is a power actuator, which converts direct current electrical energy into rotational mechanical energy. The DC motors are still often used in industry and in numerous control applications, robotic manipulators and commercial applications such as disk drive, tape motor as well. Considering an armature-controlled DC motor in which a constant field current is been utilized, a fractional-order $I^{\lambda}D^{\mu}$ controller for controlling the rotation speed has been developed in [17], which offers resistorless implementation, electronic tunability, and capability of monolithic implementation. All these features are originated from the employment of Operational Transconductance Amplifiers (OTAs) as active elements. On the other hand, the active component count and, therefore, the power consumption, are relatively high in this implementation. Owing to the fact that increased number of active elements means increased power dissipation, the reduction of the active component count is very important in nowadays applications, where there is demand for reduced power systems. In order to overcome the aforementioned obstacle, a novel $I^{\lambda}D^{\mu}$ controller topology is introduced in this work, where the most attractive achievement is that the number of active elements is significantly reduced. This is achieved by expressing the transfer function of the fractional-order integrator as a product of the transfer functions of a fractional-order differentiator and an integer-order integrator. In addition, the proposed structure still offers the benefit of the electronic adjustment of its characteristics and this is very important because possible deviations in frequency characteristics caused by the imperfections of the employed active cells can be easily minimized through appropriate adjustment of the corresponding dc bias currents.

The control of liquid level in tanks as well as its flow between tanks is a very important problem in industry. This is originated from the fact that most of industrial application of liquid level control is hazardous in chemical petroleum, mixing treatment industries, pharmaceutical and food processing industries. Therefore, the development of the corresponding controllers has a significant practical value. Towards this goal, a novel PI^{λ} controller suitable for controlling the liquid level into a two tank system is introduced, where the employed active blocks for implementing the required fractional-order integrator were current-mirrors, while the gain stage was implemented by a simple trans-linear loop. The resulting benefit is that the transistor count is minimized and, consequently, the dc power consumption is minimized. Originating from the electronic tuning capability of the controller, the same core can be used for implementing controllers with different characteristics, providing design versatility and flexibility.

This article is organized as follows: the proposed fractional-order DC motor controller design is presented and evaluated in Section 2. In Section 3, an example of control of two interactive tanks system, new controller topology, and simulation results are presented. Section 4 concludes this article with some ideas for further work.

2. Proposed Fractional-Order DC Motor Controller

2.1. Proposed Concept for Controller Implementation

The mini DC motor with model number PPN-13KA12C, depicted in Figure 1, is suitable for small robots, remote control applications, CD/DVD mechanics, and so on [18]. The dynamics of the DC motor are described by the transfer function $G_{DCM}(s)$ given by (2)

$$G_{DCM}(s) = \frac{0.08}{s\,(0.05s+1)}\,. \tag{2}$$

Assuming that the phase margin of the controller-plant system is $\Phi_m = 45^\circ$, then the transfer function of the controller becomes

$$C(s) = 12.5\, s^{-0.5} + 0.625\, s^{0.5}\,. \tag{3}$$

Comparing (1) and (3), it is readily obtained that the integration and differentiation constants are: $K_i = 12.5$, $K_d = 0.625$, respectively, while the orders of integration and differentiation are both equal to 0.5 (i.e., $\lambda = \mu = 0.5$).

In order to make a correspondence between the integration constant K_i and differentiation constant K_d, with the associated time-constants, the expression in (3) is alternatively expressed as

$$C(s) = (\tau_i\, s)^{-\lambda} + (\tau_d\, s)^{\mu}\,, \tag{4}$$

where variables τ_i and τ_d represent the time-constant of the integrator and differentiator, respectively. Comparing (3) and (4), it is concluded that: $K_i = \tau_i^{-\lambda}$ and $K_d = \tau_d^{\mu}$. Consequently, the corresponding time-constants will be $\tau_i = 6.4$ ms and $\tau_d = 391$ ms, respectively, while the unity-gain frequency of the integrator (calculated according to the formula $\tau = 1/\omega$) will be 24.9 Hz, and for the differentiator 410 mHz.

The functional block diagram that has been followed in [17] for implementing a fractional-order DC motor $\mathrm{I}^{\lambda}\mathrm{D}^{\mu}$ controller is presented in Figure 2. The proposed functional block diagram, in order to reduce the circuit complexity, is depicted in Figure 3. According to this, instead of having separate integration and differentiation paths, the required integration function is implemented through the cascade connection of a fractional-order differentiator with an integer-order integrator and the transfer function of the controller becomes

$$C(s) = \left(\frac{\tau_d^{\mu}}{\tau_0}\right) s^{-(1-\mu)} + (\tau_d\, s)^{\mu}\,. \tag{5}$$

Comparing (4) and (5), it is concluded that the integration constant will be given by (6)

$$K_i = \frac{\tau_d^{\mu}}{\tau_0}\,, \tag{6}$$

and, thus, the value of the time-constant of the integer-order integrator τ_0 will be equal to 50 ms. The number of OTAs, required for implementing the summation stage, is also decreased thanks to the employed configuration. This concept is also useful for minimizing the spread of capacitors and/or bias currents in the cases where large values of the order of integration/differentiation are required [19].

Figure 1. Photo of the mini DC motor.

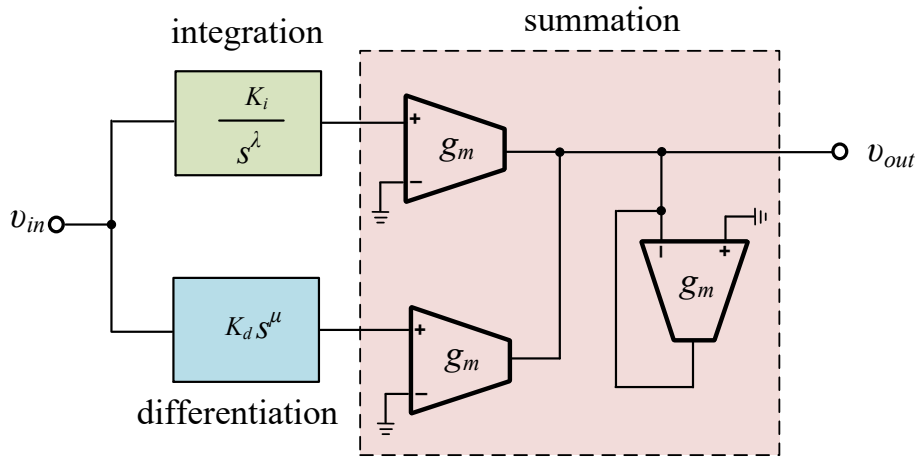


Figure 2. Typical functional block diagram for implementing a DC motor controller.

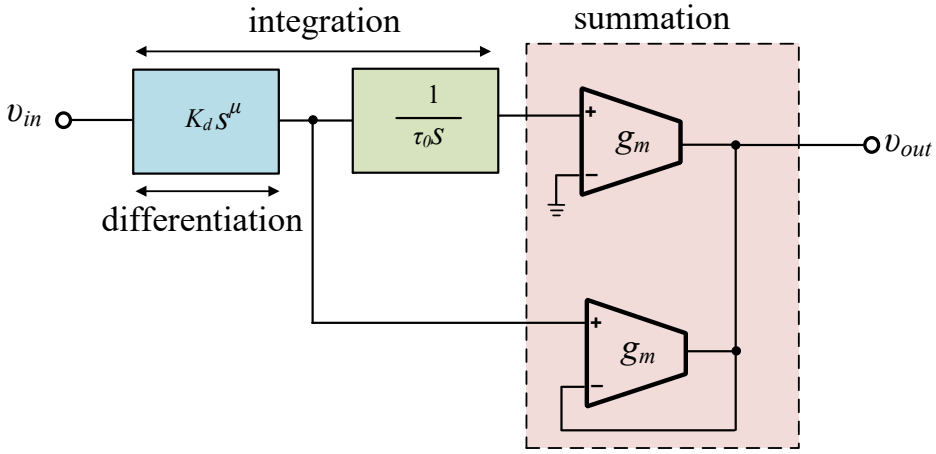


Figure 3. Proposed functional block diagram of the controller in order to reduce the active component count.

2.2. Circuit Implementation of Controller

Using the 5th–order Oustaloup's approximation [20,21], the rational transfer function which approximates (7) in the range $[10^{-3}$ rad/s, 10^{+3} rad/s], is

$$0.625\,s^{0.5} \approx \frac{19.8\,s^5 + 2656\,s^4 + 2.2\times10^4\,s^3}{s^5 + 535s^4 + 1.7\times10^4 s^3 + 3.4\times10^4 s^2 + 4249s + 31.6} + \frac{1.1\times10^4\,s^2 + 334.3\,s + 0.62}{s^5 + 535s^4 + 1.7\times10^4 s^3 + 3.4\times10^4 s^2 + 4249s + 31.6}, \tag{7}$$

and can be implemented using the OTA-C topology depicted in Figure 4. The transfer function is given by

$$H(s) = \frac{G_5 s^5 + \left(\frac{G_4}{\tau_1}\right) s^4 + \cdots + \left(\frac{G_0}{\tau_1\cdot\tau_2\ldots\tau_5}\right)}{s^5 + \left(\frac{1}{\tau_1}\right) s^4 + \cdots + \left(\frac{1}{\tau_1\cdot\tau_2\ldots\tau_5}\right)}. \tag{8}$$

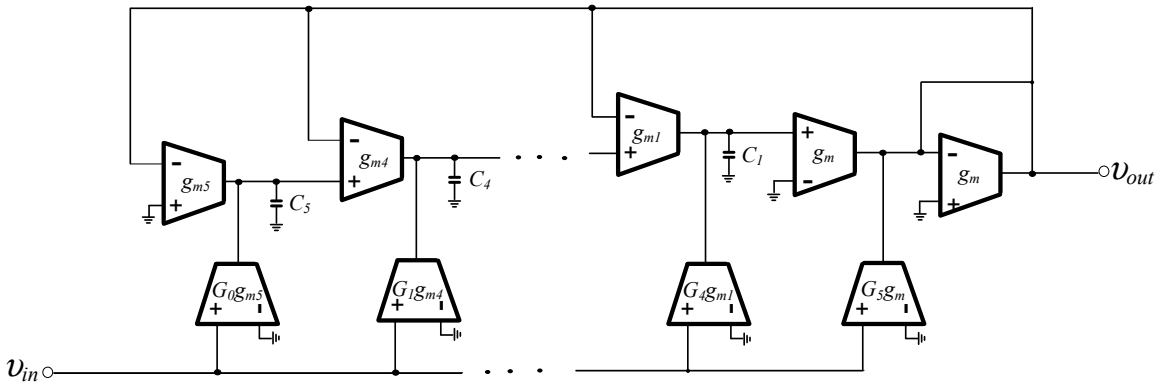


Figure 4. OTA-C realization of the fractional-order differentiator.

The calculation of the time-constants τ_i ($i = 1 \ldots 5$) and scaling factors G_j ($j = 0 \ldots 5$) is performed by equating the corresponding coefficients of the polynomials in (7) with those in (8), and the resulted values are summarized in Table 1.

Table 1. Values of gain factors and time-constants for implementing the fractional-order differentiator.

$G_0 \ldots G_5$	$\tau_1 \ldots \tau_5$ (s)
0.032	—
0.126	0.73 m
0.501	12.3 m
1.996	196 m
7.943	3.12
31.63	52.5

The required integer-order integrator, implemented in OTA-C form, is demonstrated in Figure 5, where the realized transfer function is given by (9)

$$H(s) = \frac{1}{\tau s}, \tag{9}$$

where the time constant is given by the expression $\tau = C/g_m$, with g_m being the transconductance of the OTA. An efficient OTA implementation, which offers improved linearity, is depicted in Figure 6 [22]. Assuming that the MOS transistors are biased in the sub-threshold region, the transconductance of the OTA is given by (10)

$$g_m = \frac{5}{9} \cdot \frac{I_{bias}}{nV_T}, \tag{10}$$

where n is the slope factor of a MOS transistor in sub-threshold region ($1 < n < 2$) and V_T is the thermal voltage (26 mV @ 27 °C).

Comparing the implementation of the functional block diagrams in Figures 2 and 3, the number of the required OTAs is 29 and 15, respectively, leading into an almost 50% reduction of the number of the OTAs. As this is achieved without losing the benefits of electronic tuning of the controller characteristics, it is a very attractive feature from the circuit complexity and power dissipation points of view.

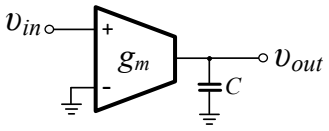


Figure 5. Integer-order integrator topology using OTAs.

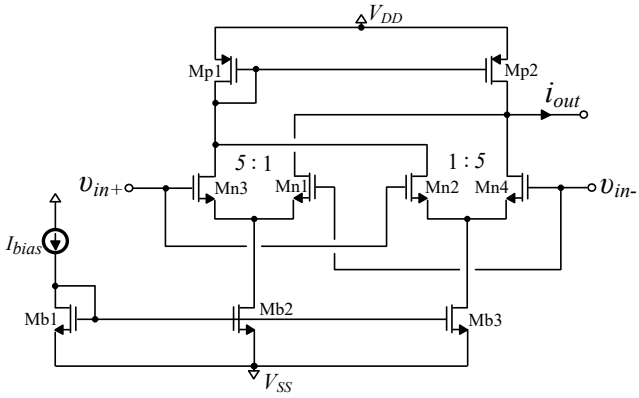


Figure 6. Improved linearity OTA circuit.

2.3. Simulation Results

The performance evaluation of the proposed controller will be performed using the Analog Design Environment of the Cadence software and the MOS transistor models provided by the 0.35 μm Austria Mikro Systeme CMOS process. The employed dc power supply voltages were $V_{DD} = -V_{SS} = 0.75$ V, while the MOS transistors operated in the sub-threshold region. The aspect ratios of the MOS transistors of the OTAs employed in the fractional-order part and in the summation stage were 5 μm/5 μm for Mn1–Mn2, 25 μm/5 μm for Mn3–Mn4, 50 μm/15 μm for Mp1–Mp3, and 2 μm/10 μm for Mb1–Mb3. The aspect ratios of the transistors of the OTA used for implementing the integer-order integrator in Figure 5 were 2 μm/15 μm for Mn1–Mn2, 10 μm/15 μm for Mn3–Mn4, 1 μm/15 μm for Mp1–Mp3, and 5 μm/5 μm for Mb1–Mb3.

Choosing a DC bias current equal to 2.5 nA for all OTAs in Figures 4 and 5, then according to (10) they will have a transconductance $g_m = 44.6$ nS. Using Table 1, the calculated values of capacitors of the topology in Figure 4 will be $C_1 = 26$ pF, $C_2 = 438$ pF, $C_3 = 6.97$ nF, $C_4 = 110.9$ nF, and $C_5 = 1.87$ μF, while the value of the capacitor in Figure 5 will be 2.23 nF. The power consumption of the controller was 445 nW, while for the controller in [17] it was 906 nW, leading to an almost 50% reduction.

The obtained magnitude and phase frequency responses of the open-loop controller-plant system are demonstrated in Figure 7a,b, where the corresponding theoretically predicted ones are given by dashes. The corresponding error plots are provided in Figure 7c, where the error of the magnitude is less than 2% for the whole range and the maximum error in phase is about 10%. As the observed deviation in phase is observed at the lower limit, it is mainly caused by the limitations imposed by the order of the employed approximation [21]. The values of the gain crossover frequency and phase margin are 129.5 mHz and 42.68°, close to the theoretically predicted values of 158 mHz and 45°, respectively. The closed-loop responses of the controller-plant system are demonstrated in Figure 8a,b, with the corresponding error plots given in Figure 8c. The maximum errors of the gain and phase are 0.5% and 11%, respectively. As in previous case the maximum error of the phase is observed at the upper limit of the frequency range it is also caused by the approximation, as in the previous case. The robustness of the controller, with regards to the MOS transistor mismatching and process parameters variations, has been evaluated through a Monte Carlo statistical analysis and the derived histograms ($N = 100$ runs) are demonstrated in Figure 9, where the standard deviation of the gain crossover frequency was 0.64 mHz and for the phase margin was 0.08°. Taking into account that

the corresponding mean values are 129.5 mHz and 42.7°, respectively, it can be concluded that the controller has reasonable sensitivity characteristics.

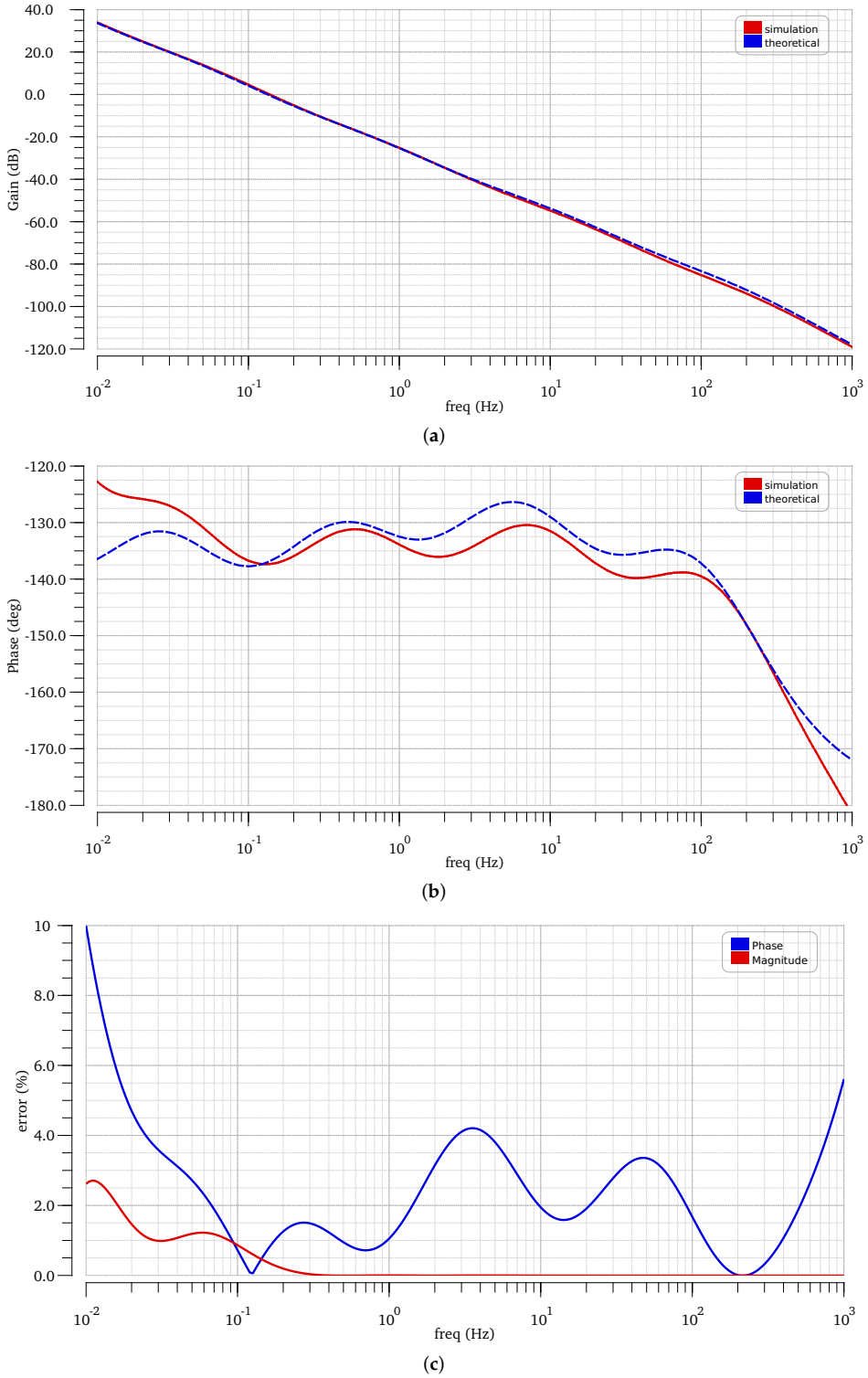
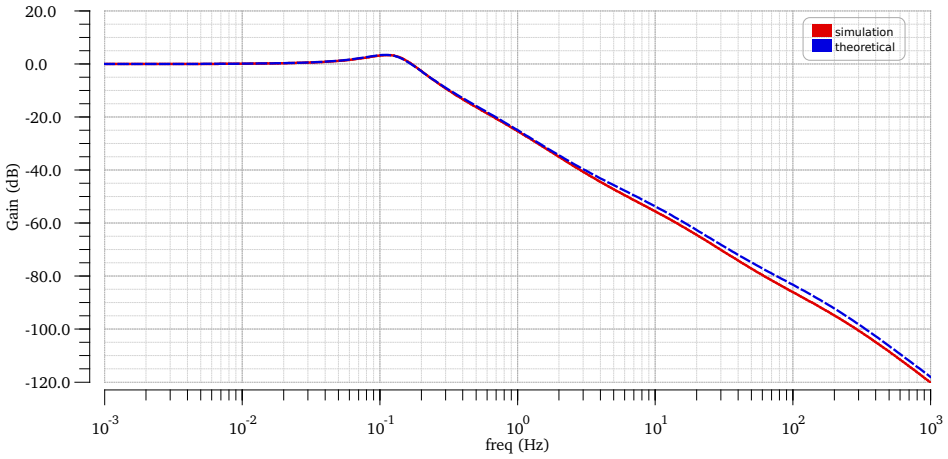
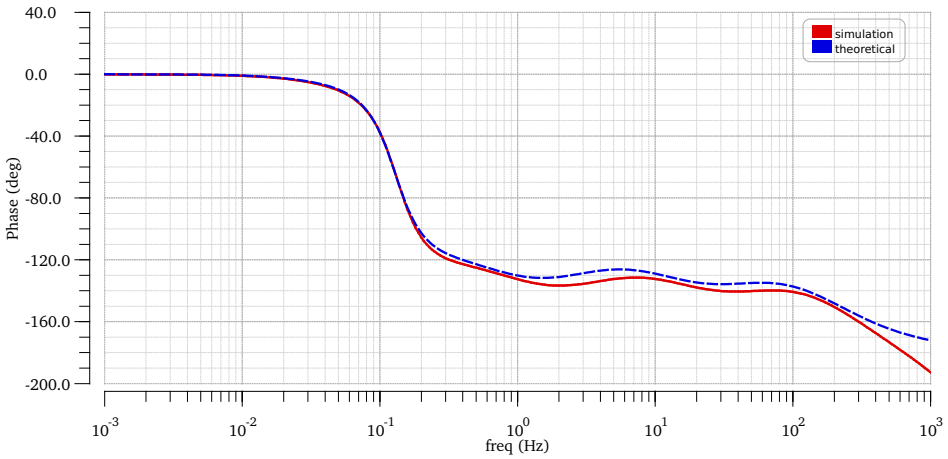


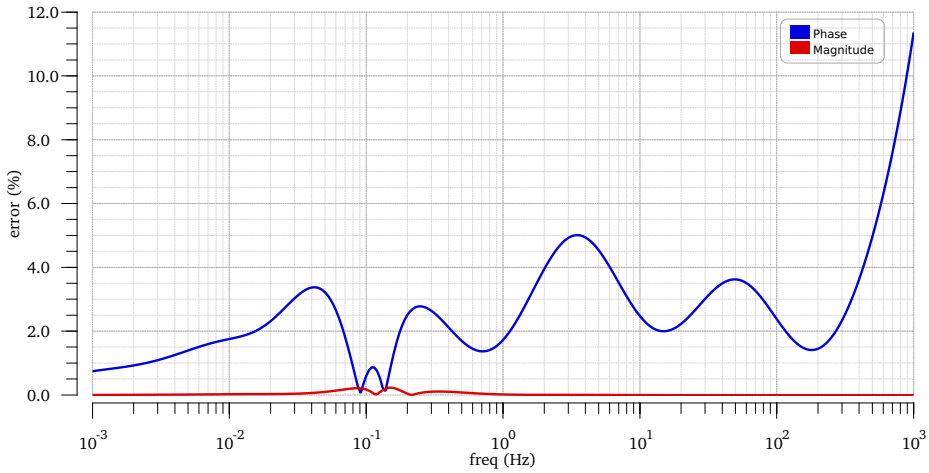
Figure 7. Frequency responses of (**a**) magnitude, (**b**) phase, and (**c**) error of magnitude and phase of the open-loop controller-plant system.



(**a**)



(**b**)



(**c**)

Figure 8. Frequency responses of (**a**) magnitude, (**b**) phase, and (**c**) error of magnitude and phase of the closed-loop controller-plant system.

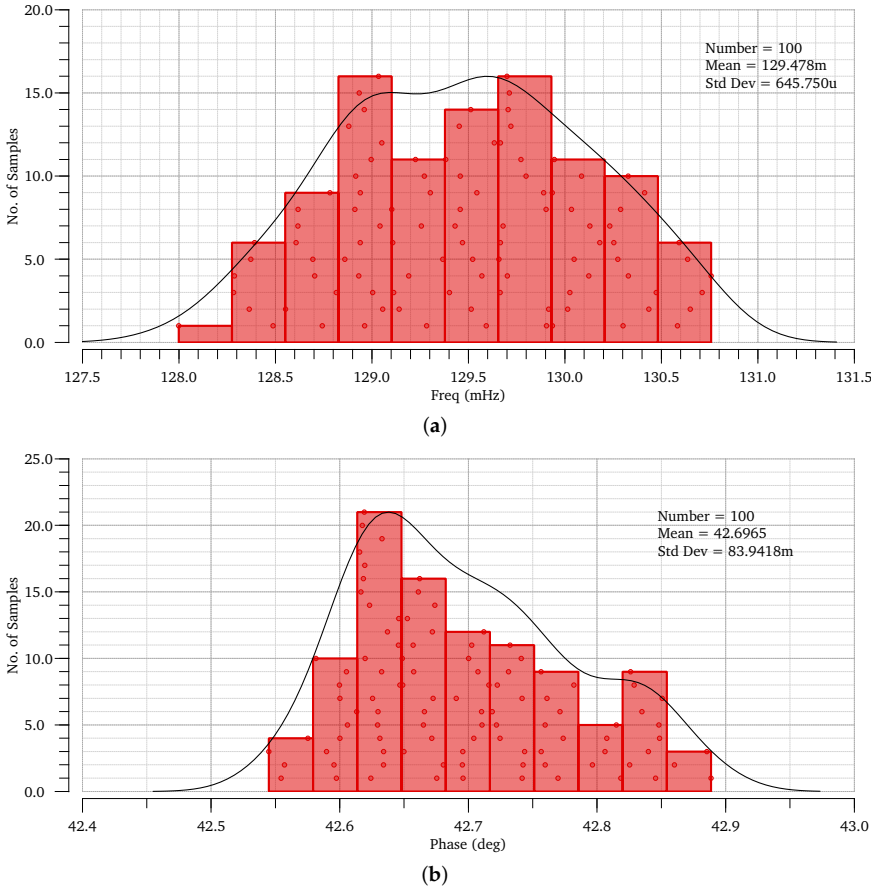


Figure 9. Sensitivity performance of the (**a**) gain crossover frequency, and (**b**) phase margin derived using Monte Carlo analysis.

3. Proposed Fractional-Order Controller of Two Interactive Tanks

Following the previous example, where OTAs have been employed as active elements in order to implement a fractional-order DC motor $I^{\lambda}D^{\mu}$ controller, in this example a new concept is presented. Although OTAs approach offers electronic tunability through appropriate reconfiguration of the biasing DC currents or voltages in the circuit, its disadvantage is the increased number of necessary transistors leading to an increase in power dissipation.

In order to overcome the aforementioned obstacles, a novel fractional-order proportional-integral (PI^{λ}) controller topology is introduced in this example with the attractive features: (a) reduced number of MOS transistors compared to that required in [17] and (b) electronic tuning capability of both proportional gain and integration constant. Electronic tuning of the proportional gain is achieved through the utilization of the trans-linear circuit design principle for implementing a programmable gain stage, while the tuning of the integration constant is achieved through the employment of biasing currents. The designed controller is suitable for controlling, for example, the liquid level into two interacting tank system where the adjustment of the controller parameters for different operating conditions is performed without altering the core of the controller, simply by adjusting the appropriate electrical bias currents.

3.1. Description of the Controller

The two interacting tank system is used in many industrial processes, like petroleum refineries, the paper industry and water treatment facilities. The main problem in these processes is the control of liquid level in tank system and flow between tanks, which varies among different systems. The shape,

volume and area of the tanks, the inflow and outflow rate, the type of liquid and the ambient conditions are factors that affect the whole operation of the system and, thus, the required control.

A two interacting tank level system is demonstrated in Figure 10 (adopted from [23]). It consists of two identical cylindrical tanks, with equal cross sectional area, which are connected through cylindrical pipes of uniform cross sectional area. The liquid is pumped from the reservoir into the first tank through a control valve, while the two tanks are interconnected through manual valves. The objective is to control the level of liquid in tank 2 by varying the inflow rate (q_i) in tank 1. In this work, we consider five different operating points, determined by the height in tank 1 (h_1) and in tank 2 (h_2) as given in Table 2. The corresponding transfer functions C_q ($q = 1, 2, \ldots, 5$) of the controller are, respectively:

$$C_1(s) = 4.917 + \frac{0.236}{s^{0.7}}, \tag{11}$$

$$C_2(s) = 2.578 + \frac{0.0568}{s^{0.7}}, \tag{12}$$

$$C_3(s) = 1.433 + \frac{0.020}{s^{0.7}}, \tag{13}$$

$$C_4(s) = 1.112 + \frac{0.013}{s^{0.7}}, \tag{14}$$

$$C_5(s) = 0.690 + \frac{0.004}{s^{0.7}}. \tag{15}$$

Inspecting (11)–(15), it is concluded that only the proportional gain and integration constant change while the order of integration 0.7 remains constant. This is very important because if we consider that the transfer function of an integrator of order $0 < \lambda < 1$ has the general form

$$H(s) = \frac{1}{(\tau s)^{\lambda}}, \tag{16}$$

where τ is the associated time-constant, then the integration constant K_i and the time-constant are related as

$$K_i = \frac{1}{\tau^{\lambda}}. \tag{17}$$

Utilizing a fractional-order capacitor with pseudo-capacitance C_λ (expressed in Farad/s$^{1-\lambda}$) and the small-signal transconductance g_m (measured in Ω^{-1}) of a MOS transistor for realizing the required time-constant, then the expression in (17) can be alternatively written as

$$\tau = \left(\frac{C_\lambda}{g_m}\right)^{\frac{1}{\lambda}}. \tag{18}$$

Substituting (18) into (17) one obtains

$$K_i = \frac{g_m}{C_\lambda}. \tag{19}$$

The transconductance of a MOS transistor operating in the sub-threshold region is known to be given by

$$g_m = \frac{I_0}{nV_T}, \tag{20}$$

where I_0 is a DC bias current. Therefore, using (19) and (20) we obtain

$$K_i = \frac{I_0}{nC_\lambda V_T}, \tag{21}$$

which means that the tuning of the integration constant could be performed through the appropriate linearly adjusted DC bias current, avoiding the requirement for tuning the value of the fractional-order capacitor. This means that a fixed RC network can be used to approximate the behavior of C_λ.

Table 2. Operating points of the two interacting tank system.

Operating Point	Height h_1 (cm)	Height h_2 (cm)
#1	0.29	0.23
#2	1.41	1.09
#3	3.40	2.64
#4	6.66	5.17
#5	14.06	10.92

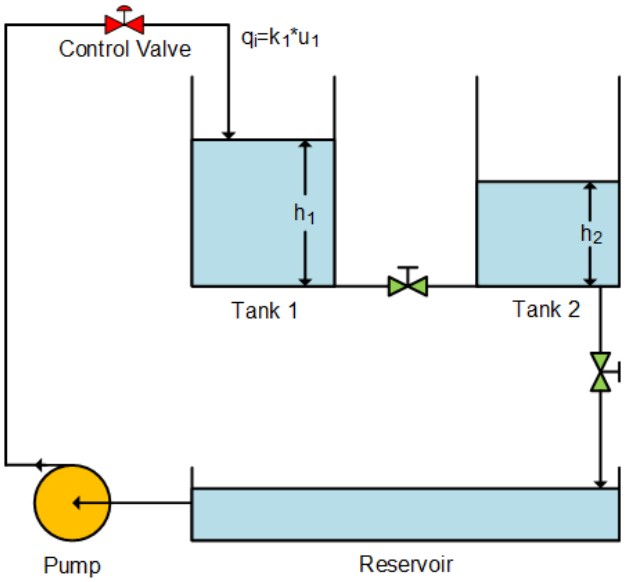


Figure 10. Illustration of the two interactive tanks system.

3.2. Controller Building Blocks

3.2.1. Proportional Stage

The implementation of a gain stage can be easily performed using the simple current-mirror topology depicted in Figure 11a, where the aspect ratio of transistor Mn2 is K_p times the aspect ratio of the diode-connected transistor Mn1 [24]. The input-output relationship, which is realized by the circuit in Figure 11a, is: $i_{out} = K_p i_{in}$. Although this topology offers simple circuitry, it suffers from the absence of electronic adjustment of the gain. This is due to the fact that the scaling factor K_p is tuned through the geometry of the corresponding MOS transistors. Although a bank of output branches of the current-mirror in Figure 11a could be established, which will be digitally controlled, only pre-defined values of the gain are possible, losing the benefit of the design versatility.

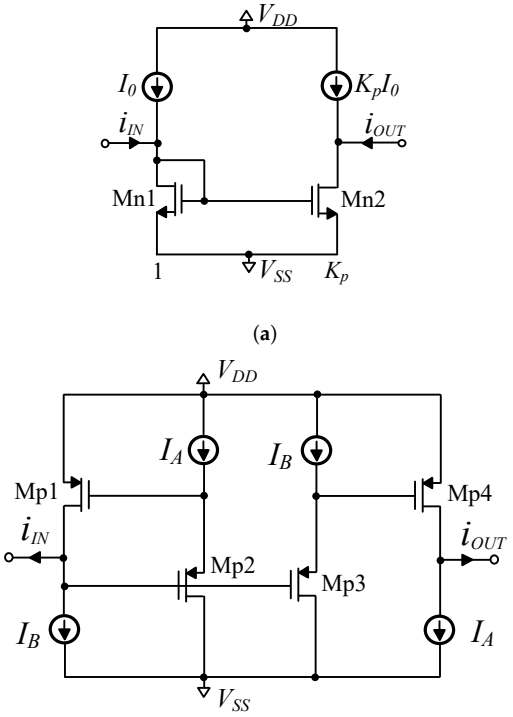


Figure 11. Implementation of the gain stage using a (**a**) current-mirror, and (**b**) a trans-linear loop.

In order to overcome this obstacle, the topology depicted in Figure 11b will be employed. Assuming that transistors Mp1-Mp4 are identical and are biased in the sub-threshold region, then by applying the trans-linear principle [25] in the loop formed by Mp1-Mp4, it is derived that

$$i_{MP1} \cdot i_{MP2} = i_{MP3} \cdot i_{MP4}\,. \tag{22}$$

Since $i_{Mp1} = i_{IN} + I_B$, $i_{Mp2} = I_A$, $i_{Mp3} = I_B$, and $i_{Mp4} = i_{out} + I_A$, the expression of the output current, obtained after some algebraic manipulation, is

$$i_{out} = \left(\frac{I_A}{I_B}\right) \cdot i_{in} \equiv K_p \cdot i_{in}\,. \tag{23}$$

Thus, the gain is now electronically adjusted through the ratio of the DC bias currents I_A and I_B without altering the aspect ratio of the MOS transistors.

3.2.2. Integration Stage

The topology of a fractional-order lossless integrator, using current-mirrors, is depicted in Figure 12. The impedance of the fractional-order capacitor C_λ is given by (24)

$$Z(s) = \frac{1}{C_\lambda s^\lambda}\,, \tag{24}$$

and the realized transfer function is

$$H(s) = \frac{1}{\left[\left(\frac{C_\lambda}{g_m}\right)^{\frac{1}{\lambda}} s\right]^\lambda}\,, \tag{25}$$

with g_m being the transconductance parameter of the diode-connected transistor Mn1, calculated using the formula in (20). Comparing (16) and (25), it is easily obtained that the realized time-constant is given by the form of (18) and, consequently, the expression in (21) is still valid.

A practical problem that appears, for a given value of the pseudo-capacitance C_λ, is that the values of the DC bias current I_0 could be relatively high. This is due to the fact that according to (11)–(15), the maximum current will be 60 times the basic current. For example, considering that $I_0 = 9$ nA, the calculated maximum value will be equal to 0.6 μA. In order to overcome this problem, the integration stage in Figure 12 will be enhanced by embedding a topology similar to that in Figure 11b, as it is demonstrated in Figure 13. As a result, the integration constant becomes

$$K_i = K_{ex} \cdot \frac{I_0}{nC_\lambda V_T}, \tag{26}$$

with the gain factor given by the formula: $K_{ex} = I_{A,ex}/I_{B,ex}$. Considering a fractional-order capacitor equal to 22 μF/s$^{0.3}$ and considering $I_0 = 9$ nA, then according to (26), the relationship between the proportional and integration constant becomes $K_i = 0.0121 \cdot K_{ex}$ and, consequently, the set of values of K_{ex} that must be implemented are $\{19.5, 4.693, 1.652, 1.074, 0.3313\}$. Taking into account that these values are determined by the ratio of the appropriate DC currents, it is obvious that this extra degree of freedom offers reasonable values of currents, in order to keep the transistors operating in the sub-threshold region. The price paid is the increased circuit complexity of the integrator.

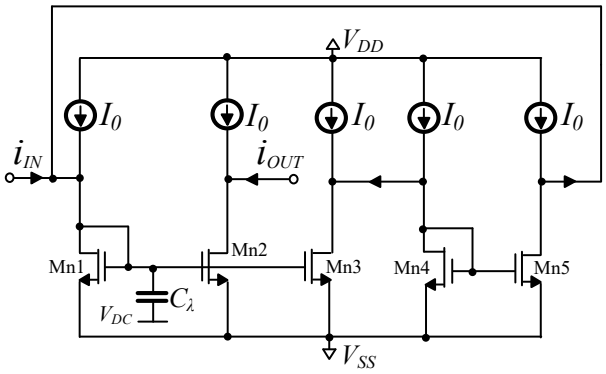


Figure 12. Fractional-order integrator using current mirrors.

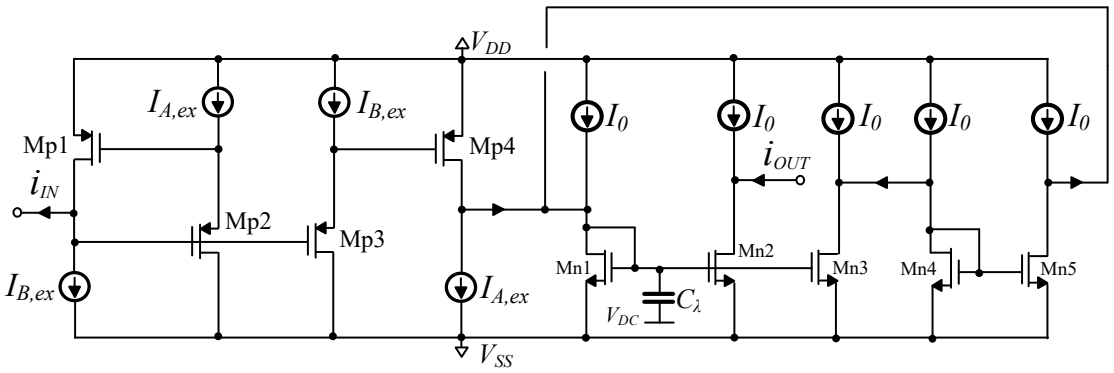


Figure 13. Fractional-order integration topology with an extra gain stage for achieving large time constants.

3.2.3. Fractional-Order Capacitor Emulator

An efficient network for approximating the behavior of a fractional-order capacitor is demonstrated in Figure 14, constructed from m parallel RC branches and two correction elements notated as R_p and C_p, respectively [26]. The total admittance of this network is given by (27)

$$Y_{tot}(s) = sC_p + \frac{1}{R_p} + \sum_{k=1}^{m} \frac{sC_k}{sR_kC_k + 1}. \tag{27}$$

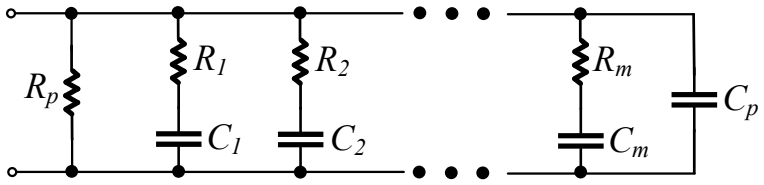


Figure 14. RC network for the approximation of fractional-order capacitors.

Given the pseudo-capacitance C_λ, the fractional order λ, the phase error $\Delta\varphi$ within the frequency range $[\omega_l, \omega_h]$, then choosing the values of R_1 and C_1 in such a way that the $\omega_l = 1/R_1C_1$, the values of passive elements are calculated through the formula

$$R_k = R_1a^{k-1},\ C_k = C_1b^{k-1},\ k = 1, \ldots, m \tag{28}$$

$$R_p = \left(\frac{1-a}{a}\right) R_1\,, C_p = \left(\frac{b^m}{1-b}\right) C_1 \tag{29}$$

The factors $0 < a, b < 1$ are derived through (30) and (31)

$$\varphi_{av} = 90 \cdot \lambda = 90 \cdot \frac{\log(a)}{\log(ab)}, \tag{30}$$

$$ab = \frac{0.24}{1 + \Delta\varphi}. \tag{31}$$

Calculating the impedance Z_{av} at the average frequency $\omega_{av} = \sqrt{\omega_l\omega_h}$ from (27) and comparing the achieved result with the theoretically predicted value, which is equal to $1/C_\lambda\omega_{av}^\lambda$, the values of all the resistors must be multiplied while all the capacitances must be divided by the same factor in order to appropriately scale the implemented impedance. Another point that must be mentioned is that the number of required sections is calculated according to (32), rounded to the nearest integer

$$m = 1 - \frac{\log(\omega_h/\omega_l)}{\log(ab)}. \tag{32}$$

Following the procedure described in Section 3.2.3, the values of passive elements for approximating a fractional-order capacitor of order $\lambda = 0.7$ and pseudo-capacitance $C_\lambda = 22\ \mu F/s^{0.3}$ with phase error $\Delta\varphi = 1^\circ$ within the frequency range [1 mHz, 10 Hz] derived using the Matlab code available in [27], are summarized in Table 3. The magnitude and phase responses along with the theoretically predicted ones, which are given by dashes, are plotted in Figure 15a,b, respectively. The phase response, which is very important for the simulation of the fractional-order capacitor, is also very close to the ideal value of -63°, with the defined expected maximum error of 1° for almost the entire frequency band. The error is increased for frequencies higher than 2 Hz and reaches a maximum of 5° at 10 Hz.

Table 3. Values of the passive elements for approximating a capacitor of order $\lambda = 0.7$ and pseudo-capacitance $C_\lambda = 22$ μF/s$^{0.3}$.

Element	Value	Element	Value
R_1	2.89 MΩ	C_1	55.1 μF
R_2	654.79 kΩ	C_2	29.17 μF
R_3	148.43 kΩ	C_3	15.44 μF
R_4	33.65 kΩ	C_4	8.17 μF
R_5	7.63 kΩ	C_5	4.33 μF
R_p	9.85 MΩ	C_p	4.87 μF

3.3. Simulation Results

The functional block diagram of the realized controller is provided in Figure 16, where the plant is described by the transfer functions $G_i = 1, 2, \ldots, 5$, which correspond to the five different operating points described in Table 2.

$$G_1(s) = \frac{0.8613}{52.56s + 1} e^{-3.96s}, \tag{33}$$

$$G_2(s) = \frac{1.915}{116.5s + 1} e^{-8.66s}, \tag{34}$$

$$G_3(s) = \frac{2.997}{180.1s + 1} e^{-13.4s}, \tag{35}$$

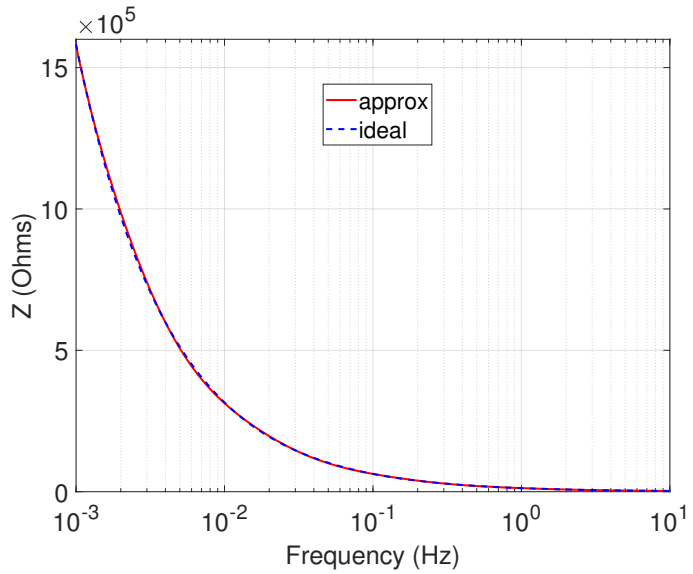
$$G_4(s) = \frac{3.332}{212.5s + 1} e^{-18.5s}, \tag{36}$$

$$G_5(s) = \frac{7.156}{442.3s + 1} e^{-28.9s}. \tag{37}$$

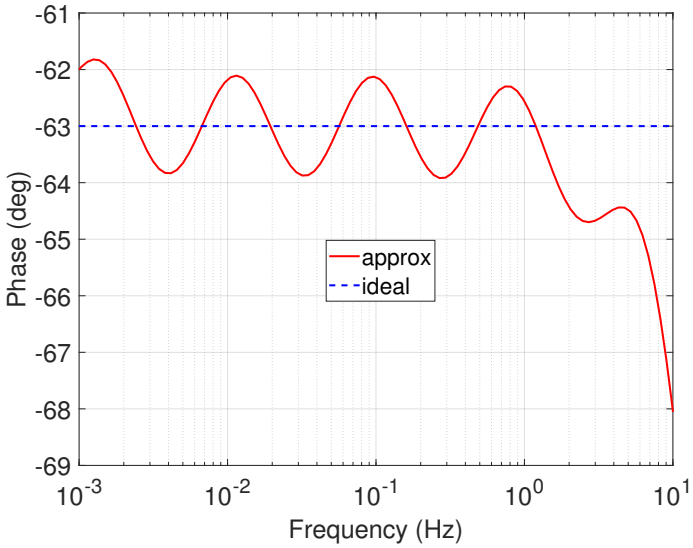
In order to evaluate the behavior of the controller, the same CMOS process will be used as in the previous design example. The employed DC bias voltage scheme was $V_{DD} = -V_{SS} = 0.5V$.

With regards to the gain stage in Figure 11b, the DC current I_B has been chosen equal to 200 pA. Using (11)–(15) the calculated values of the DC bias current I_A were $\{983.4, 515.6, 286.6, 222.4, 138\}$ pA. The dimensions of transistors Mp1-Mp4 were 150 μm/5 μm, while the distribution of the DC bias current I_A has been performed using current-mirrors with the aspect ratio of the nMOS and pMOS transistors equal to 12 μm/6 μm and 60 μm/6 μm, respectively. In the case of the substitution of the DC bias current I_B, the corresponding values were 12 μm/6 μm and 3 μm/1.5 μm. The bias current I_0 of the integrators has been chosen equal to 9 nA. Considering a 22 μF/s$^{0.3}$ pseudo-capacitance then, using (26) and choosing $I_{B,ex} = 300$ pA, the values of $I_{A,ex}$ have been calculated as $\{5.85, 1.41, 0.496, 0.322, 0.1\}$ nA. The aspect ratio of transistors Mp1–Mp4 in Figure 13 were 440 μm/4 μm and the aspect ratios of the transistors in the current mirrors used for distributing the currents $I_{A,ex}$ and $I_{B,ex}$ were 6 μm/3 μm, 100 μm/10 μm, and 6 μm/3 μm, 3 μm/1.5 μm, respectively. The aspect ratio of transistors Mn1–Mn5 in Figure 13 was 16 μm/4 μm and the distribution of the DC bias current I_0 has been performed using current-mirrors with transistor aspect ratio 160 μm/4 μm. Finally, the distribution of the input current of the controller was also performed using current-mirrors with transistor aspect ratios equal to 10 μm/5 μm. The DC bias current of this stage was equal to 200 pA.

The layout design of the active core of the controller is demonstrated in Figure 17. The obtained open-loop gain and phase responses of the controller-plant system are demonstrated in Figure 18, for all the operating points presented in Table 2. The phase margin for the operating points was measured as 70.4°, 69.5°, 74.5°, 76°, and 76.3°, respectively. From the derived results it is concluded that the phase margin increases as the height increases. The corresponding closed-loop responses are provided in Figure 19, while the step responses for all the operating points are depicted in Figure 20.



(**a**)



(**b**)

Figure 15. Frequency responses of the impedance (**a**) magnitude and (**b**) phase of the RC network in Figure 14 approximating a fractional capacitor with $\lambda = 0.7$ and $C_\lambda = 22\ \mu\text{F/s}^{0.3}$.

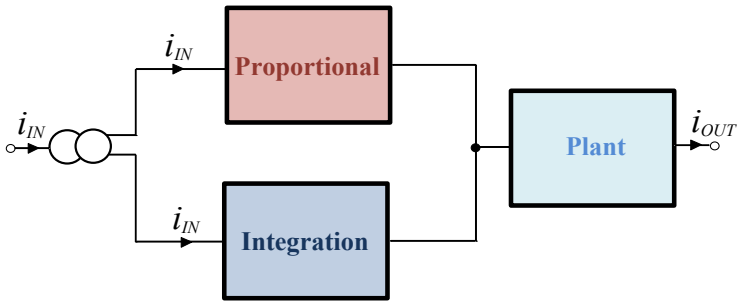


Figure 16. Functional Block Diagram of the realized controller.

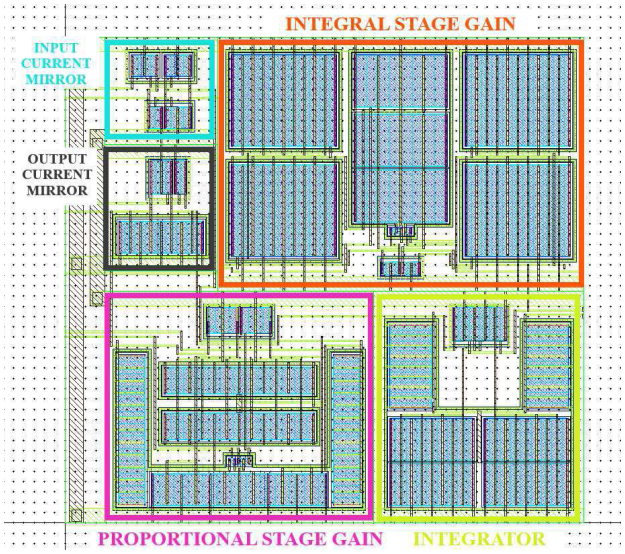
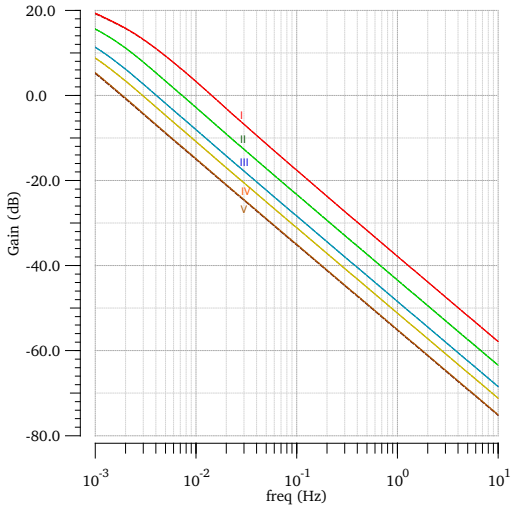
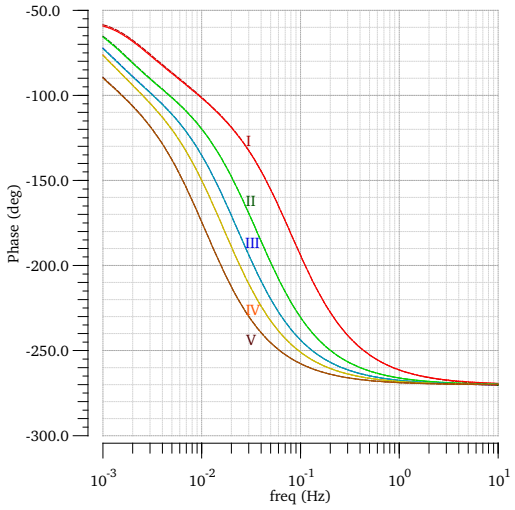


Figure 17. Chip layout design of the complete controller.



(**a**)



(**b**)

Figure 18. Post-layout simulation results showing the (**a**) gain and (**b**) phase responses of the open-loop plant.

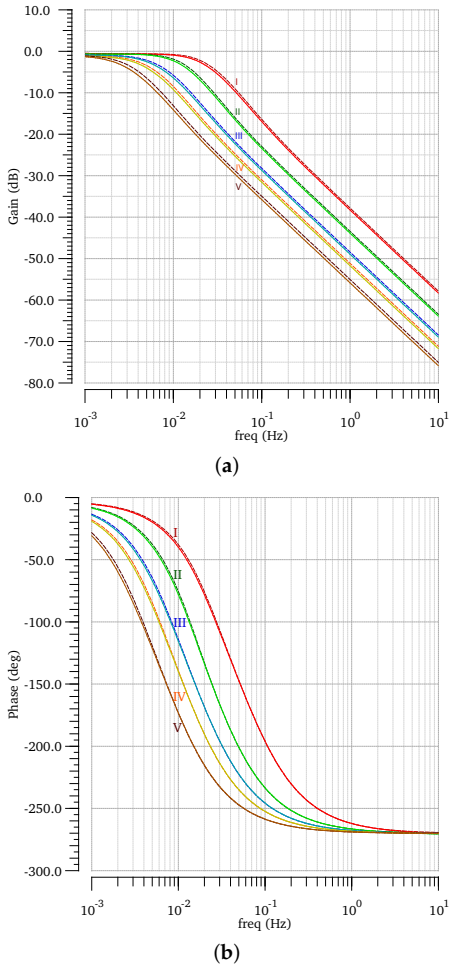


Figure 19. Post-layout simulation results showing the (**a**) gain and (**b**) phase responses of the closed-loop plant.

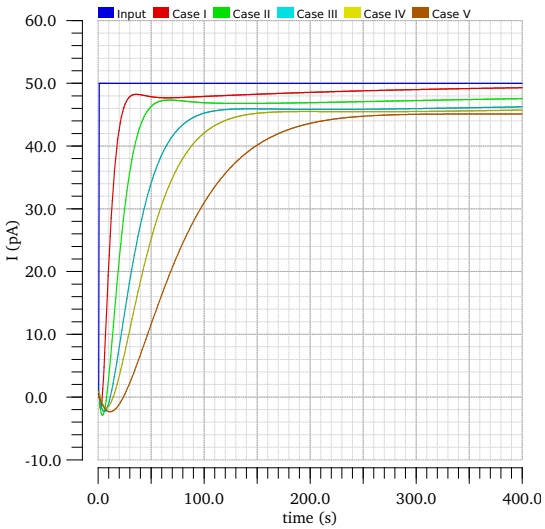


Figure 20. Step response of the controller-plant system.

4. Conclusions

The proposed fractional-order DC motor $I^{\lambda}D^{\mu}$ controller offers an almost 50% reduction of the active component count as well as of power dissipation compared to that introduced in [17].

With regards to the specifications, a 129.5 mHz gain-crossover frequency and 42.68° phase margin are achieved, with the corresponding nominal values being 158 mHz and 45°, respectively.

Moreover, a fully re-configurable controller topology suitable for controlling the level of liquid into two interacting tanks has also been presented in this work. The adjustment of the controller's behavior into various conditions has been achieved through an appropriate adjustment of the corresponding DC bias currents, without altering the topology of the controller. The chip operates within ± 0.5 V power supplies making the design very attractive from the reduced power dissipation point of view. In addition, the presented scheme is general and can be used in other applications, where a PI^{λ} controller is required without changing its core, just by changing the values of the DC bias currents.

The simulation results presented in this article are very promising. Future research directions could be the following:

- improvement of the consistency between theoretical and simulation results through the utilization of higher order approximation of fractional-order Laplacian operator,
- fabrication and experimental verification of chips containing the proposed controller structures.

Author Contributions: This work involved all coauthors. S.K., V.B. and P.B. did the simulations and contributed to the visualization. C.P. investigated and analyzed the simulation results. A.E. proposed the methodology of the controller implementation. I.P. contributed to the controller analysis and prepared the original draft and the editing. All authors have read and agreed to the published version of the manuscript.

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Conflicts of Interest: The authors declare no conflict of interest.

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