

# New Applications and Architectures Based on FPGA/SoC

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## 1. Introduction

Nowadays, the digital world demands continuous technological evolutions. Within the field of electronic devices, one relevant example is field-programmable gate arrays (FPGAs). Systems based on reconfigurable hardware are more capable also including new features: novel architectures, hardware accelerators related to communications, signal, and image processing are being implemented within one single chip. A new technologic era in this field was launched a few decades ago. Novel advanced features embedded in these devices bring a new scenario for the use of these in new applications. Areas based on image/data processing are the most usual fields where these devices are implemented. Nevertheless, new ones such as telecommunications or Internet of Things (IoT) are now adopting these devices. With the advancements in the software system design, they are being used more widely, with many applications and scenarios. Programmable hardware is now commonly used in different applications; however, the appearance of system-on-chip (SoC) has revolutionized the electronics market. Furthermore, the software tools' advancements open the use of these devices to new users and implementations.

There is still a long path concerning development tools and new advanced hardware resources. However, it is already possible to connect microprocessors with programmable hardware resources through the use of SoC resources. Thus, advantages from the software environment like operating systems, high-level functions, or specific drivers to use ad-hoc peripherals can be merged with the hardware advantages provided through the internal FPGA resources.

The combination of SW/HW teams under a common framework accelerates the project design time because the dependencies for validation and verification procedures are reduced using a common device and tool. In addition, there are new high-level for system designers to accelerate the market time and take advantage of the powerful all-in-one system that new SoCs offer. The research community is taking advantage of these devices to develop prototypes or even final products with a high technology readiness level (TRL) with short design time.

This Special Issue is an example of adopting the new FPGA features and SoC resources applied to different disciplines such as indoor positioning, optimization of algorithms using operating systems (OS), optimizing codes, software-defined networks (SDN) or new artificial intelligence (AI) processing platforms. So, several articles are focused on sharing and showing new designs based on FPGAs and SoCs applying new development tools to speed-up data processing and optimise algorithms, present novel architectures, and propose novel hardware for new machine learning systems running in real-time.

## 2. Processing Speed-ups and Algorithm Optimisations Based on FPGA/SoCs

The Special Issue contains several articles about speeding up a specific algorithm or data processing employing FPGA/SoC implementation. For instance, the paper [1] presents a customized hardware RTOS (real-time operating systems) implementation based on multiple pipeline registers and MIPS32 architecture. The implementation of RTOS requires several mechanisms such as task context switch operations, inter-task synchronization, or data communication. Software implementations of RTOS-specific functions can generate significant delays, adversely affecting the deadlines required for particular applications. In this paper, the authors implement a dedicated processor with MIPS32 architecture, based on multiple pipeline registers and hardware support for a dynamic scheduler with an enhanced performance, ensuring real-time control operation. A whole review of similar initiatives validates the robustness and performance of the proposed architecture. Thus, the paper shows an interesting comparison among the most usual microprocessor approaches. Indicators such as frequency, pipeline stages, or scheduler implementation are included.

Within the same thematic field, the paper [2] implements a high-performance time server core for FPGA system-on-chip. It shows a complete design and implementation of a low-cost, low-footprint, network time protocol server core using programmable hardware, which can easily fit in a low-range field-programmable chip. The most remarkable novelties introduced are a hardware-optimized timekeeping algorithm implementation, a full-hardware protocol stack, and automatic network configuration. The proposed modular architecture implemented in a low-cost FPGA (Spartan 3E) can achieve all expected time requirements and provide a similar performance that other solutions without this hardware implementation. The system used a commercial GPS connected to a serial port through an FPGA evaluation board.

In [3] an optical signal-based indoor positioning system (IPS) from a SoC-microprocessor unit (MCU) is presented. Different techniques and conditions are evaluated, finally integrating both the hardware and software requirements for an IPS detector in the MCU obtaining the frequency domain information implemented through the Goertzel's algorithm. Additionally, the signal acquisition and up-to 16 digital filtering processing is all included in the MCU-SoC approach.

The next paper [4] presents an FPGA implementation of a low complexity near maximum likelihood detection algorithm for a multiple input-multiple output (MIMO) quadrature spatial modulation (QSM) transmission system. The detection algorithm is based on a tree search and a spherical detection strategy. The proposal has been validated with a MIMO receiver. The achieved results show a low complexity detection algorithm reaching similar performance to other complex solutions. The reduction of operations is based on optimized fixed-point accuracy. The last paper of this block [5] presents a co-design tester, mixing the design and implementation of CPU plus FPGA systems for software defined network (SDN) switches the direct access into SDN switches, which accelerates the innovation and deployment of network functions in the data plane. The developed co-designed architecture provides flexible APIs for test cases of the control plane and high performance for testing functions in the data plane. The novel approach is based on an FPGA-CPU tester binding the advantages of reconfigurable hardware and software complexity through the CPU. The use of this solution is validated for SDN switches obtaining all expected requirements within SDN switches. Besides, the implementation of the pipelined system allows performing several testing routines in one pipeline. Relevant contributions in terms of traffic rates are provided to validate the performance of the proposed approach.

## 3. Advanced Architectures for Specific Applications

Additionally, in the Special Issue, we looked forward to new architectures for specific applications based on SoC/FPGA solutions.

Thus, paper [6] shows the application of SoCs in mobile robotics. In particular, this paper presents the design and implementation of a real-time system for robot navigation that integrates, in a Xilinx Zynq<sup>®</sup> System on Chip, algorithms of neural control, image processing, path planning,

and inverse kinematics and trajectory tracking for a BlueBotics Shrimp robot. The different blocks of an algorithm for the mobile platform are evaluated for a PC and for an SoC solution. The analysis of the partial functions between both platforms strengthens the advantages of an SoC solution for parallel implementation of routines with no data hazards.

Another paper related to specific HW architecture is [7], where a high-performance bit-vector-based packet classification implemented on FPGA is developed. The proposed solution presents a memory-optimized packet classification scheme that can significantly reduce memory resources (around 40%) without compromising the high throughput of the original Bit-Vector-based algorithms.

Following a similar research line, the paper [8] proposes a new architecture based on FPGA to implement an stochastic-local-search hardware solver. The performance and use of resources have better figures than the SW counterparts.

Finally, a remarkable example of the use of new FPGA devices for new scenarios and applications is [9]. The authors develop on an FPGA-based SmartNIC a reconfigurable pipeline for network processing. FPGA-based SmartNICs are widely deployed to accelerate network functions (NFs) for datacenter operators. The authors present a reconfigurable network processing pipeline which abstracts packet processing into multiple "drawers" connected by the same interface, enabling modular development of NFs, suitable for rapid deployment of NFs.

#### 4. Neural Networks Implementations

This last section collects different papers devoted to machine learning architectures and neural network implementations.

In the paper [10], an SoC design executes a configurable neural network trained using an extended Kalman filter (EKF). The architecture can reproduce the transfer function of different multilayer feedforward neural network (MFNN) configurations later trained by an EKF to obtain the optimal weight values for the MFNN.

Following the same idea, the paper [11] presents a novel architecture for generative adversarial neural networks implemented in programmable hardware. The acceleration architecture proposes a novel data flow exploration by splitting the required filters and corresponding input feature maps to later apply a Winograd algorithm for fast processing with high efficiency.

The last paper [12] presents a compact SoC convolutional neural network (CNN) accelerator for an internet-of-things (IoT) endpoint. The CNN accelerator achieved a large throughput, maintaining resources at a minimum. This research work provides the CNN computational power of the SoC available in the IoT nodes.

We foresee a broad research field around computing resources at the IoT edge devices inferring artificial intelligence (AI) algorithms.

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