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Comparative Performance and Assessment Study of a Current-Fed DC-DC Resonant Converter Combining Si, SiC, and GaN-Based Power Semiconductor Devices

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Abstract: This paper focuses on the main reasons of low efficiency in a current-fed DC-DC resonant converter applied to photovoltaic (PV) isolated systems, comparing the effects derived by the overlapping time in the gate-signals (gate-source voltage) combining silicon (Si), silicon carbide (SiC), and gallium nitride (GaN)-based power devices. The results show that unidirectional switches (metal–oxide–semiconductor field-effect transistors (MOSFETs) plus diode) present hard switching as a result of the diode preventing the MOSFET capacitance of being discharged. The effectiveness of the converter was verified with a 200-W prototype with an input voltage range of 0–30.3 V, an output voltage of 200 V, and a switching frequency of 200 kHz. The reduction losses by applying GaN versus Si and SiC technologies are 66.49% and 53.57%, respectively. Alternatively, by applying SiC versus Si devices the reduction loss is 27.84%. Finally, according to the results, 60% of losses were caused by the diodes on both switches.

Keywords: current-fed DC-DC resonant converter; semiconductors; parallel resonant tank; photovoltaic systems

1. Introduction

Photovoltaic (PV) energy has received a great attention in research and industry because it is one of the most efficient and effective solutions to the environmentally friendly sources [1]. It can be classified into isolated systems and interconnected systems. Isolated systems represent those applications that store energy in battery banks, and the interconnected systems supply the generated energy by the PV panel to the electrical grid, satisfying standards as appropriate.

The interconnected systems represent one of the most studied applications, generally, they are represented by five stages. The first stage allows a low-frequency ripple. The second stage increases the voltage level from the PV according to the inverter specifications. The third and fourth stages represent the decoupling capacitor and the inverter, which has to fulfill three functions: 1. to shape the current into a sinusoidal waveform, 2. to invert the current into an AC current, and 3. if the PV array voltage is lower than the grid voltage, the PV array voltage must be boosted with an additional element. This last point is important because there must be no reverse energy to the DC source. Finally, the fifth stage filters the sinusoidal signal.

Alternatively, the PV energy varies with changes in atmospheric conditions and the non-linear source. According to the literature, there are control schemes to deliver the maximum power considering changes in atmospheric conditions, load demands, or external faults. Examples of common control schemes in the Maximum Power Point Tracking (MPPT) are presented in [1–4]. Furthermore, there are some studies that evaluate the MPPT control by applying current controllers as proportional integral (PI), hysteresis, predictive, and sliding-mode controllers [5] maintaining the stable operation of a grid-connected PV system as they can regulate the current to follow the reference current (PV system).

In this way, it is necessary to take into account a controller through partial feedback linearization, and a calculation of the sinusoidal reference current in order to control the current injected into grid, thus the operation of the PV system at the MPPT is guaranteed [6].

One of the key energy conversion systems of the PV-interconnected systems is the DC-DC power converter (stage two), which can be divided into two categories: resonant and non-resonant converters. The non-resonant converters represent the most studied topologies for PV-interconnected systems. One of the widely used is the Boost converter [7–9]. Part of the problem using a Boost converter is related to the need to use two large inductors, causing a challenging point on the size reduction [10]. Furthermore, due to its limited efficiency, it is generally a viable option for low power applications.

Similar to the Boost converter, the conventional [11–14] and active [15,16] Flyback converters are typically used, showing some disadvantages related to the high percentage of energy managed by the transformer, considerably increasing its size. In addition, the “stress” presented by the rectifier diode and the issue of pulsating input current make it a system that requires the placement of additional capacitive elements.

Recently, several DC-DC resonant converters have been reported in the literature since they present a higher efficiency working at higher frequencies and higher power density than the conventional DC-DC converters. These resonant converters could be divided into two categories: voltage-fed DC-DC resonant converters (VFRC) and current-fed DC-DC resonant converters (CFRC).

The VFRC represent the majority of the resonant topologies applied [17–25] and have less components, higher efficiency, higher power density, and frequency operation. However, these topologies present a pulsating input current, thereby, it is necessary to use an additional filter stage [26].

On the other hand, the CFRC represent the minority of the studied topologies in PV-interconnected systems [27–30] and do not present a pulsating input current, and thus the stage to avoid the ripple current being reflected to the PV system is unnecessary. However, the main disadvantages of these topologies are the requirements of a large inductor to feed the inverter with current instead of voltage, as well as the use of unidirectional switches. This point results in one of the primary reasons of low efficiency in the whole converter. Additionally, the control stage is more complex.

The use of CFRC is based on parallel resonant tanks, and the unidirectional switches used can be applied by IGBTs, BJTs or an array of a metal–oxide–semiconductor field-effect transistor (MOSFET) in series with a diode. These converters usually present zero voltage switching (ZVS), and in comparison with other resonant converters, they commonly use only two choke inductors instead of the push-pull current source inverter (CSI), and only two grounded switches instead of the full-bridge. Moreover, the CFRC satisfy the front-end DC-DC converter requirements for this application since the two current-fed inductors used comprise a high gain voltage ratio. Additionally, in comparison with topologies fed in voltage, the CFRC has independent active/reactive power control and fast dynamic response [31].

According to the last characteristics, there is a need to study the feasibility of the minority part of topologies applied in PV-interconnected systems. In this sense, the main contribution of this paper is to assess the performance of the CFRC applied in PV-isolated systems (in stage 2), specifically considering the losses in the unidirectional switches comparing the key performance indicators for silicon (Si), silicon carbide (SiC), and gallium nitride (GaN)-based power devices.

This paper is divided as follows: Section 2 presents the topology, design methodology, study of key parameters in power losses, and a brief comparison of key performance indicators for Si, SiC,

and GaN power devices. Section 3 shows the experimental results. Section 4 presents a study of the power losses originating from the commutations and the overlap of the unidirectional switches used. Finally, Section 5 presents the conclusions.

2. Current-Fed DC-DC Resonant Converter and Power Devices

Based on [32], there are different configurations of CFRC. For this work, the studied current inverter is the two current sources resonant inverter. The resonant inductor of the parallel resonant tank is changed by a transformer to obtain galvanic isolation. The sinusoidal signal obtained from the parallel resonant tank is rectified with a full-bridge rectifier and filtered with an LC filter.

An important characteristic in a CFRC is that the current source must be short-circuited. The time in both switches (S_1 and S_2) during the short-circuit is named overlapping. In this time, the parallel resonant tank is isolated to the rest of the circuit. To obtain this isolating, it is necessary to use unidirectional switches to prevent the flow of AC current to the DC side of the inverter [33]. To establish unidirectional switches, it is possible to use two arrays: the first one by a diode in series with a MOSFET and the second one by an IGBT.

The general characteristics of both arrays have been discussed and compared before [34–36]. Basically, the primary disadvantage of IGBT is related to the operational frequency, since it can only operate in frequency ranges of up to 150 kHz. On the other hand, the array configured by a MOSFET in series with a diode partially solves the switching frequency problem. However, the primary problem with this configuration is the increase in parasitic capacitances (MOSFET and diode), which represent a substantial increase in power loss. Therefore, a selection of the semiconductor devices to be used in the experimental stage should be performed.

Considering remarks and because the motivation to use resonant converters is the relation of higher power/weight and power/size ratios, the arrangement to allow operation at a high switching frequency needs to be considered. In this manner, not only the large passive elements need to be considered in the converter design, but also the efficiency target and thermal design. Therefore, Figure 1 shows the CFRC studied.

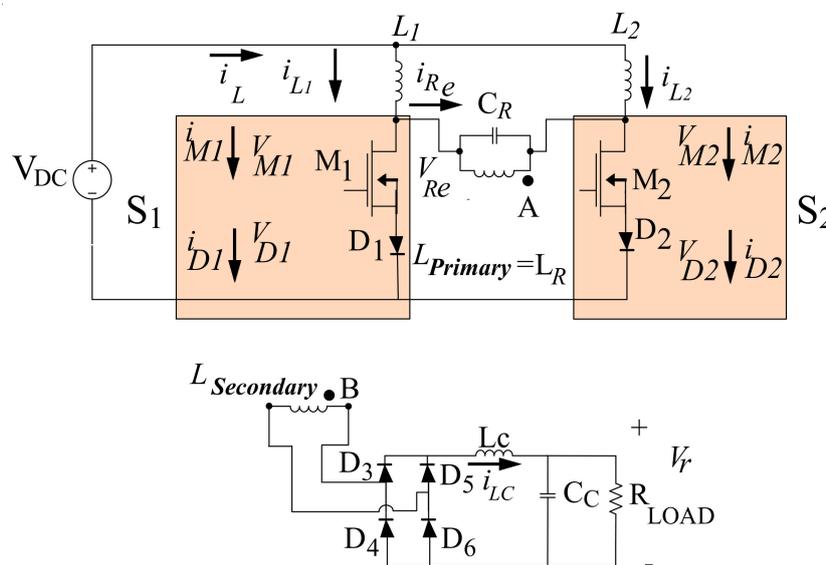


Figure 1. Current-fed DC-DC resonant converters (CFRC) performing unidirectional switches using a metal–oxide–semiconductor field-effect transistor (MOSFET) in series with a diode.

The topology shown in Figure 1 is comprised of four stages: the first stage consists of two current sources (L_1 and L_2) and a DC voltage source (V_{DC}), the second stage by a parallel resonant tank ($L_{Primary}$ and C_R) with magnetic isolation derived by $L_{Primary}$, where $L_{Primary}$ is coupled to $L_{Secondary}$ (from part A to B), the third stage by a full-wave rectifier (D_3 – D_6), and the fourth stage by the decoupling elements

(C_c and L_c). The operation of the circuit is as follows: the two inductors L_1 and L_2 provide the two current sources to the parallel resonant tank, the unidirectional switches S_1 and S_2 short-circuit the current sources periodically in order to feed the parallel resonant tank formed by the transformer (composed by $L_{Primary}$ and $L_{Secondary}$) and the resonant capacitor C_R with a square current waveform. The parallel resonant tank filters this waveform and applies a sinusoidal voltage waveform to the full-bridge rectifier (D_3, D_4, D_5 and D_6). The rectified signal is filtered by L_C and C_C and it is applied to the load (R_{LOAD}). One important characteristic of the CFRC (Figure 1) is the need to have an overlapped control, because if there is no overlapping control between M_1 and M_2 , the inductance (L_1) would be charged by the current $i_{L1}(t)$, and the current $i_{L2}(t)$ from the second inductance (L_2) would flow directly through the resonant tank. Under the dual condition, $i_{L1}(t)$ would flow through the resonant tank and $i_{L2}(t)$ through L_2 . However, if there is no overlapped control, $i_{L1}(t)$ and $i_{L2}(t)$ could be canceled, although not completely, producing a considerable increase in the losses on the unidirectional switches. Furthermore, the resonant tank and the components used need to be carefully selected, since these parameters directly affect the overlap signals in S_1 and S_2 . Additionally, the high frequency transformer is a critical part of the resonant converter. Its design affects efficiency, weight, and dimension of the whole topology. This fact is important to improve the efficiency of the topology. Considering these statements, a brief comparison of different semiconductor devices should be performed. As a result of the advancement in the field of power semiconductor technologies [37–39], SiC MOSFETs, SiC junction gate field-effect transistors (JFETs), SiC Schottky barrier diodes, and gallium nitride (GaN) transistors provide a valuable opportunity to obtain high efficient performance with compact size. Part of the primary characteristics in all power semiconductor devices are related to the operating at high power, high frequency, and high temperature. In fact, many works have been reported in the literature analyzing the physical breakdown mechanisms, modeling, characterizations, and the trade-off characteristics between the breakdown voltage and the on-resistance of Si, SiC, and GaN-based power semiconductor devices [40–43]. As a result of these studies, some characteristics are shown in Table 1.

Table 1. Physical properties of silicon (Si), silicon carbide (SiC), and gallium nitride (GaN).

Electrical Property	Units	Si	SiC	GaN
Band gap energy	eV	1.1	3.26	3.4
Thermal conduction	W/cm·K	1.5	3.7	1.3
Electron mobility	cm ² /V·s	1300	900	900–2000
Saturation drift velocity	cm/s	1×10^7	2×10^7	2.5×10^7

The capacity to achieve high switching frequency in every semiconductor is directly proportional to its drag-velocity. The speeds present in GaN devices are more than twice the speed in Si components, achieving commutations at much higher frequencies. However, a negative characteristic by GaN devices in comparison with Si and SiC is less thermal conductivity [44–46], which means the heat generation of SiC devices can be easily dissipated as compared to GaN. From the previous characteristics, one of the key behaviors to compare with these power devices in a CFRC is the overlap stage control. In this way, a brief study of this condition is presented below.

Overlap in Gate-Signals of M_1 and M_2

To determine the effect of the overlap, an initial simulation study is developed under the following considerations: (1) time delay proposed between the turn on of M_1 and M_2 is 0.49, this value was taken because T_D must be as close as 0.5, with the aim of not having such a long overlap; (2) a quality factor of the resonant tank is sufficiently high to filter all the current harmonics, except the fundamental; (3) all inductors and capacitors are lossless; (4) D_3, D_4, D_5 , and D_6 are ideal diodes; and (5) unidirectional switches were performed by SiC diodes (C4D08120) and SiC MOSFETs (C2M0160120D), because of their improvements for AC-DC and DC-DC converters. These devices can operate with reduced conduction

and switching losses over higher frequencies, and higher temperatures minimize the requirements for the passive components and reduce cooling demands [47–49]; however, the performance given by SiC power devices will be compared with Si and GaN. The switching frequency (F_{sw}) was considered to be 200 kHz. The simulation results in Figure 2 created in PSpice® show the key waveforms of S_1 (Figure 2a), S_2 (Figure 2b), D_1 (Figure 2c), gate-signals in M_2 (Figure 2d), and M_1 (Figure 2e). These simulation results are also based on the design parameters and design methodology shown in Tables 2 and 3.

Table 2. Design parameters.

Parameter	Symbol	Value
Output power	$P(W)$	200
Input voltage	$V_{DC}(V)$	30.3
Switching frequency	$F_{sw}(kHz)$	200
Quality factor	Q	5
Output voltage	$V_r(V)$	210
Rectifier voltage	$V_{AB}(V)$	267.38
Angular frequency	$\omega_r(Hz)$	1,257,000

Table 3. Design methodology.

Parameter	Symbol	Equation	Value
Load	R_{load}	$\frac{V_r^2}{P_{load}}$	213.8 Ω
Current sources	L_1, L_2	$\frac{v_{cc}^2}{0.2 \cdot P_{grid} \cdot F_{sw}}$	114.8 μH
Resonant capacitor	C_R	$\frac{Q}{2\pi(60) \cdot R_{equ}}$	186.7 nF
Number of turns	n	$n = \frac{1}{V_{DC} \cdot \pi} \cdot \sqrt{\frac{2 \cdot P_{load} \cdot R_{equ}}{\eta_{res}}}$	3.588
Secondary winding	$L_{Secondary}$	$\frac{1}{\omega_r^2 \cdot C_r}$	3.392 μH
Primary winding	$L_{Primary}$	$n^2 \cdot L_s$	43.66 μH
Decoupling inductance	L_c	$\frac{V_{AB}}{4 \cdot F_{sw} \cdot 0.199}$	3 mH
Decoupling capacitor	C_c	$\frac{(1-D) \cdot V_r}{8 \cdot L_b \cdot F_{sw}^2 \cdot \Delta v_o}$	5 μF

From Figure 2, when the overlap begins (gate-signal in M_1 and gate-signal in M_2 are in the on-state), the current i_{S1} decreases to zero, and the current i_{S2} increases. This behavior is related to the charge and discharge of the internal stray capacitances of D_1 and D_2 .

In this sense, when S_2 is in the on-state, M_2 can be modeled by its output parasitic capacitance in parallel with its parasitic resistance, and D_2 as a parallel made up of the same diode and its stray capacitance. Furthermore, Figure 3 shows the hard switching in D_1 and M_1 caused by the effect given by the overlap. In this manner, to determine the converter performance effects, based on Figure 3, three modes are proposed considering the current and voltage waveforms of S_1 and S_2 ; therefore, the first mode (MODE A from t_0 to t_2) performs a fall-rise of i_{S1} and a rise-fall of i_{S2} , the second mode (MODE B from t_2 to t_3) represents the time when i_{S1} keeps its value and i_{S2} is zero, and the third mode (MODE C from t_3 to t_4) represents the dual condition of MODE B.

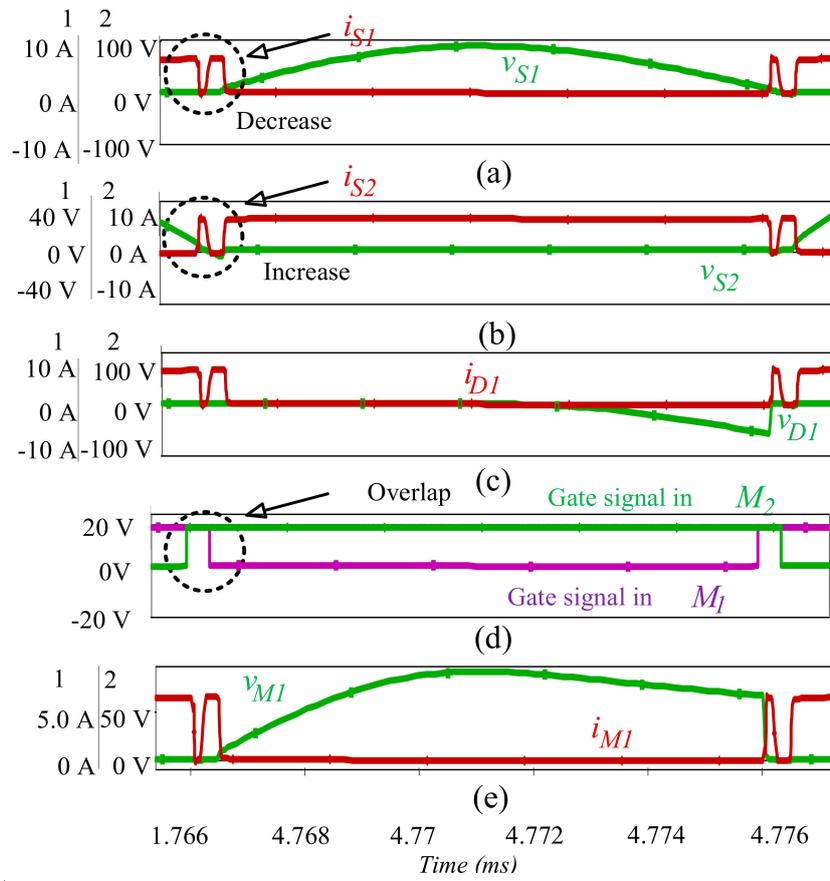


Figure 2. Simulation key waveforms: (a) voltage and current in switch S_1 (v_{S1} and i_{S1}), (b) voltage and current in switch S_2 (v_{S2} and i_{S2}), (c) voltage and current at the diode D_1 (V_{D1} and i_{D1}), (d) gate-signal in M_1 (V_{GSM1}) and gate-signal in M_2 (V_{GSM2}), (e) drain-source voltage and current at the MOSFET M_1 (v_{M1} and i_{M1}).

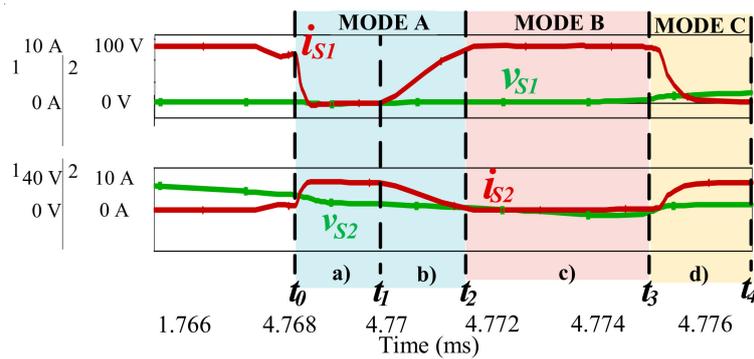


Figure 3. Key waveforms: voltage and current in S_1 and S_2 .

From Figure 3 and based on times t_0 to t_4 , the equivalent circuits are obtained, as shown in Figure 4. In these circuits, an equivalent resistance (R_{equ}) was considered as the load in the resonant tank, where R_{equ} represents the R_{LOAD} seen from L_r . Then, based on the operation, MODES are shown during the overlap and equivalent circuits in Figures 3 and 4, respectively. The modes A, B, and C are detailed below:

Time t_0 - t_1 (Figure 4a): this time starts when the gate-signal in M_2 is in the on-state, thereby the overlap starts. During this time, i_{S1} decreases to zero (and remains at 0 A) and i_{S2} increases its value

the same as the input current (I_L). Moreover, since S_2 is in the on-state, the diode D_1 can be modeled as a parallel by the same diode and its stray capacitance C_{D1} , and M_1 by a drain-source resistance R_{DSONM1} . In this moment, the voltage of the stray capacitance in D_1 (V_{CD1}) can be represented as shown in Equation (1).

$$V_{CD1} = V_{RES} - V_{DSM1} - V_{DSM2} - V_{D2} \tag{1}$$

where V_{RES} is the voltage of the resonant tank, V_{DSM1} represents the voltage drain-source in M_1 , V_{DSM2} the voltage drain-source in M_2 , and V_{D2} the forward voltage in D_2 . Furthermore, in this time, there is a “charge” condition in C_{D1} which generates an increase of switching losses in S_1 until the voltage in D_1 reaches its forward voltage.

Time t_1-t_2 : It represents the instant when i_{s1} increases and i_{s2} decreases its value, turning on S_1 , and modeled D_2 as a parallel by D_2 and its stray capacitance C_{D2} , and M_2 by a drain-source resistance R_{DSONM2} (Figure 4b). In this time, the voltage of the stray capacitance in D_2 (V_{CD2}) can be represented as shown in Equation (2), where V_{D1} represents the forward voltage in D_1 .

$$V_{CD2} = V_{RES} - V_{DSM1} - V_{DSM2} - V_{D1} \tag{2}$$

Time t_2-t_3 : In MODE B (Figure 4c), M_1 and M_2 are in the on-state. Furthermore, i_{s1} stays constant and i_{s2} stays at 0A, modeling D_2 and M_2 the same as from t_1 to t_2 . On the other hand, there is no current in S_2 but there is a voltage in D_2 , increasing the power losses. Moreover, the voltage of the stray capacitance in D_2 (V_{CD2}) can be represented the same as Equation (2).

Time t_3-t_4 : MODE C starts (Figure 4d), the gate-signal in M_1 is in the off-state, and thus the overlap is finished. Furthermore, M_2 is in the on-state and i_{s2} is increasing. During this time, S_1 is in the off-state after finishing the discharging process, which causes the stored energy to be lost not only in M_2 but also in D_2 . Additionally, as a result of M_1 in the off-state, V_{RES} will be split in D_1 and M_1 with a complementary voltage in D_2 . In fact, V_{CD2} can be modeled as shown in Equation (3).

$$V_{CD2} = V_{RES} - V_{DSM1} - V_{DSM2} \tag{3}$$

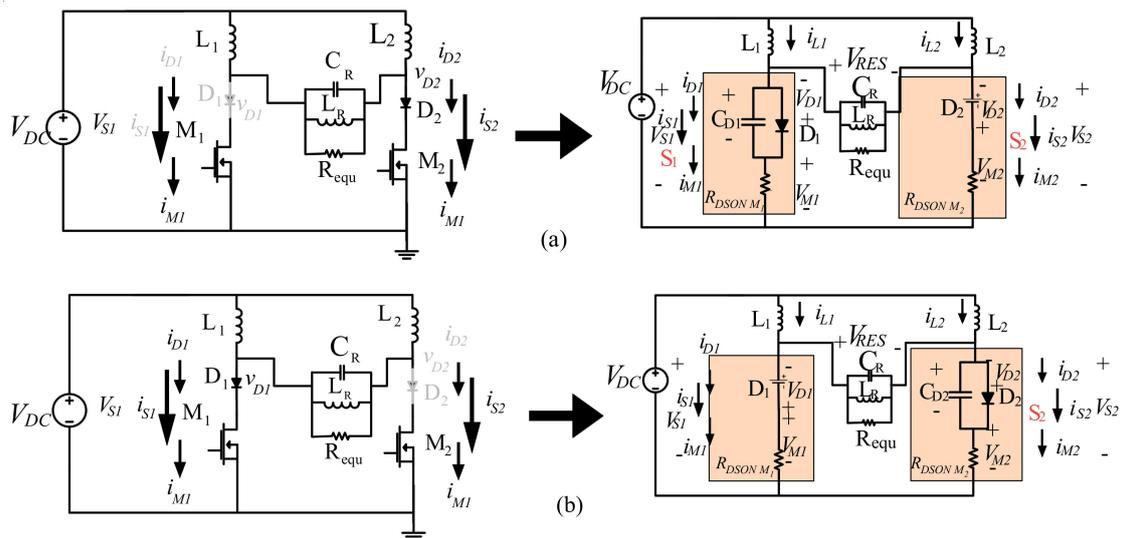


Figure 4. Cont.

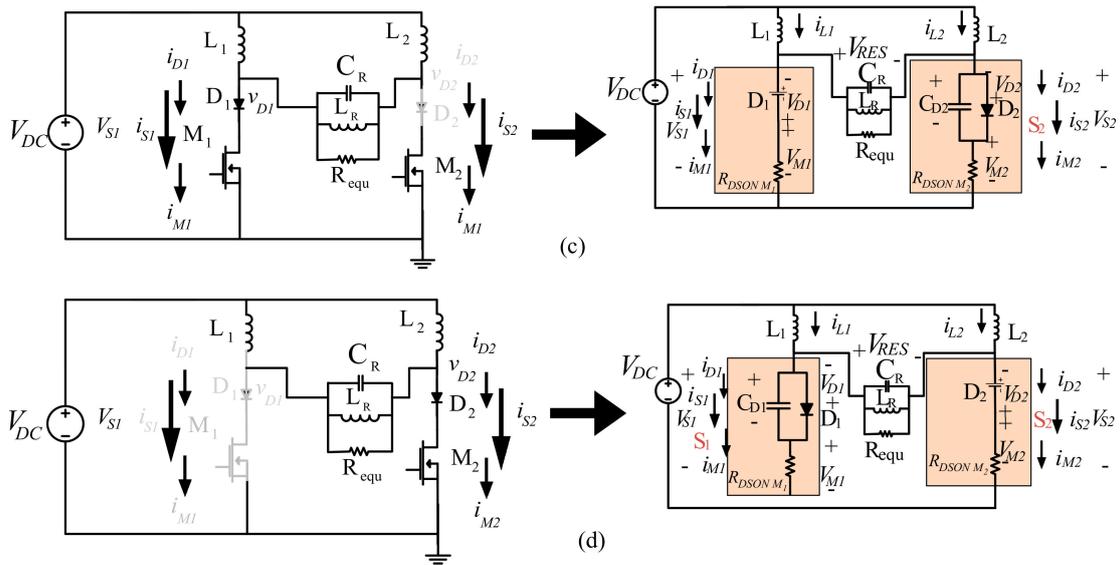


Figure 4. Equivalent circuits; (a) from t_0-t_1 , (b) from t_1-t_2 , (c) from t_2-t_3 , (d) from t_3-t_4 .

From Figures 3 and 4, the behavior given by the recovery time in D_1 and D_2 during their shutdown states causes D_1 and D_2 to be in the on-state even when M_1 and M_2 are in the off-state, which indicates that if the complete switch is analyzed, the MOSFET and diode do not share the same shutdown time. Furthermore, in MODE A, i_{S2} increases, and the stray capacitance in D_1 is discharging, causing i_{S1} to decrease to zero, then, the current i_{S1} increases its value because the current i_{S2} decreases. This current will be zero, until the voltage in D_2 is zero again.

In this sense, when the voltage in D_2 is zero, the current i_{S2} will increase, therefore, this is the main reason to generate hard switching in the complete switch. On the other hand, the power losses achieved in the simulation by S_1 plus S_2 are 31 W with a global efficiency of 62% and a time delay between gate-signals of 0.49. It is important to estimate the applied overlap. Therefore, Figure 5 shows the overlap to consider in the analysis.

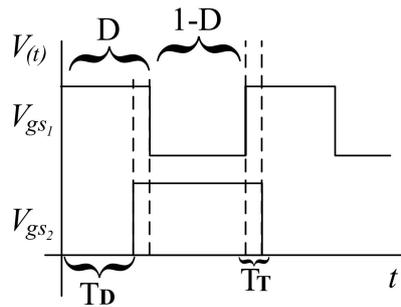


Figure 5. Overlapped signals in M_1 and M_2 .

From Figure 5, D is the applied duty cycle, the time delay between the gate-signals of M_1 and M_2 (V_{GSM1} and V_{GSM2}), and represents the overlap time when M_1 and M_2 are in the on-state. As mentioned, T_T is defined in Equation (4) and T_D is defined in Equation (5).

$$T_T = D - (1 - D) \tag{4}$$

$$T_D = D - T_T \tag{5}$$

Replacing (4) into (5) and considering that the energy transferred to the load depends on the duty cycle, the selected duty cycle of the resonant tank is 0.5.

$$T_D = \frac{2D - 2D + 1}{2} \tag{6}$$

$$T_D = \frac{1}{2} \tag{7}$$

To assess the combination of power semiconductor devices in the unidirectional switch and to verify Equation (7) based on the parameters and design methodology described above, three different converters are designed combining Si-MOSFET and diode (first array), SiC-MOFET and diode (second array), and GaN-transistor SiC-diode (third array). The power devices are selected based on the stress level calculations as well as the similarity in the electrical ratings between the Si and SiC devices (as a result of the reduced drain to source voltage in the GaN-transistor), parasitic capacitances, current rating, switching speed, on-resistance, maximum junction temperature, and following the primary comparison between the characteristics of every device [50,51], mainly focused in the work presented in [52]. Therefore, Table 4 shows the specifications of each power device used in the design.

Table 4. Characteristics of the power semiconductor devices.

Model	Device	Characteristics	Material
EPC2007C	Transistor	V_{DS} (V)	100
		I_D (A)	6
		$R_{DS(on)}$ (Ω)	0.03
C2M0160120D	MOSFET	V_{DS} (V)	1200
		I_D (A)	19
		$R_{DS(on)}$ (Ω)	0.160
C4D08120	Diode	V_{RRM} (V)	1200
		I_F (A)	6.4
		T_J ($^{\circ}$ C)	175
STF12N120K5	MOSFET	V_{DS} (V)	1200
		I_D (A)	12
		$R_{DS(on)}$ (Ω)	0.69
STTH812	Diode	V_{RRM} (V)	1200
		I_F (A)	8
		T_J ($^{\circ}$ C)	175

Figure 6 shows the efficiency versus variations in T_D performed by different power semiconductor devices obtained in the simulation.

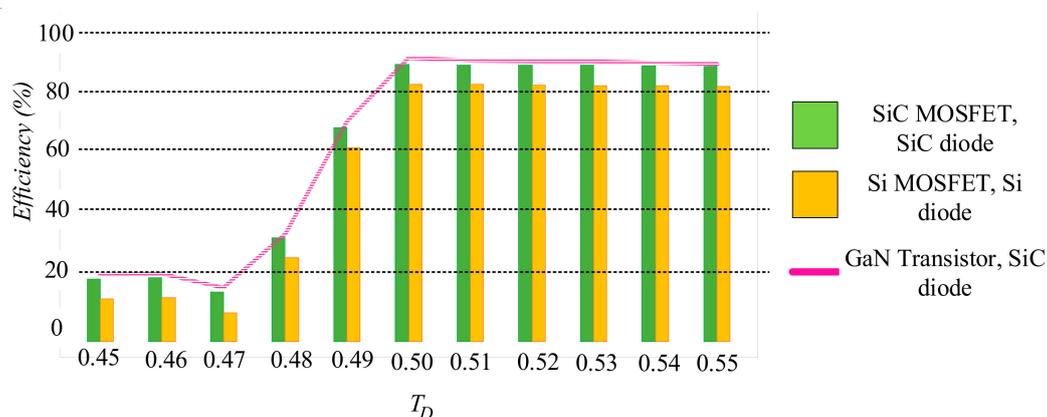


Figure 6. Efficiency versus time delay (T_D) with different power devices.

According to Figure 6 and considering $T_D = 0.5$, a global efficiency and total power losses (switching plus conduction) in S_1 plus S_2 of 86% and 27 W were performed by the Si-MOSFET and Si-diode combination. Furthermore, SiC-MOSFET plus SiC-diode performed an efficiency and power losses in S_1 plus S_2 of 92.7% and 14 W, respectively. Finally, the performance given by the combination of GaN-transistor plus SiC-diode were similar to the combination of SiC-MOSFET plus SiC-diode with an efficiency of 94% and power losses in S_1 plus S_2 of 11 W.

Moreover, the performance given by the overlap dramatically affects the efficiency of the whole converter, thus, it is suggested to take into account an overlapped control in a CFRC since the problems associated with the discharging of the transistor output the capacitance (C_{out}). When the switch voltage increases, the MOSFET (M_1) C_{out} is charged via D_1 to the peak value of the switch voltage, and then remains at that voltage until the transistor turns on. At this time, the capacitance C_{out} is discharged through the transistor, resulting in switching loss. According to Figure 6, with T_D estimated to be 0.5, the power losses in S_1 plus S_2 and global efficiency performed by SiC-MOSFET plus SiC-diode were 14 W and 92.7 %, which performance is reasonably similar in comparison with the combination of GaN-transistor plus SiC-diode. In this way, the complete simulation results achieved from the DC-DC resonant converter performed by SiC-MOSFET plus SiC-diode are presented in Figure 7.

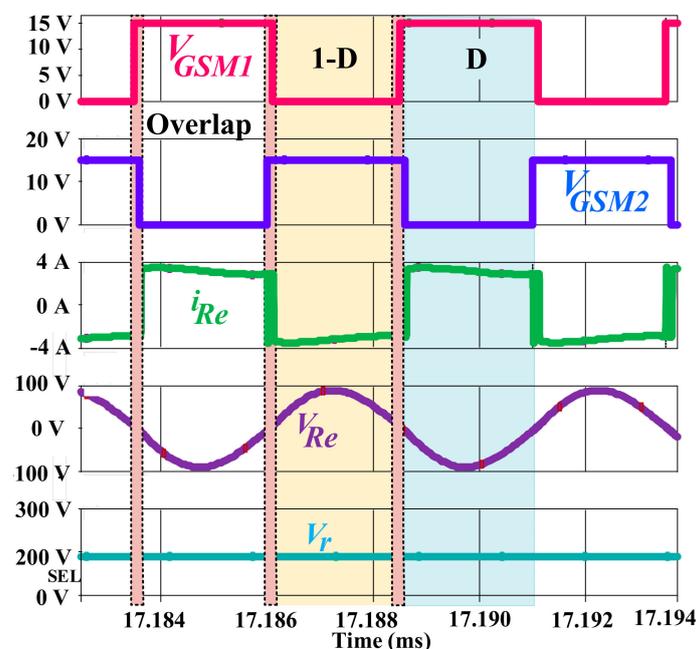


Figure 7. Waveforms of the DC-DC resonant converter: gate-signals (V_{GSM1} and V_{GSM2}), input voltage, and current at the resonant tank (i_{Re} and V_{Re}) and output voltage (V_r).

The key waveforms from the resonant tank in Figure 7 show the previously calculated overlap of M_1 and M_2 . Alternatively, both the input current (i_{Re}) and voltage (V_{Re}) at the resonant tank show a condition close to resonance since both signals are in phase. Furthermore, the output voltage (V_r) is 207 V, which indicates that the parameters proposed in Table 2 have a relative error of 1.42% between them and the simulation results.

On the other hand, with the aim to compare the performance and conditions given for the topology, a comparison of a non-overlapped (Figure 8a) and overlapped control (Figure 8b) was made, focusing its attention on v_{S1} and i_{S1} .

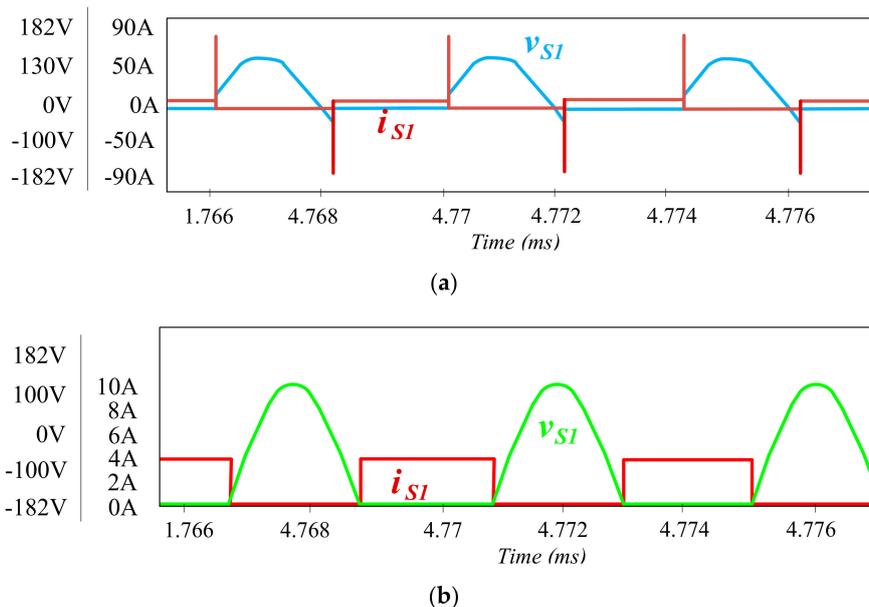


Figure 8. Signals: (a) current and voltage on S_1 with a non-overlapped control, (b) current and voltage on S_1 with an overlapped control.

From Figure 8a, with a non-overlapped control, not only the voltage and current on S_1 , but also the resonance condition will be dramatically affected, causing negative voltages, as shown in Figure 8a. This issue would affect the entire efficiency because an overlap control provides a ramp shift signal to the ramp generator in response to a detection signal that indicates activity of the switches in the power stage. The ramp shift signal adjusts the first and second ramp signals relative to each other so as to minimize any gap and any overlap between the first and second ramp signals.

In this way, to have a good relation overlap-efficiency, an important point to consider is to work with an overlapped control to have optimal conditions, as shown in Figure 8b. Furthermore, Figure 8b shows less power losses as a result of the less current peaks obtained in comparison with the non-overlapped behavior presented in Figure 8a.

3. Experimental Results

Based on Tables 2 and 3, the experimental prototype was elaborated. For experimental results, power devices used in the different combinations are shown in Table 4. Inductors were designed based on the Kg methodology [53], the PWM control optimized for high switching frequency, and the drivers used were UC3825 and MIC4452, respectively. Furthermore, $T_D = 0.5$ was considered. The elaborated prototype is shown in Figure 9.

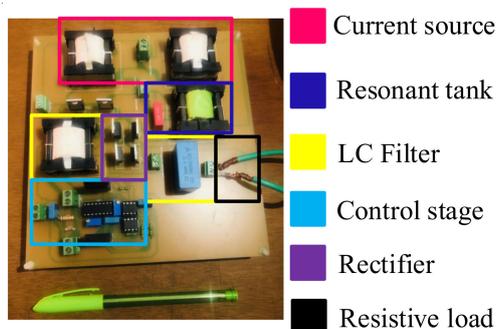


Figure 9. Current fed DC-DC resonant converter implemented.

Developing the experimental prototype at maximum power, the experimental results under different combinations of power devices are briefly described below by applying the OHMITE Rheostat RRS250E as a resistive load, which can be operated at a maximum ohmic and power value of 250 Ω and 500 W, respectively:

3.1. Overlap and Performed Efficiency by Si-Based Power Devices

For the first analysis, Figure 10 shows the overlapping signals (gate-source voltage) between M_1 and M_2 .

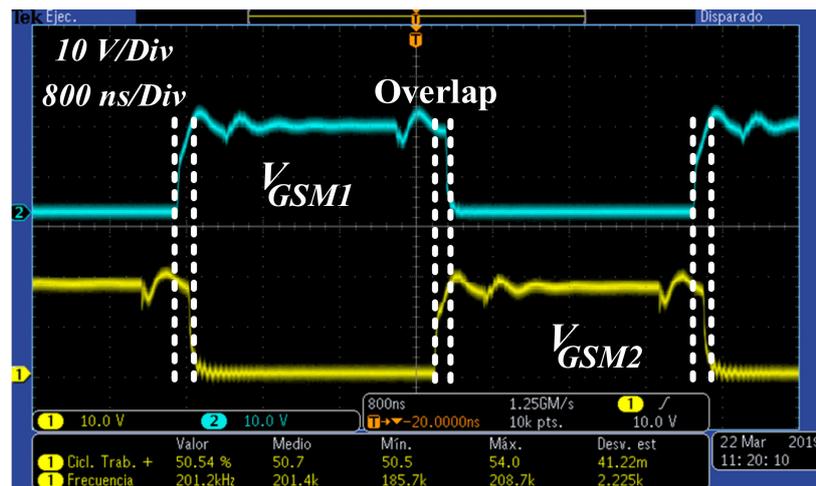


Figure 10. Overlapping signals performed for the first array.

From Figure 10, the performance given for silicon devices presents disturbances in the gate-signal modulation derived by the parasitic capacitance of each MOSFET. This noise will be reflected in the resonant tank. Moreover, S_1 and S_2 will be affected because of the reverse recovery current of D_1 and D_2 , which will be reflected in the drain current of M_1 and M_2 .

Additionally, it is well-known that Si power devices present a greater variation of non-linearity behavior of the output capacitance, whereas the low voltage part of the output capacitance increases due to higher area specific density. The high voltage part of the output capacitance decreases with the area shrink factor of the device, increasing the power losses and consequently affecting the overall performance of the converter. In this way, there is a need to study the performance given by new power devices technologies that permit a reduction of the high voltage part of the output capacitance leads to significant lower energy values being stored in it, because turning off Si devices with lossless would require to turn off the channel current before the voltage significantly rises across the device. The shape of the output capacitance, being charged by the full load current, will determine the voltage waveform. Conversely, the gain in the energy stored in the output capacitance, being dissipated as heat in hard switching applications during turn-on, is hence correlated to an increase of switching frequency. On the other hand, the overlapped signal in Figure 10 shows an operation frequency of ≈ 200 kHz, considering a duty cycle of 50%. In contrast, another important parameter is to determine the electrical efficiency; therefore, Figure 11a shows the input (P_{in}) and output power (P_{out}) as well as the efficiency (Figure 11b) obtained in the implemented topology.

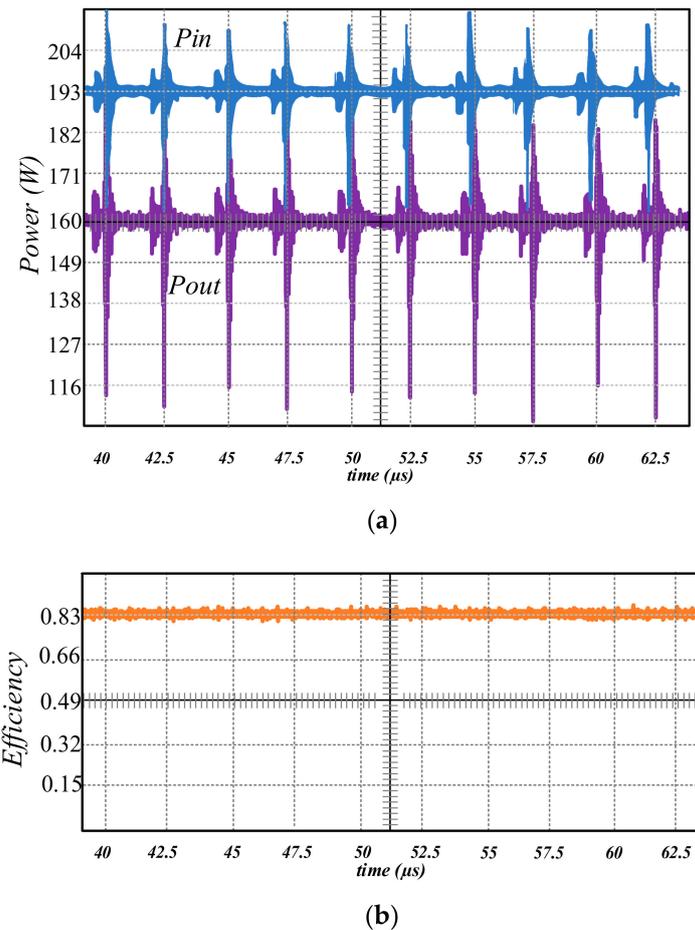


Figure 11. Electrical signals implemented by the first array: (a) input and output power, and (b) efficiency.

According to the results, the converter efficiency is 83% and the loss is 32.8 W, which are significant. Additionally, as a result of the efficiency obtained with an optimized $T_D = 0.5$, all losses were calculated to assess the electrical performance in all elements. To evaluate the passive elements, references [54] and [55] were used. In the case of capacitors, the loss is primarily from the equivalent series resistance (ESR), which is typically provided in the datasheet. Finally, the total power losses in MOSFETs are composed of switching and conduction losses; on the other hand, the total power losses in diodes are the sum of conduction, reverse, and switching losses. In this manner, Table 5 presents the total power losses on all elements of the experimental prototype, which parts of the estimated results were obtained from [34,36,55].

Table 5. Total power losses distribution by applying Si power devices.

Component	Power Losses (W)
Current source L_1 and L_2	1.2
Inductor L_C	1.33
Rectifier	4
Transformer	4.2
S_1 and S_2	19.4
Stage control and wiring	2.7

From Table 5, S_1 and S_2 present the higher total power losses, which indicates a similarity with the analysis presented in Section 2. Alternatively, in order to determine the distribution of power losses on the unidirectional switch, a study is presented in Section 4.

3.2. Overlap and Performed Efficiency by SiC-Based Power Devices

The second converter was developed by applying the second array of power devices. Figure 12 shows the gate-source voltage. Compared with Si devices, the overlap presented shows a reasonably better performance. The results show less disturbances in the gate-signal modulation derived by the parasitic capacitance of M_1 and M_2 , since SiC devices present vertical current flow from the top surface to the bottom surface and have a blocking pn-junction with injection of bipolar carriers in reverse operation. In this sense, the reverse recovery charge is more than one magnitude lower than in corresponding silicon devices.

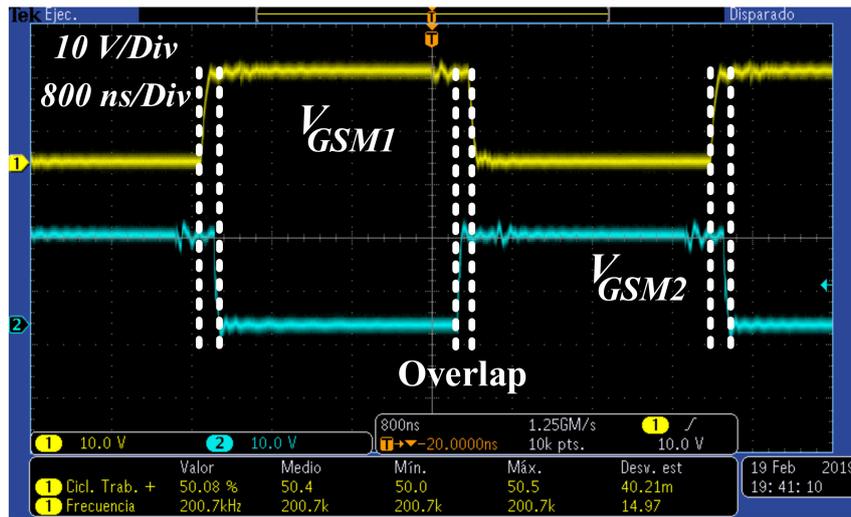
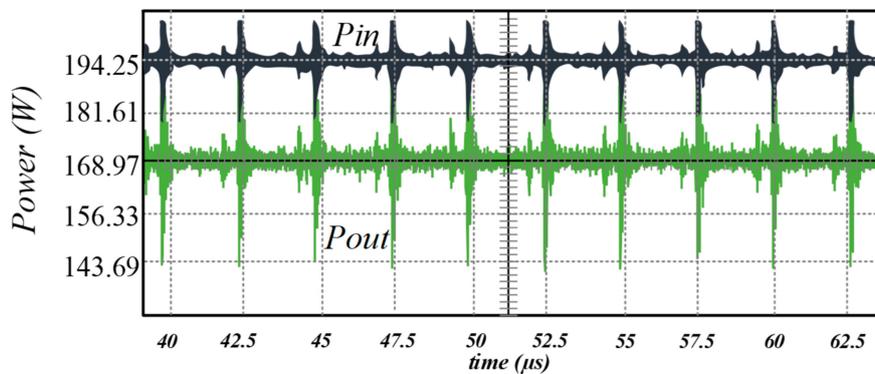


Figure 12. Overlapping signals performed for the second array.

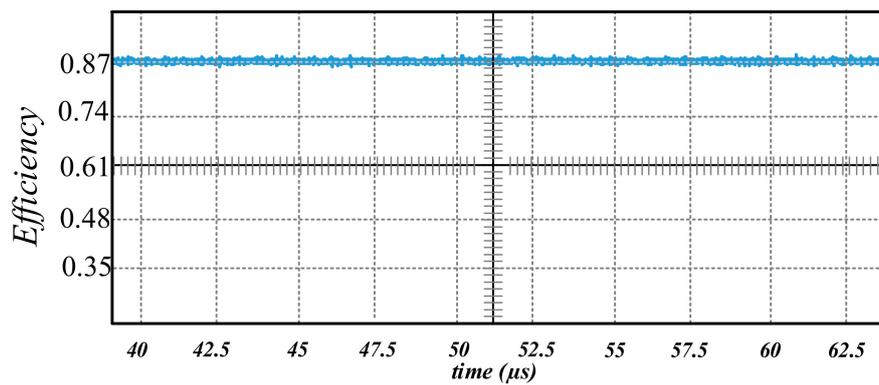
The results from Figure 12 make SiC components very suitable for applications with continuous hard commutation of the body diode as shown in the efficiency obtained (Figure 13b) according to the input and output power (Figure 13a). Furthermore, since the output capacitance is lower than in Si-based power devices, the stored energy in the output capacitance is comparable to GaN HEMTs semiconductors.

According to the results, the CFRC presents an incremented efficiency of 4% in comparison with Si devices. This results in 87% efficiency and losses of 26 W, which are quite significant. The distribution of these power losses is described in Table 6.



(a)

Figure 13. Cont.



(b)

Figure 13. Electrical signals of the second array (a) input and output power, (b) efficiency implemented.

Table 6. Total power losses distribution by applying SiC power devices.

Component	Power Losses (W)
Current source L_1 and L_2	1.1
Inductor L_C	1.31
Rectifier	3
Transformer	4
S_1 and S_2	14
Stage control and wiring	2.56

From Table 6, the performance given by SiC power devices presents a better performance in comparison with Si-based power technology. In fact, the percentage power reductions in comparison with the first array are shown in Table 7.

Table 7. Power reduction percentage; first vs. second array.

SiC Vs. Si	L_1 and L_2	L_C Inductor	Rectifier	Transformer	S_1 and S_2	Stage Control
	8.33%	1.50%	25.00%	4.76%	27.84%	5.19%

From Table 7, the components with the highest change are S_1 and S_2 with a considerable reduction of 27.84%, which results will be compared in Section 4.

3.3. Overlap and Performed Efficiency by GaN-Transistor and SiC-Diode

The third CFRC is designed considering the third array. Alternatively, since the topology under study is capable to works on a switching frequency of up to 200 kHz, a considerable reduction of the total power losses on the switch is not expected as a result of the reduction of the parasitic capacitance in the GaN-transistor. In this sense, the overlapping signals between M_1 and M_2 are shown in Figure 14.

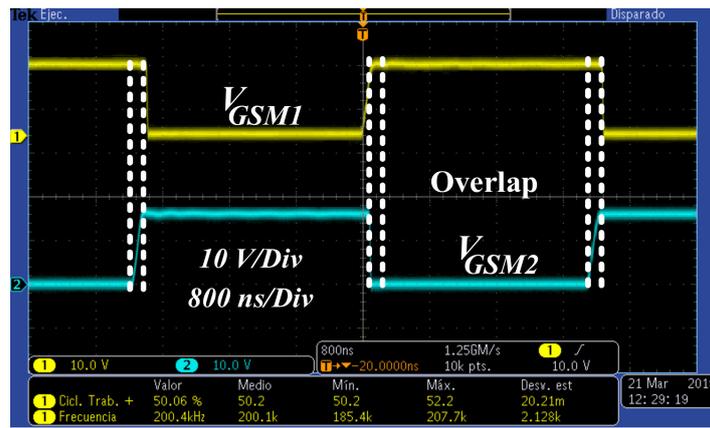


Figure 14. Overlapping signals performed for the third array.

Based on Figure 14, the overlap signals in M_1 and M_2 show a better performance by applying GaN-transistors because of the zero reverse recovery charge, which starts when the drain voltage falls below the sum of the gate potential and the threshold voltage, thus creating a reverse channel. This unique characteristic makes GaN-transistors the first choice for applications with continuous switching on a reverse biased device such as in half-bridge or full-bridge configurations. However, GaN power devices represent the best solution for high switching frequency applications. In this way, SiC power devices have similar efficiency and qualities by applying the same switching frequency in the CFRC presented in this work as shown in Figure 15.

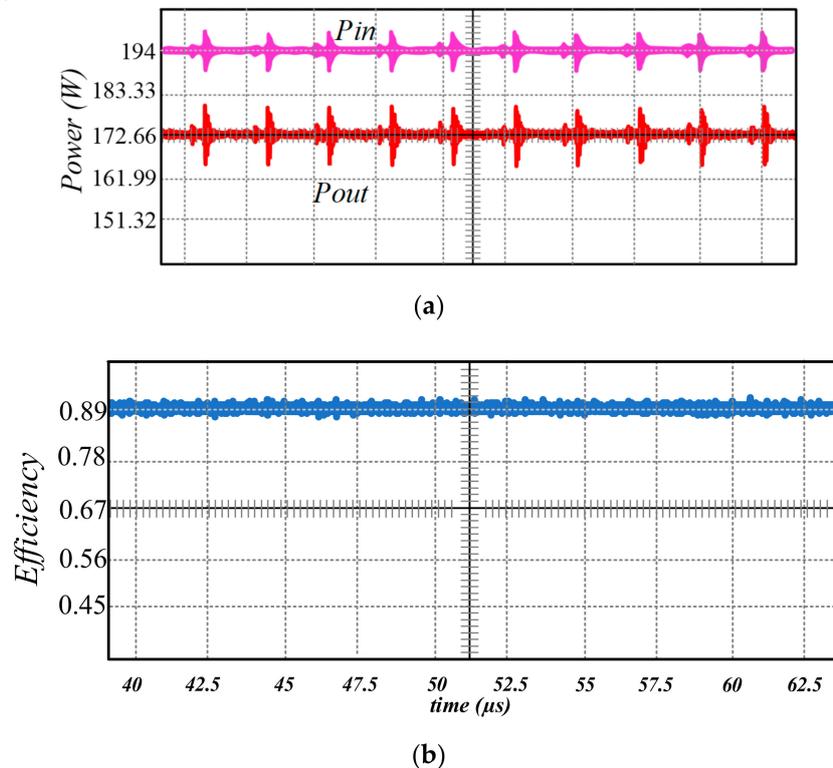


Figure 15. Electrical signals of the third array (a) input and output power, (b) efficiency implemented.

According to Figure 15, the converter has an efficiency of 89% and losses of approximately 21.34 W. The power losses distribution is presented in Table 8.

Table 8. Total power losses by applying GaN and SiC power devices.

Component	Power Losses (W)
Current source L_1 and L_2	1
Inductor L_C	1.265
Rectifier	3
Transformer	3
S_1 and S_2	11
Stage control and wiring	2.12

From Table 8, the performance given by the combination of GaN-transistor and SiC-diodes presents a better performance in comparison with Si and SiC-based power technologies.

In this way, the power reduction percentage in comparison with Si and SiC power devices are shown in Tables 9 and 10, respectively.

Table 9. Power reduction percentage; first vs. third array.

GaN Vs. Si	L_1 and L_2	L_C Inductor	Rectifier	Transformer	S_1 and S_2	Stage Control
	16.67	4.89	25.00	28.57	43.30	21.48

Table 10. Power reduction percentage; second vs. third array.

GaN Vs. SiC	L_1 and L_2	L_C Inductor	Rectifier	Transformer	S_1 and S_2	Stage Control
	9.09	3.44	0.00	25.00	21.43	17.19

From the comparison presented in Table 9, there is a considerable power reduction percentage as a result of the hybrid combination of GaN-transistor plus SiC-diode. Moreover, from the comparison in Table 10, the components with the highest change are S_1 and S_2 with a reduction of 21.43%. On the other hand, not only the losses in power devices are reduced but also in passive elements. The main reason is due to the input current ripple reduction, as shown in the input power ripple in Figures 11, 13 and 15, thus the conduction power losses are reduced. However, the converter electrical efficiency does not increase significantly and remains at approximately 89%. These results will be compared and analyzed in the following section.

4. Switching Loss Analysis

The switching losses of S_1 and S_2 for the different combinations of power devices consist of turn-on and turn-off loss, reverse recovery loss of the body diode, and output capacitance loss (C_{oss}). The output capacitance loss effect is presented when S_1 is in on-state because during both charging and discharging, the loss is generated. Therefore, the total additional loss caused by parasitic capacitances C_{oss} from S_1 and S_2 estimated with the drain-source voltage charged is defined in (8).

$$E_{cap} = \frac{1}{2}C_{oss(S_1)} \cdot V_{dc}^2 + \frac{1}{2}C_{oss(S_2)} \cdot V_{dc}^2 = \frac{1}{2}C_{oss(total)} \cdot V_{dc}^2 \quad (8)$$

where $C_{oss(total)} = C_{oss(S_1)} + C_{oss(S_2)}$ is the total parasitic capacitance of the two switches. Therefore, regarding these issues and based on [56], Tables 8 and 9 show the power loss distribution of S_1 (MOSFET and diode) with $T_D = 0.5$ by applying the different combinations of power devices. In this way, the results for S_2 basically are the complementary losses of S_1 .

According to Tables 11 and 12, the power losses in S_1 and S_2 considering $T_D = 0.5$ show that 60% of the total power losses are caused by D_1 and D_2 . This means that the primary problem caused by the use of unidirectional switches and overlap is related to the high voltages that will be absorbed by the parasitic capacitances of the power devices, increasing switching losses as a result of the diode in

series with the MOSFET, preventing the MOSFET output capacitance from being discharged before the ZVS event.

Table 11. Power losses distribution in MOSFET M_1 .

Component	$P_{\text{Switching}}$ (W)	$P_{\text{Conduction}}$ (W)	Total (W)	Material
STB57N65M5	0.776	3.104	3.88	Si
C2M0160120D	0.56	2.24	2.8	SiC
EPC2007C	0.26	1.04	1.3	GaN

Table 12. Power losses distribution in diode D_1 .

Component	$P_{\text{Switching}}$ (W)	$P_{\text{Conduction}}$ (W)	P_{Reverse} (W)	Total (W)	Material
DSS17-06CR	0.582	2.91	2.328	5.82	Si
C4D08120	0.42	2.1	1.68	4.2	SiC

Conversely, the percentage power reduction of GaN-transistor versus Si and SiC MOSFETs is approximately 66.49% and 53.57%, respectively. Additionally, the percentage power reduction of SiC-MOSFET, SiC-diode versus Si-MOSFET, Si-diode is around 27.84%.

As a result of the use of unidirectional switches in a CFRC, the switching stage will require power devices with low or zero reverse recovery charge, thus showing a clear value proposition for both GaN HEMTs and SiC devices, with both lower stored energies in the output capacitance, faster turn-off, and lower reverse recovery charge. On the other hand, GaN HEMTs power devices show better performance benefits as compared to their SiC counterparts by increasing the switching frequency. However, according to the topology under study, the use of both SiC and GaN power devices present a comprehensive similar performance.

As a result of the combination of Si, SiC, and GaN-based power devices in the CFRC applied to a PV-interconnected system in the DC-DC stage, at moderate switching frequencies, typically below 200 kHz, silicon carbide devices can compete. If switching frequencies move up to 400 kHz or above, the energy stored in the output capacitance will increase. In this case the value of GaN is significantly higher than its silicon counterparts. In fact, the benefits to the use of GaN power devices lies in its significantly lower charge stored in the output capacitance and its perfect linearity of the output capacitance. Additionally, the intrinsic capability to cope with hard commutation events in case of control errors is an additional benefit versus silicon and silicon carbide-based power devices.

5. Conclusions

This paper presents part of the key performance indicators for a CFRC combining Si, SiC, and GaN-based power devices. Regarding losses, one of the main problems associated with the low efficiency is related to the management that the overlap provides on the behavior of the unidirectional switch during the overlap the diode, preventing the MOSFET capacitance from being discharged.

The performance development by the unidirectional switches presents ZVS (Zero Voltage Switching) and ZCS (Zero Current Switching); however, hard switching appears when every device (MOSFET or diode) is analyzed independently. This issue is derived as a result of the energy losses in the parasitic capacitances of the MOSFET and diode. Furthermore, there is a recovery time on D_1 and D_2 in their shutdown states, generating that diodes are on-state even when the MOSFETs are off-state. Therefore, 60% of the total losses are generated by the diodes. Conversely, the percentage power reduction of GaN-transistor versus Si and SiC MOSFETs is approximately 66.49% and 53.57%, respectively. Additionally, the percentage power reduction of SiC-MOSFET plus SiC-diode versus Si-MOSFET plus Si-diode is around 27.84%.

The value proposition of SiC devices relies on the same arguments like for GaN devices with key performance indicators; however, not entirely reaching the level of corresponding GaN power devices for topologies that increase the switching frequency.

On the other hand, compared to conventional topologies, the proposed converter has continuous input current, and thus a capacitor in series with the photovoltaic panel is not necessary. Furthermore, the proposed converter does not present stability problems, and thanks to the arrangement of the parallel resonant tank, the topology provides galvanic isolation.

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