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An Efficient H7 Single-Phase Photovoltaic Grid Connected Inverter for CMC Conceptualization and Mitigation Method

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Abstract: Transformerless inverters are the economic choice as power interfaces between photovoltaic (PV) renewable sources and the power grid. Without galvanic isolation and adequate power convert design, single-phase grid connected inverters may have limited performance due to the presence of a significant common mode ground current by creating safety issues and enhancing the negative impact of harmonics in the grid current. This paper proposes an extended H6 transformerless inverter that uses an additional power switch (H7) to improve common mode leakage current mitigation in a single-phase utility grid. The switch with a diode in series connection aims to make an effective clamp of common mode voltage at the DC link midpoint. The principles of operation of the proposed structure with bipolar sinusoidal pulse width modulation (SPWM) is presented and formulated. Laboratory tests' performance is detailed and evaluated in comparison with well-known single-phase transformer-less topologies in terms of power conversion efficiency, total harmonic distortion (THD) level, and circuit components number. The studied topology performance evaluation is completed with the inclusion of reactive power compensation functionality verified by a low-power laboratory implementation with 98.02% efficiency and 30.3 mA for the leakage current.

Keywords: common mode inverters; photovoltaic; leakage current elimination; pulse width modulation

1. Introduction

The energy demand for industrial, commercial, and residential consumers is a fact in the 21st century. One way to accomplish this demand without harming the environment has been seen through the incorporation of distributed generation (DG) systems in distribution networks. Large and as well as small-scale photovoltaic (PV) arrays for home applications have become popular rather than other DG sources due to the improvement in manufacturing techniques and significant advances in power electronic interfaces. Electrical energy produced by a PV installation is basically a DC system. Therefore, it must be converted into AC power to make it available in power utility through a grid-tie inverter [1–3]. Transformerless voltage source inverters (VSIs) are the standard choice in detriment of current source inverters (CSIs), because they show better conversion efficiency, smaller size, and lower manufacturing costs for the same power rating. Transformerless inverters generally have two classes of connection such as galvanic or non-galvanic categories. When a high-frequency low-size transformer on the DC side or low-frequency large-size transformer on the AC side are used, the electric connection is removed, which means electrical isolation between the two electrical systems [4]. This electrical separation improves operation security and reliability. However, it deteriorates power conversation

efficiency. If the transformer is removed (following protection guidelines [5,6]), renewable power generation investment cost is considerably lower. Many studies have been conducted so far on this issue to explain how common mode current (CMC) could be surpassed [7]. CMC circulation is only possible, since there is no galvanic isolation which, combined with the stray capacitance that appears between PV installation and the DC side ground, allows a path for ground current to be injected into the neutral point at the AC side. The stray capacitance level may depend on:

- Class of PV cells;
- Climate type and residential localization;
- The height between PVs and ground on the DC side;
- Voltage level; and
- Electromagnetic Interference (EMI).

To guarantee grid reliability, modern grid-connected PV standards propose leakage current protection device actuation according to CMC amplitude. This means that CMC values below 300 mA are permanently acceptable, while above this point, the protection must react and trigger a break by isolating the transformerless inverter from the utility grid. Furthermore, this current must not continue over 0.3 s during the operation scheduling period. If the CMC increases, the maximum permissible time to trip will be decreased, correspondingly. Table 1 depicts the recommended tripping time as a function of CMC amplitude.

Table 1. Maximum common mode current (CMC) [7].

RMS Value	Automatic Disconnection Time
CMI > 300 mA	0.3 s
CMI > 450 mA	0.15 s
CMI > 800 mA	0.04 s

To eliminate the leakage current presence, several topologies have been studied and analyzed in the literature, which are shown in Figure 1. The Karschny structure depicted in Figure 1a [8] is based on an asymmetrical output inductor. The topology works at low voltage on the DC side being configured to be operated in two different modes. In one half cycle, its operation is very similar to a buck converter. On the other hand, when S_1 and S_5 are switching in a complementarily way, the topology operates as a buck-boost converter. This allows generating a semi-pure sinusoidal current. In practical terms, it is not easy to implement because it requires a complex control technique. In addition, the three switches that contribute to the current path lead to an increase in the active power loss. Other forms of proposed topologies are based on dual-buck topologies [9,10], which can be seen in Figure 1b,c. These structures are basically two buck converters that can be connected in series or in parallel being operated complementarily to perform DC decoupling of the current path. Switches S_{L1} and S_{L2} are commuted at a power grid frequency in order to prevent the reversal of the inductor current [10]. The half-bridge-based transformerless inverters as shown in Figure 1d may limit the CMC presence, but at the cost of operating restrictions such as the requirement of the DC input voltage being at least twice that of the utility grid voltage. In addition, from a design point of view, power switch components are subjected to higher voltage stress and require a larger output filter size [11]. In Figure 1e, the neutral point clamped (NPC) VSIs have been recently applied in grid-connected PV systems. Due to its structure, extended switching frequency is possible, allowing in turn smaller filter size calculations and reduced voltage stress on power switches. The NPC inverters can balance the voltage applied to off-biased switches. Despite their advantages, the active power loss is not negligible, taking into account the number of components used [12].

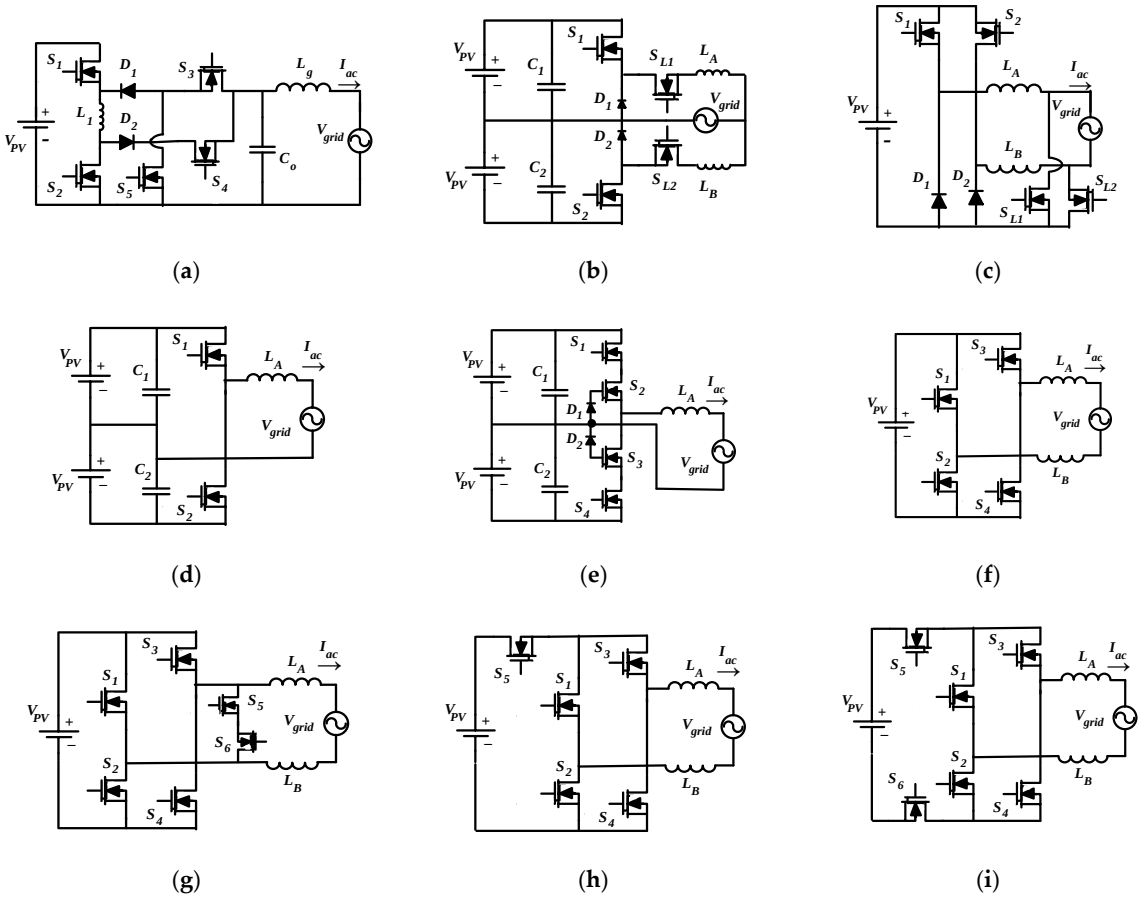


Figure 1. The main configurations of transformerless photovoltaic (PV) inverters in the literature. (**a**) Karschny [8], (**b**) series buck [9], (**c**) parallel beck [10], (**d**) half bridge [11], (**e**) neutral point clamped (NPC) [12], (**f**) full bridge [13], (**g**) highly efficient and reliable inverter (HERIC) [14], (**h**) H5 [15], (**i**) H6 [16].

The full bridge topology represented in Figure 1f that uses symmetrical inductor filters cannot effectively decouple the CMC on the AC side, since high-amplitude CMC is generated with the sinusoidal pulse width modulation (SPWM) technique [13].

A concept known as highly efficient and reliable inverter (HERIC) can be seen in Figure 1g. It comprises a full bridge configuration where two additional high-frequency switches are arranged in opposite directions on the AC side. The freewheel path is also produced by those high-frequency switches in high-efficiency operation. The main disadvantage of HERIC VSI is that the exact regulation of them results in output voltage and current chopping. The H5 topology shown in Figure 1h is obtained from a full bridge converter by incorporating a switch on the DC side to decouple it from the AC side, and therefore suppressing the CMC interference [14,15]. The three upper-side switches are controlled by the power grid frequency, while the rest are under high-frequency signal switching control. In the freewheel condition, only two semi-conductor switches are conducted, but in an active state, three of them are tuned on, which results in large active power loss consequently. Adding an extra switch to H5 topology will make those DC side switches work in pairs and will obtain the H6 topology represented in Figure 1i. However, the modulation performance varies regarding H5 topology and the most important drawback of this structure is the active power loss achieved in conduction operation mode with three switches [16].

This paper is organized as follows: Section 2 presents the CMC conceptualization for a single-phase PV inverter. The mitigation method and CMC evaluations are discussed in Sections 3 and 4, respectively. The design considerations and maximum power point tracking (MPPT) algorithm are presented in

Section 5. Section 6 analyzes the active power loss into two categories: switching and conduction. The simulation results and experiments are conducted in Section 7, and finally, the reactive power compensation is described in Section 8. Briefly, in this paper, a high-efficiency grid-tie inverter structure for non-isolated PV systems is proposed. The main contributions of the presented VSI are briefly mentioned below:

- An extended H6 topology by comprising seven switches, of which five are controlled in high frequency. The remaining switches operate in line frequency modulation to create the freewheel path.
- The 7th switch is used to clamp the common mode voltage; if the voltages ($V_{AN} \approx V_{BN}$) are higher than half of the DC link voltage, freewheeling current flows through S7 and D1 to the midpoint of the dc link, which results in V_{AN} and V_{BN} being clamped at $V_{pv}/2$.
- The maximum power point tracking (MPPT) algorithm based on perturb and observe (P&O) is considered to increase the total system efficiency.
- The AC decoupling strategy has been chosen.
- The unipolar SPWM pattern is applied to gate inputs.
- A reduced filter size is hired to decrease the unsolicited harmonic generated by output current and restrict the total harmonic distortion (THD).

2. CMC Origin in Transformerless Inverter

In the first categories of PV inverter topologies without galvanic connections mentioned before, which may be known as switching inverters or transformerless inverters, many applications are verified. The main drawback of these configurations is the CMC generation, which has appeared between the AC mains and the DC side of the inverter. A general structure of a transformerless PV inverter highlighting the path of $i_{leakage}$ (i_{cm}) is shown in Figure 2. As it can be seen clearly, the common mode current is flowed in a loop that consists of a DC input voltage source or PV arrays voltage, inverter switches, output filter inductances, AC grid, grounding impedance, and parasitic stray capacitances of PV cells. The common mode voltage is the mean of voltages of node A and node B. Besides, V_{dm} is the differential of the aforementioned nodes. Figure 3 has been depicted to represent the simple single-line circuit of the discussing topology in order to calculate the total common mode voltage. Consequently, according to these explanations, it could be expressed with the following equations.

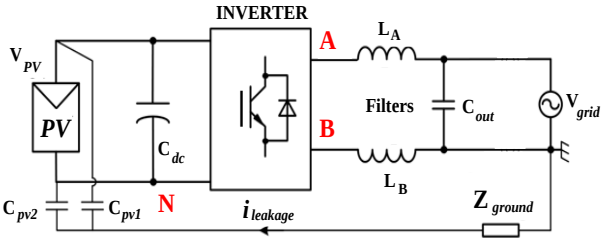


Figure 2. Equivalent circuit of a PV transformerless inverter.

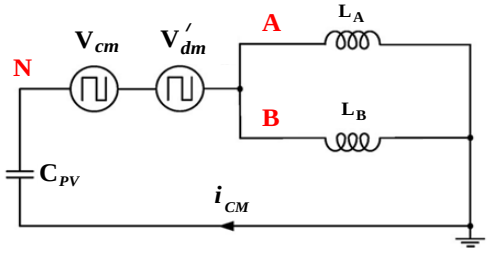


Figure 3. Common mode equivalent circuit.

$$V_{cm} = \frac{V_{AN} + V_{BN}}{2} \tag{1}$$

$$V'_{dm} = \frac{V_{dm}}{2} \frac{(L_B - L_A)}{(L_B + L_A)} \tag{2}$$

$$V_{dm} = V_{AN} - V_{BN} \tag{3}$$

Since i_{cm} appeared due to $V_{t,cm}$ flows in the abovementioned loop, it could be proved that the total common mode voltage is obtained in (4):

$$\begin{array}{c} V_{t,cm} = V_{cm} + \frac{V_{dm}}{2} \frac{(L_B - L_A)}{(L_B + L_A)} \\ = \frac{V_{AN} + V_{BN}}{2} + \frac{V_{AN} - V_{BN}}{2} \frac{(L_B - L_A)}{(L_B + L_A)} \end{array} \tag{4}$$

Clearly, it is observed that the criteria for the elimination of i_{cm} is to make $V_{t,cm}$ remain constant. Thus, we should have:

$$V_{t,cm} = \frac{V_{AN} + V_{BN}}{2} + \frac{V_{AN} - V_{BN}}{2} \frac{(L_B - L_A)}{(L_B + L_A)} = cte \tag{5}$$

In some configurations such as half-bridge family or Karschny inverters and some of those indicated in Figure 1a, only one inductor is used in the output to filter the harmonics, so that the other inductor is equal to zero or does not need to be considered. Thus, by assuming that $L_A = 0$, we find the $V_{t,cm}$ as (6).

$$V_{t,cm} = \frac{V_{AN} + V_{BN}}{2} + \frac{V_{AN} - V_{BN}}{2} \frac{(L_B)}{(L_B)} = V_{AN} = cte \tag{6}$$

If $L_B = 0$, $V_{t,cm}$ will be extracted in (7).

$$V_{t,cm} = \frac{V_{AN} + V_{BN}}{2} + \frac{V_{AN} - V_{BN}}{2} \frac{(-L_A)}{(+L_A)} = V_{BN} = cte \tag{7}$$

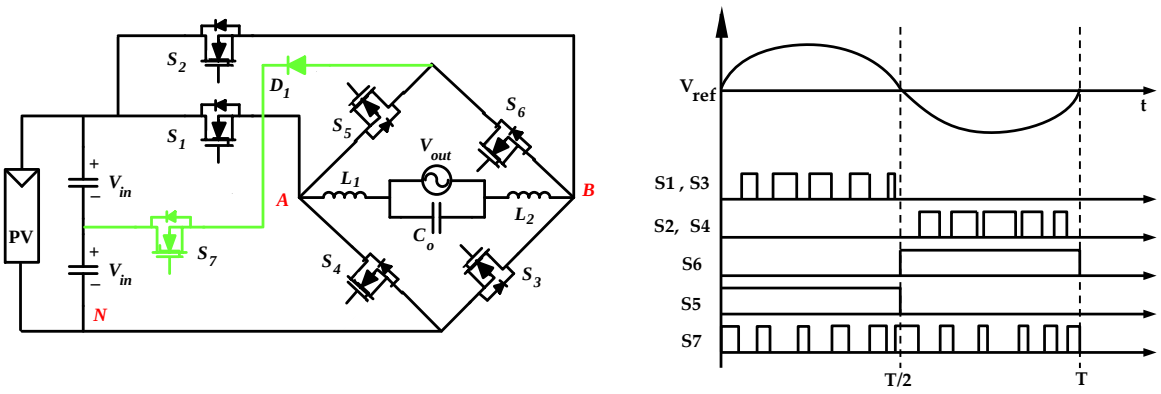
In other PV transformerless inverter topologies, as shown in Figure 1, both inductors L_A and L_B are existing and equal to each other. This equality results in $V_{dm} = 0$. Therefore, to eliminate the leakage current flow, Equation (8) is being obtained:

$$L_A = L_B \rightarrow V_{t,cm} = \frac{V_{AN} + V_{BN}}{2} = cte \tag{8}$$

It is concluded that transformerless VSIs could be categorized into two groups. The first one is called "asymmetrical inductor based inverters", which trust in (6) and (7). Similarly, the second group is named "symmetrical inductor based inverter"; Equation (8) is applied to them.

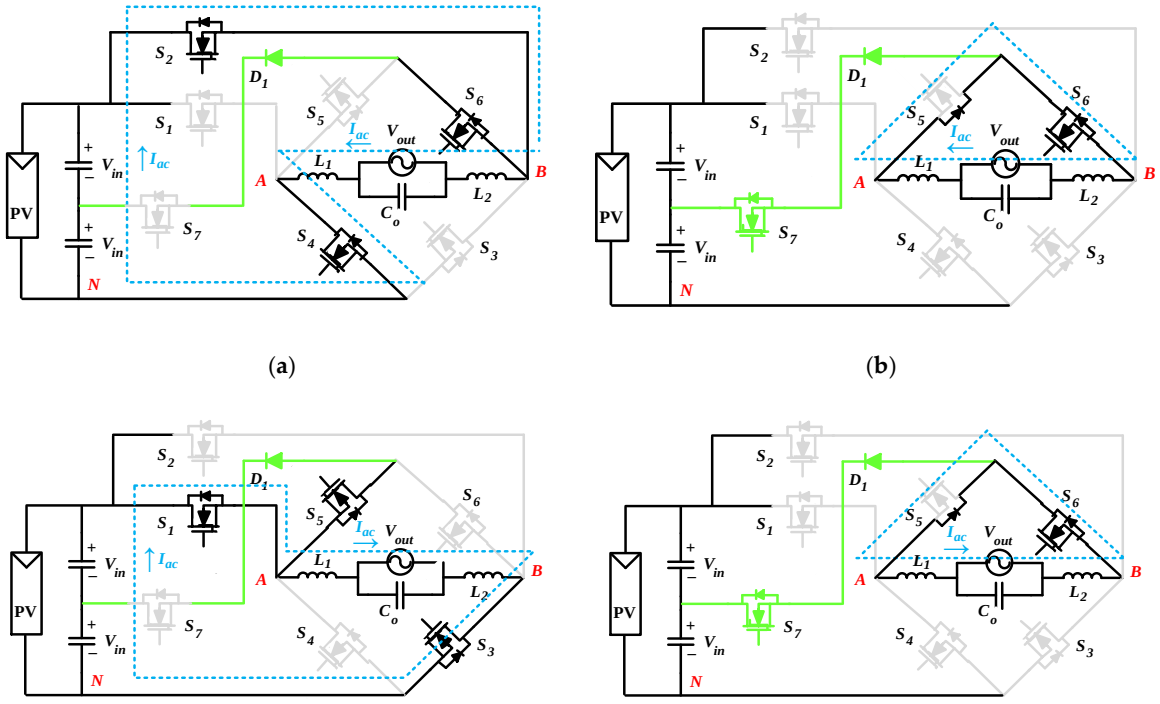
3. H7 Topology and Formal Analysis

The H7 topology combines the main H6 family characteristic with a symmetrical inductor-based inverters group, as shown in Figure 4a. It consists of a full-bridge converter with two inductors, which can generate an appropriate sinusoidal voltage with very low THD. The switches S_1, S_2, S_3, and S_4 operate in high frequency with two remaining switches being turned on/off in line with grid frequency. The switching pattern is depicted in Figure 4b. The proposed suppression process comprises four modes of operation implemented by the control strategy in each period of the power grid frequency. As it can be observed in Figure 4b, switch S_7 is conducting when high-frequency switches S_1, S_2, S_3, and S_4 are turned off. Therefore, S_7 is conducting only in freewheel modes. The operation modes are detailed in Figure 5.



(**a**) (**b**)

Figure 4. (**a**) The proposed topology, (**b**) Switching pattern.



(**a**) (**b**)

(**c**) (**d**)

Figure 5. Currents paths and operation modes of the proposed topology. (**a**) Mode 1, (**b**) Mode 2, (**c**) Mode 3, and (**d**) Mode 4.

3.1. Mode 1, Negative AC Current

In this mode, switches S_1, S_3, and S_5 are turned off, and switch S_6 operates at grid frequency. The SPWM technique is employed to generate the gate signals of the S_2 and S_4 switches. It is supposed that switches S_2 and S_4 are conducted initially. Thus, the AC current flows from the DC part to the AC side through S_2 and S_4. Therefore, voltages V_{AN} is null and V_{BN} sets at V_{pv} input voltage. This mode is detailed in Figure 5a. If the voltages ($V_{AN} \approx V_{BN}$) are higher than half of the DC link voltage, freewheeling current flows through S_7 and D1 to the midpoint of the DC link; as a result, V_{AN} and V_{BN} are clamped at $V_{pv}/2$.

3.2. Mode 2, Negative Freewheel Current

The switches S_1, S_3, and S_5 are in an off state, while the switches S_2 and S_4 remain OFF for short periods of time, as shown in Figure 4b. The common mode leakage current as observed in Figure 5b is not allowed to circulate. Thus, it is temporarily eliminated. As a result, the AC grid is decoupled from the DC PV system. Now, voltages V_{AN} and V_{BN} are brought to the same values around $V_{pv}/2$.

3.3. Mode 3, Positive AC Current

In the next mode, switches S_2, S_4, and S_6 are turned off. Switch S_5 is working under line frequency modulation. Moreover, switches S_1 and S_3 are operated in switching frequency. The switches S_1 and S_3 are conducting, and then, switch S_5 at this moment does not have a closed loop to flow the current. Thus, the current flows from the DC side to the AC side of VSI through S_1 and S_3; therefore, we could figure out $V_{AN} = V_{pv}$ and $V_{BN} = 0$. This mode is depicted in Figure 5c. Similar to Mode 1, if the voltages ($V_{AN} \approx V_{BN}$) are higher than half of the DC link voltage, freewheeling current flows through S7 and D1 to the midpoint of the dc link; as a result, V_{AN} and V_{BN} are clamped at $V_{pv}/2$.

3.4. Mode 4

Mode 4 is characterized by switches S_1 and S_3 being in a turn-off state. This means that the AC current closes through the freewheel loop that comprises the S_5 body diode, switch S_6 in conduction mode, and AC grid (Figure 5d). Due to the closed freewheel path, there is no way for the i_{cm} current path. This operating state leads to $V_{AN} = V_{BN} \approx V_{pv}/2$.

4. H7 Topology Evaluation

In order to evaluate the common mode leakage current impact on the proposed topology, we derived the equivalent circuit of the loop from Figure 6 that imports the novel structure presented in Figure 6. Since the input capacitances C_{PV} are very small, they are not considered for calculation purposes. In addition, C_{out} has no influence in i_{cm} derivation, being discarded, too. Manipulating Equations (1) and (3) can be reorganized as:

$$V_{AN} = V_{cm} + \frac{V_{dm}}{2} \tag{9}$$

$$V_{BN} = V_{cm} - \frac{V_{dm}}{2} \tag{10}$$

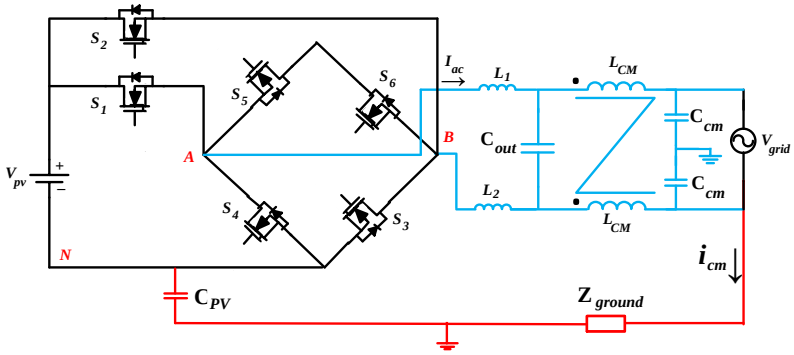
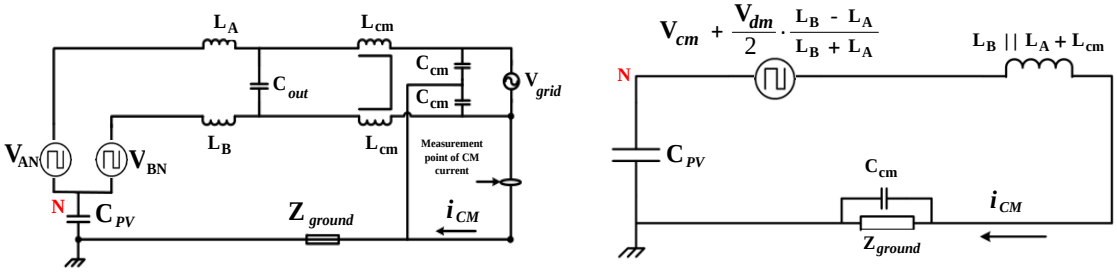


Figure 6. Proposed inverter structure with a common mode path.

Based on that, the CM equivalent circuit of Figure 6 is converted in Figure 7a. Further simplification can be obtained in the form of a single loop arrangement (Figure 7b).



(**a**) (**b**)

Figure 7. (**a**) CM equivalent circuit of Figure 6, (**b**) CMC single loop.

Using the single loop circuit simplification, CM voltage and current values are computed as follows:

(a) In mode 1:

$$V_{t,cm} = \frac{V_{AN}+V_{BN}}{2} + \frac{V_{AN}-V_{BN}}{2}\frac{(L_g-L_g)}{(L_B+L_A)} = \\ = \frac{0+V_{pv}}{2} = \frac{V_{pv}}{2} = cte \quad (11)$$

(b) In mode 2:

$$V_{t,cm} = \frac{V_{AN}+V_{BN}}{2} + \frac{V_{AN}-V_{BN}}{2}\frac{(L_g-L_g)}{(L_B+L_A)} = \\ = \frac{\frac{V_{pv}}{2}+\frac{V_{pv}}{2}}{2} = \frac{V_{pv}}{2} = cte \quad (12)$$

(c) In mode 3:

$$V_{t,cm} = \frac{V_{AN}+V_{BN}}{2} + \frac{V_{AN}-V_{BN}}{2}\frac{(L_g-L_g)}{(L_B+L_A)} = \\ = \frac{V_{pv}+0}{2} = \frac{V_{pv}}{2} = cte \quad (13)$$

(d) In mode 4:

$$V_{t,cm} = \frac{V_{AN}+V_{BN}}{2} + \frac{V_{AN}-V_{BN}}{2}\frac{(L_g-L_g)}{(L_B+L_A)} = \\ = \frac{\frac{V_{pv}}{2}+\frac{V_{pv}}{2}}{2} = \frac{V_{pv}}{2} = cte \quad (14)$$

5. Prototype Design Consideration

This part of the paper is organized in three sections: filter inductance design, filter capacitance selection, and semi-conductor components sketching. In these topologies, typically the maximum ripple of the current is considered between 10% and 25% of the root meat square (RMS) current [17]. Therefore, for a 36 W prototype fed a load with 30 V at 8 kHz switching frequency, the filter inductance is obtained as (15).

$$L_f = T_{on}\frac{V_{pv}-V_{ac}}{2\times\Delta i_{ripple}^{MAX}} \sim 2\ mH \quad (15)$$

where the maximum current ripple is assumed to be 20% of the nominal current. Consequently, the capacitance of the output filter is generally designed based on the cut-off frequency. This frequency is normally between 10% and 20% of the switching frequency [18]. Equation (16) is given to help the selection of filter capacitance.

$$f_{cut-off} \leq (10\% \sim 20\%)\times f_s \\ f_{cut-off} = \frac{1}{2\pi\sqrt{L_g C_{filter}}} \quad (16)$$

Therefore, filter capacitance will achieved as approximately 220 µF. In order to select the semi-conductor components, it is noted to say that in high-frequency conditions, the switches

S_1 to S_4 should work properly. On the other hand, the switches S_5 and S_6 are operated at line frequency. According to peak inverse diode (PIV), total standing voltage (TSV), and nominal parameters of load, the MOSFET IRFP150 was selected as a power switch that could withstand up to 100 V and 40 Amperes as the nominal current. For the diodes configuration, the BY3099 reference was chosen, while the MOSFET driver role is ensured by the ICL 7667. Finally, to guarantee galvanic isolation between the gate signals and power circuit, we used a 6N137 optocoupler [19].

MPPT

The P&O approach is a well-known algorithm to perform the MPPT function. It works by applying a small disturbance in the system; then, the set-point of PV arrays are going to be changed due to tracking the maximum power point. The equation that describes the P&O algorithm operation is shown in (17) [20].

$$\begin{array}{c} MPP_{k+1} = MPP_k \pm \Delta P_{PV} = MPP_k \\ +(MPP_k - MPP_{k-1}) \times sign(\Delta P_{PV}) \end{array} \quad (17)$$

where $\Delta P_{PV} = P_k - P_{k-1}$. The MPPT flowchart of the P&O strategy is shown in Figure 8.

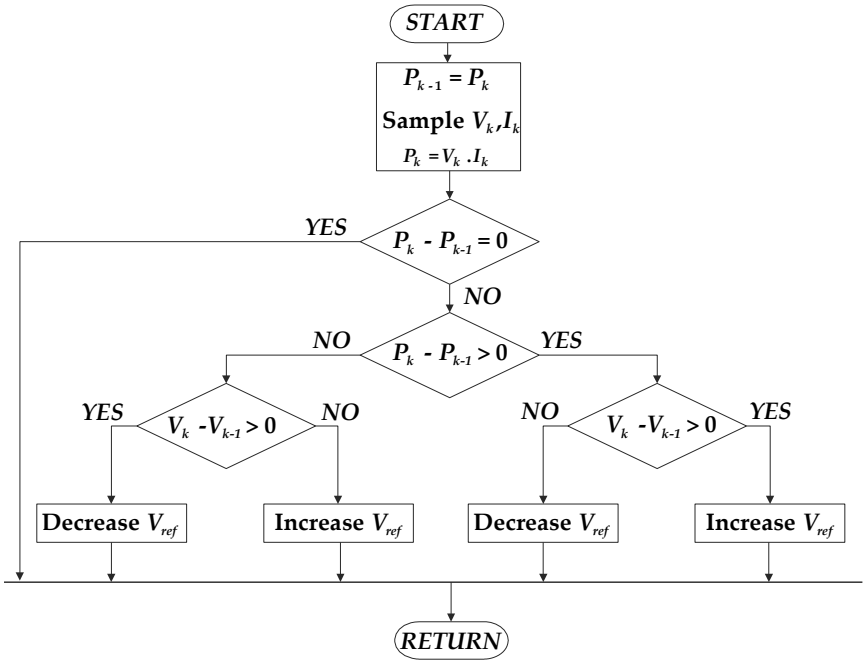


Figure 8. Maximum power point tracking (MPPT) flowchart by perturb and observe (P&O) approach [20].

6. Power Loss Analysis

Since the transformerless VSIs should be operated with maximum power conversion efficiency, the characterization of internal power losses is evaluated in the proposed topology [21]. For a modeling viewpoint, the AC current is given by Equation (18).

$$i(t) = I_m \sin(\omega t) \quad (18)$$

where I_m is the current injected in the power grid and ω is the angular frequency related to the utility frequency.

The voltage drop of these semi-conductors can be divided into two categories (19).

$$\begin{array}{c} V_{ds}(t) = i(t) \times R_{ds} \rightarrow for\ MOSFETs \\ V_{ak}(t) = V_f + i(t) \times R_{ak} \rightarrow for\ Diodes \end{array} \quad (19)$$

where R_{ds} and R_{ak} are the MOSFET and diode conducting resistance and V_f is the forward voltage of diode. Active and zero conditions regarding conduction time T_{active} and non-conduction time T_{zero} of semi-conductor components are given by (20) and (21), respectively.

$$T_{active}(t) = M\sin(\omega t) \tag{20}$$

$$T_{zero}(t) = 1 - M\sin(\omega t) \tag{21}$$

where M is the modulation index.

6.1. Steady-State Conduction Losses

The average conduction loss of MOSFETs and diodes are expressed as (22) and (23), respectively. Since the switches S_5 and S_6 are working at a line frequency, the conduction losses should not be ignored. Average power loss is calculated according to Equation (24).

$$P_{c,MOSFET} = \frac{1}{2\pi}\int_0^{\pi} i(t) \times V_{ds}(t) \times T_{active}(t) \times d(\omega t) = \frac{2M}{3\pi} I_m^2 R_{ds} \tag{22}$$

$$P_{c,Diode} = \frac{1}{2\pi}\int_0^{\pi} i(t) \times V_{ak}(t) \times T_{zero}(t) \times d(\omega t) = I_m V_f\left(\frac{1}{\pi} - \frac{M}{4}\right) + I_m^2 R_{ak}\left(\frac{1}{4} - \frac{2M}{3\pi}\right) \tag{23}$$

$$P_{c,MOSFET,line} = \frac{1}{2\pi}\int_0^{\pi} i(t) \times V_{ds}(t) \times T_{zero}(t) \times d(\omega t) \ = I_m^2 R_{ds}\left(\frac{1}{4} - \frac{2M}{3\pi}\right) \tag{24}$$

6.2. Switching Losses

Ordinarily, the switching losses are calculated by multiplying instantaneous voltage and the current of the commutation state, where they meet each other. This results in (25) and (26) for the evaluation of ON and OFF conditions, respectively.

$$P_{sw,on} = \frac{1}{2\sqrt{\pi}} f_s h I_m^k K_{g_{on}} \frac{V_{ds}}{V_{test}} \frac{\Gamma\left(\frac{k+1}{2}\right)}{\Gamma\left(\frac{k}{2}+1\right)} \tag{25}$$

$$P_{sw,off} = \frac{1}{2\sqrt{\pi}} f_s m I_m^k K_{g_{off}} \frac{V_{ds}}{V_{test}} \frac{\Gamma\left(\frac{n+1}{2}\right)}{\Gamma\left(\frac{n}{2}+1\right)} \tag{26}$$

It is proved $\Gamma\left(\frac{n+1}{2}\right) \div \Gamma\left(\frac{n}{2}+1\right) = \frac{1}{\sqrt{\pi}}\int_0^{\pi} \sin(\omega t)^n d(\omega t)$. Here, coefficients h and k are turn-on energy factors; m and n are turn-off energy factors, K_g is the correction factor to take account of the gate drive impedance, and V_{test} is the test voltage for the model parameters [22]. If the paralleled capacitors of each switch are considered, the charge and discharge losses of them will be given by (27).

$$P_{cap,sw} = \frac{1}{2} C_{MOSFET} V_{ds}^2 f_s \tag{27}$$

The power loss during the reverse recovery period of diode performance due to the switching is estimated by (28). However, the diode reverse recovery current not only contributes to its loss as mentioned above, but it also generates the loss in the main switches as shown in (29) [23].

$$P_{sw,Diode} = \frac{1}{2\pi}\int_0^{\pi}\left(\frac{1}{2}V_{dc}\right)\times\left(\frac{1}{2}I_{rr}\right)\times f_s \times t_b \times d(\omega t) = \frac{V_{dc}I_{rr}f_s t_b}{8} \tag{28}$$

$$\begin{aligned} P_{D_{rr}} &= \frac{1}{2\pi}\int_0^{\pi}\left(\begin{array}{c} I_m.sin(\omega t).t_a \\ +\frac{I_{rr}}{4}(2t_a+t_b)\end{array}\right)\times V_{dc}\times f_s \times d(\omega t) \\ &= \left(\frac{I_m t_a}{\pi}+\frac{I_{rr}(2t_a+t_b)}{8}\right)V_{dc}\times f_s \end{aligned} \tag{29}$$

7. Simulation and Experimental Results

In order to evaluate the H7 topology an inverter prototype was built. It can be seen in Figure 9 the main elements of the inverter system used in bench tests. Table 2 gather the main electrical parameters that characterize the electrical tests. The switching frequency is chosen as 8 kHz and the line frequency is 50 Hz. Figure 10a,b represent the V_{AN} and V_{BN} signals obtained by simulation. Being signals with pulsating periodic waveform, this behavior makes $V_{t,cm}$ constant, as can be verified in Figure 10c. Consequently, the common mode current elimination target is accomplished. For emulating as close as possible a real scenario, it was chosen a stray capacitance of 75 nF. The experimental waveforms are shown in Figure 11, demonstrating the effectiveness of the novel photovoltaic transformerless inverter. The output voltage and load current amplitudes can be checked in Figure 11a. Voltage THD measurement at inverter output is 1.51%, in accordance with the value estimated in simulation whose result is 1.07%. Measured waveforms of V_{AN} and V_{BN} have approximately square waveforms (Figure 11b), confirming that $V_{t,cm}$ is constant (Figure 11c). Finally, in Figure 11d the CMC waveform is presented. Due to experimental device restrictions, DC input voltage of 30 volts conditioned V_{AN} and V_{BN} peak voltage around 30 V. The peak value of the output voltage and current are near 30 V and 1.2 A, respectively. From Figure 11d data the current measured in common mode is approximately 1.14 mA. Some undesirable peaks shown in these pictures appear due to non-ideality in components.

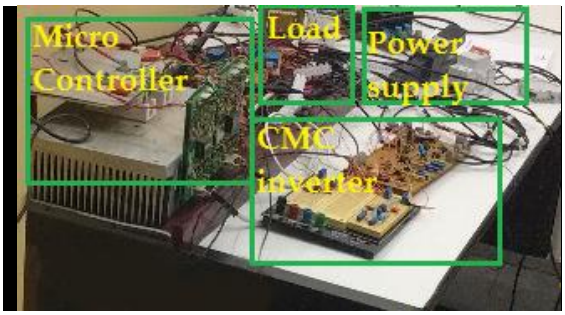


Figure 9. Laboratory setup of proposed H7-type inverter.

Table 3 shows a comparative study concerning the proposed topology with published performance data regarding some well-known single phase inverter structures. The comparison highlights that the H7-type inverter with fewer components can not only reduce significantly the CMC circulation, as well as the power conversion efficiency is one of highest. On the other hand, these results denote that the CMC of the H6 topology is the lowest of all under comparison and the two others' CMC is practically the same. However, the efficiency analysis shown in Figure 12 relies on the best performance of the proposed topology. To illustrate this, it can obviously realized by comparing our topology with those evaluated in active and freewheel conditions. In the active state, the AC current flows through only two switches in the proposed topology, similarly to HERIC-type inverter, while H6 and

H5 topologies require three power switches translating into higher active power loss. In the freewheel state, the H7-type design makes use of only one switch and one diode in line with the H6 structure. The same is not true for the H5 and HERIC converters whose operation depends on the two switches, generating consequently additional power losses.

The California efficiency that is used to calculate the diagrams shown in Figure 12 is supposed to be what is written in (30) [12–15]. Figure 13 shows the total loss of active power through the energy transmission process. As it is understood, the suggested topology has the least loss in equal condition. When the same nominal output power is selected for all topologies, the power loss in terms of nominal load percentages will be changed due to the current drawn. According to Figure 13, the proposed topology has the least power loss among all during load variations.

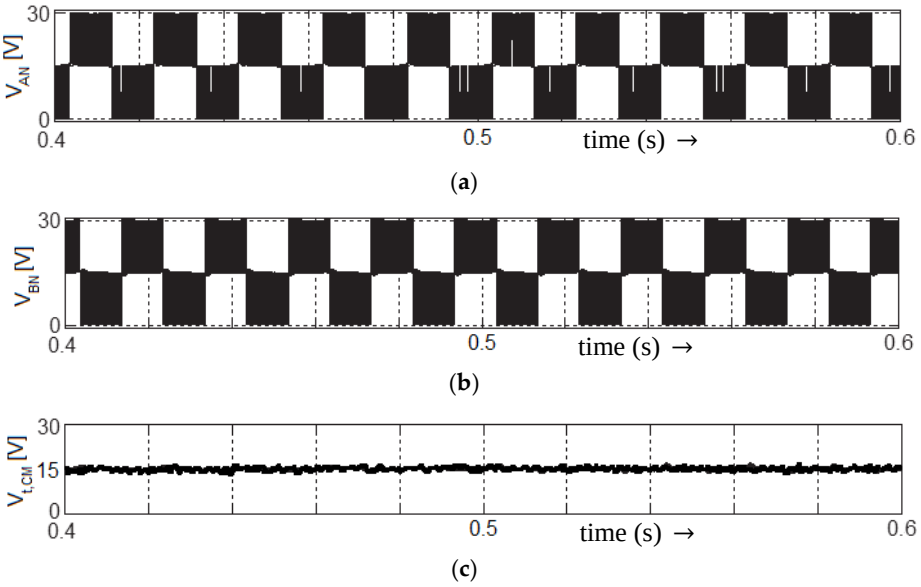


Figure 10. Simulated results of proposed inverter; (**a**) V_{AN}, (**b**) V_{BN}, and (**c**) $V_{t,CM}$.

Table 2. System parameters.

Parameter	Value
V_{dc}	30 V
f_{line}	50 Hz
f_{sw}	8 kHz
P_{out}	36 W
L_f	2 mH
C_f	220 µF
C_{PV}	70 nF

$$\eta = 0.04\eta_{10\%} + 0.05\eta_{20\%} + 0.12\eta_{30\%} + 0.21\eta_{50\%} + 0.53\eta_{75\%} + 0.05\eta_{100\%} \quad (30)$$

Figure 14 shows the percentage of each power loss shared during operation. As discussed before, the proposed topology has a conduction loss that is the same as the HERIC and the freewheel loss is the same as that of the H6 VSIs. The only difference between these converters appears in switching loss calculations. Whereas the rated power is loaded, the share of switching loss in the proposed structure obtains the biggest part among all quotas. This issue does not mean that lots of power transmitted through the VSI is wasted during switching transitions, but this justifies that the power loss could be decreased in terms of switching frequency. Consequently, the total loss will be mitigated in the proposed topology, and its exclusive capability does not appear in other VSIs.

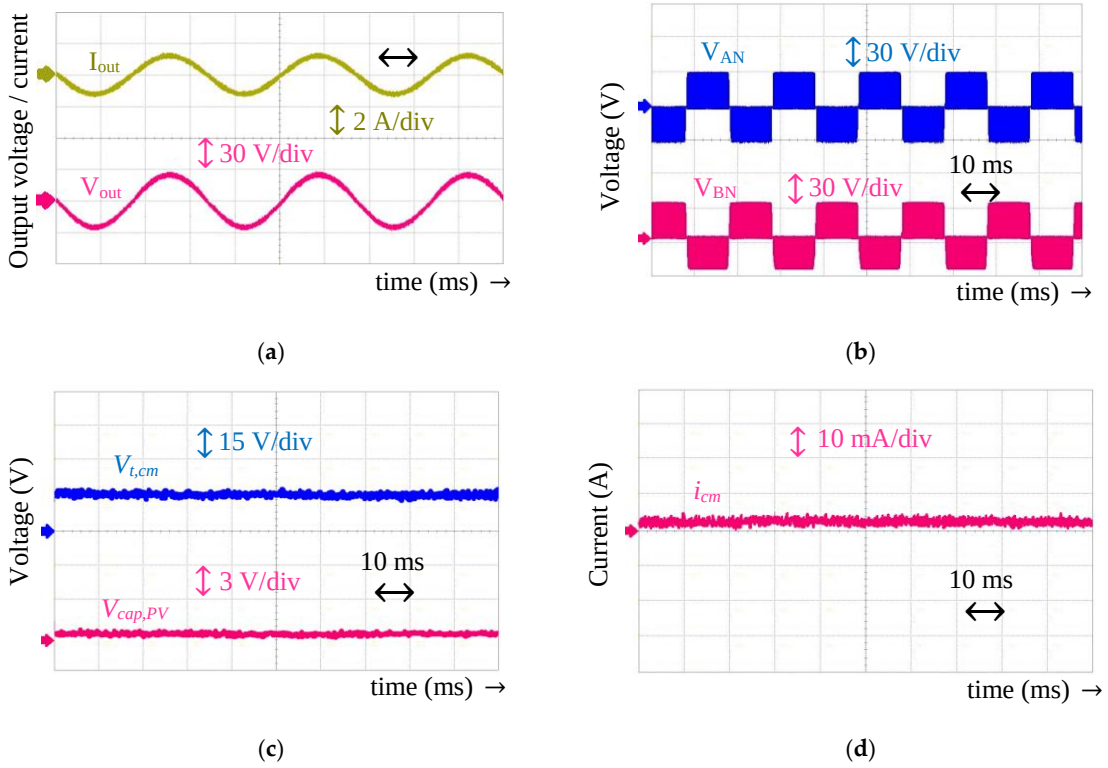


Figure 11. Experimental results; (**a**) output voltage and current; (**b**) V_{AN} and V_{BN}; (**c**) $V_{t,cm}$ (**d**) CMC.

Figure 15 compares the total loss obtained between IGBT and MOSFET utilizations. Since the switching frequency increases, the power loss growths, correspondingly, as expected. However, MOSFTE utilization can decrease the power loss about 40% rather than using IGBT in all switching scenarios. As a result, since the power loss increases as the switching frequency is enhanced, the efficiency will be decreased, subsequently. Figure 16 represents the total efficiency of proposed topology in terms of load power variations, considering switching frequency effects. If the switching frequency is chosen as 30 kHz, the maximum efficiency is obtained as 97.42% in 2.75 kW of output power. However, the maximum efficiency is being calculated as 98.02% for the other switching frequency in $P_{out} = 1.75$ kW. The average efficiency is assessed nearly as 97.1% and 97.85% for $f_s = 30$ kHz and $f_s = 8$ kHz, respectively, in all loading conditions. As the output voltage and current waveforms of experimental results are achieved at 8 kHz switching frequency, due to our laboratory equipment, the output power has been varied between 20 W and 150 W step by step. This verification implies that the proposed prototype is working successfully with high efficiency and reliable performance, as shown in Figure 17. The reactive power and its effect on efficiency is one of the most important concerns in single-phase photovoltaic inverters.

The H7-type VSI is equipped with a capability to control the active and reactive power instantly by the proposed switching pattern. The loading condition is considered as $S_{load} = 44\,W + j\,44\,VAr = 62\,VA$, and the load current is calculated as $|S_{load}|/\ V_{load} = 2.28\,A$. Then, the average and the *rms* amount of current flowing through the diodes and switches are computed, and the loss calculation is obtained as 0.886 W at 8 kHz switching frequency. Then, the effective efficiency of the proposed topology will be figured out as shown in (31).

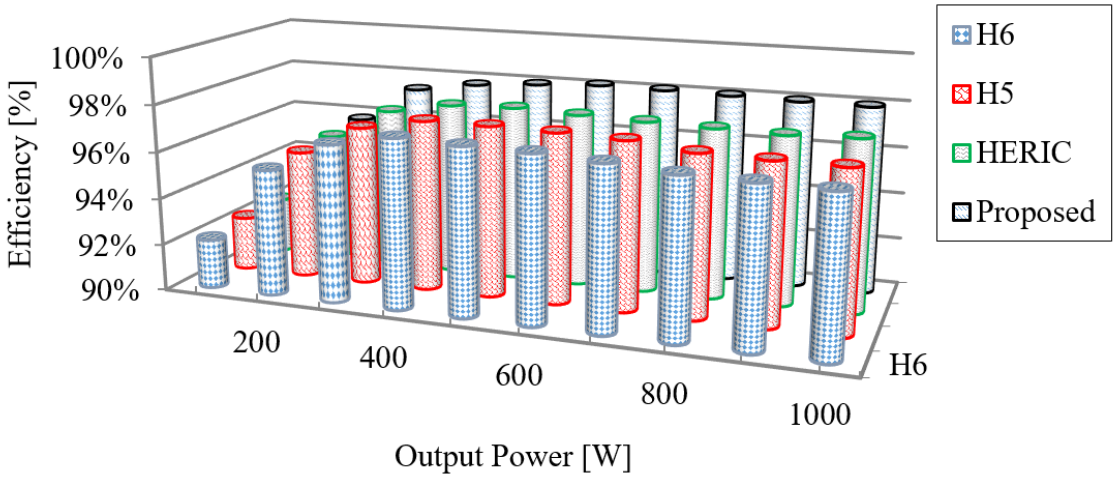


Figure 12. Efficiency evaluation in terms of output power.

Table 3. Comparison as function of components number, total harmonic distortion (THD), i_{cm}, and other properties. HERIC: highly efficient and reliable inverter.

Operation Mode	Component Numbers and Properties Evaluation								
	HERIC [14]	**H5 [15]**	**H6 [16]**	**oH5 ** [24]**	**Ref. [25]**	**Ref. [26]**	**HBZVR * [27]**	**Ref [28]**	**H7**
Active	2 switches	3 switches	3 switches	2 switches	4 switches	2 switches	3 switches	3 switches	3 switches
Freewheel	2 switches	2 switches	1 switch and 1 diode	2 switch and 1 body diode	2 switches	1 switch and 2 diode	1 switch and 1 diode	2 switches	2 switches
THD	1.59%	1.67%	1.84%	1.61%	1.86%	1.69%	1.94%	1.96%	1.75%
Experimental i_{cm}	84.3 mA	89.4 mA	45.8 mA	30.3 mA	51.7 mA	48.9 mA	55.3 mA	67.1 mA	32.5 mA
Capacitor No.	0	0	0	0	0	2	0	0	2
Inductor No.	2	2	2	2	2	2	2	2	2
Maximum efficiency	98.00%	97.87%	97.64%	98.02%	96.36%	97.44%	95.48%	96.15%	98.01%

* HBZVR: H-bridge Zero Voltage Rectifier, ** oH5: optimized H5 topology.

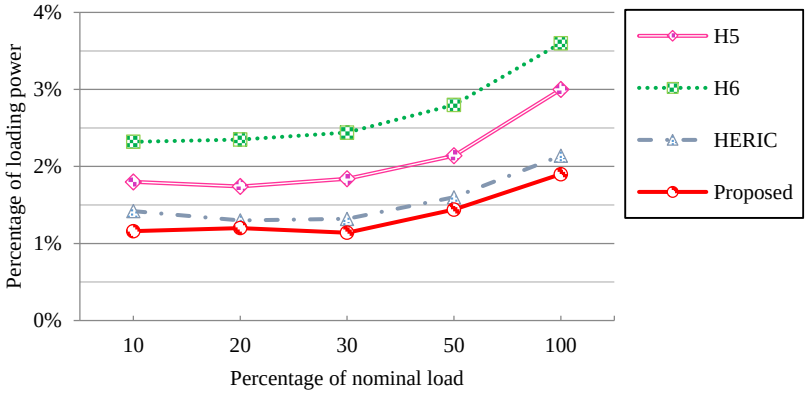


Figure 13. Total power loss through energy transmission.

It should be noted that with a rise in load power, the current ripple and the sizing of passive components are minimized due to the increment in current amplitude. Furthermore, the proposed topology has the ability to accomplish the power factor correction (PFC) operation mode as an active filter application.

$$\eta = \frac{P_{out}}{P_{out} + P_{loss}} \times 100 = \frac{44}{44 + 0.831} \times 100 = 98.02\% \quad (31)$$

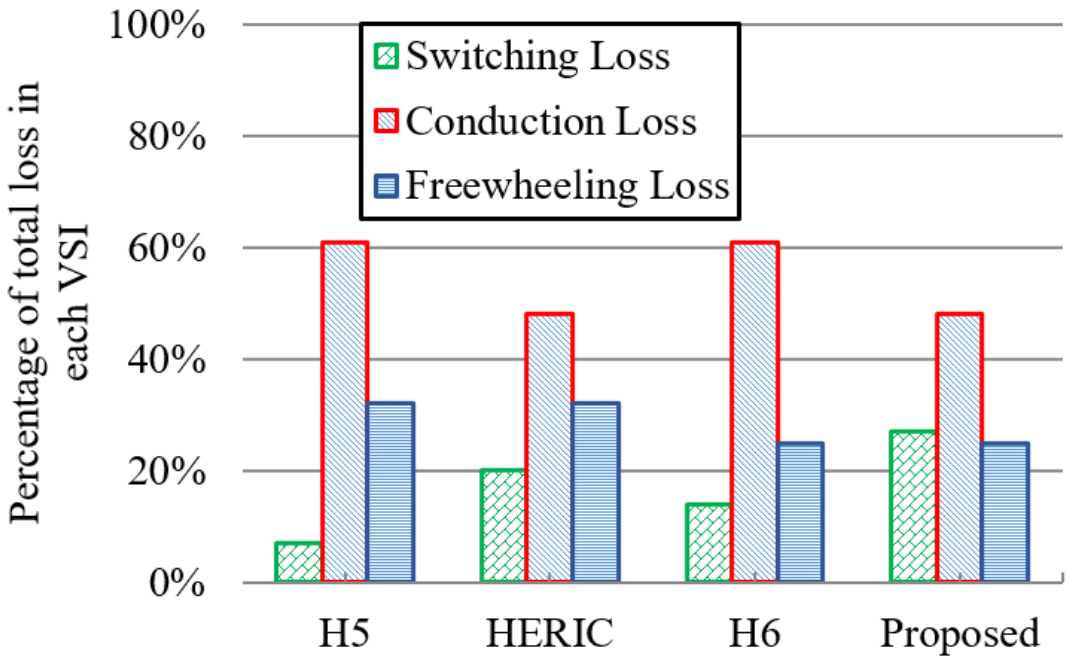


Figure 14. Percentage of self-VSI power loss sharing during operation. VSI: voltage source inverters.

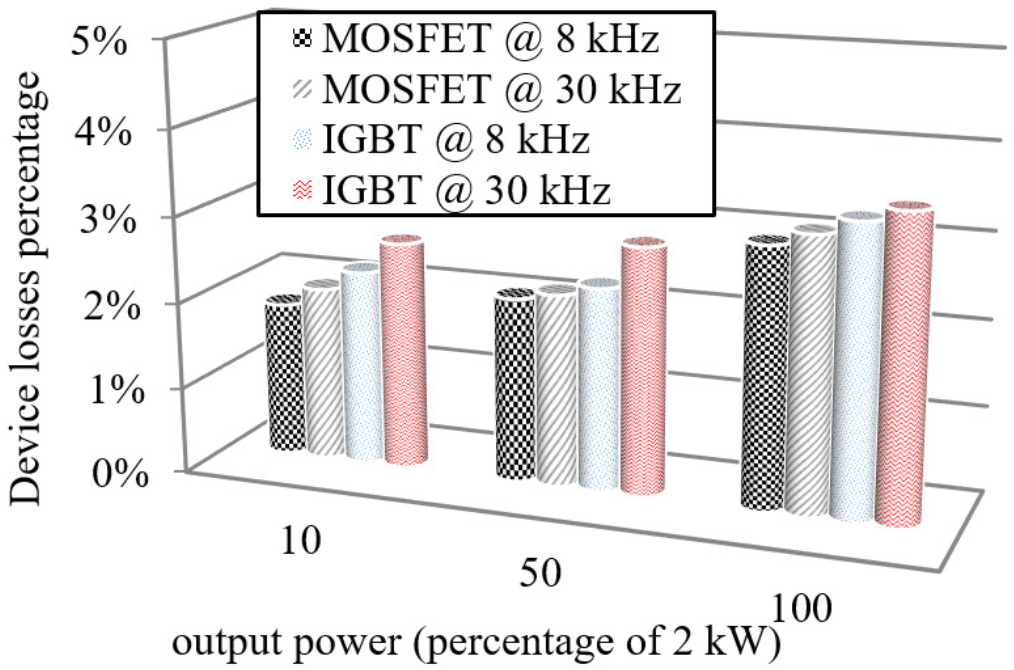


Figure 15. Percentage of device power loss in terms of output power.

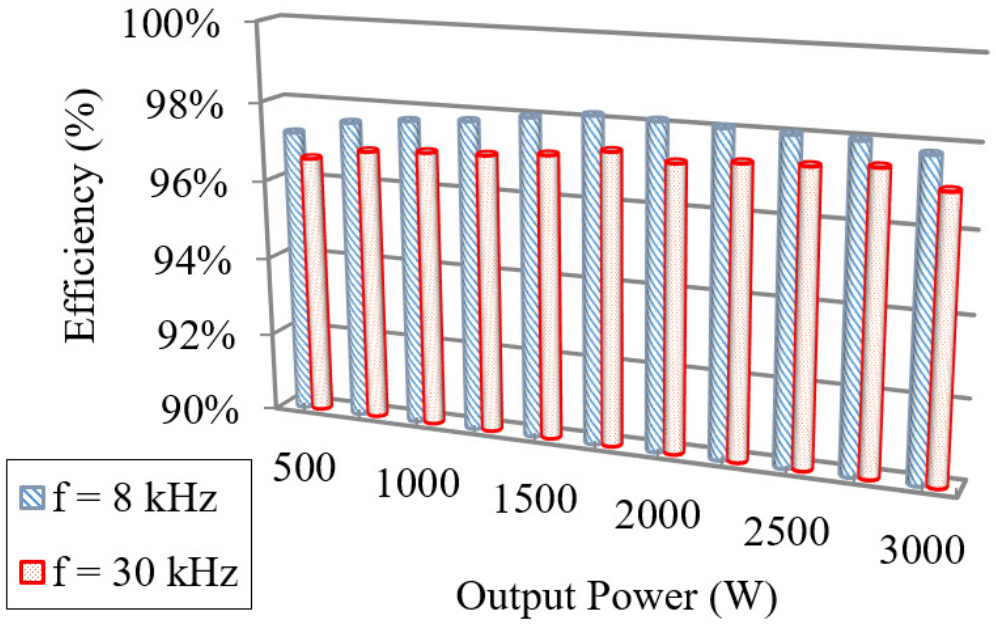


Figure 16. Efficiency analysis based on output power variations and frequency effects.

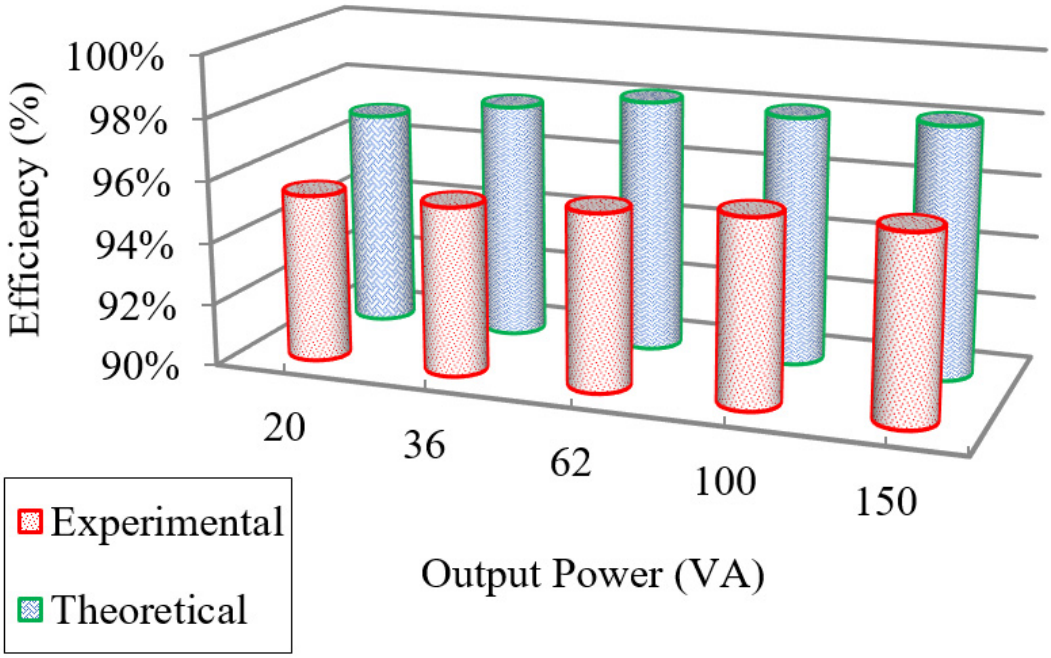


Figure 17. Experimental and theoretical efficiency analysis at 8 kHz switching frequency.

8. Reactive Power Compensation

To evaluate the active/reactive power control, an active load is connected to the system and then disconnected for a while in a time interval of 0.4 s to 1 s. At first, the system is loaded with a 50 W pure resistive load without any reactive portion. Then, at t = 0.4 s a 250 W load is paralleled to the previous load, which causes more current drawn from the DC side. While the transients resulting from connecting/disconnecting the load are inevitable, it is noticed some reactive power sharp spikes during the transient response. However, the spikes are rapidly eliminated by following the Q_{ref} reference signal as depicted in Figure 18.

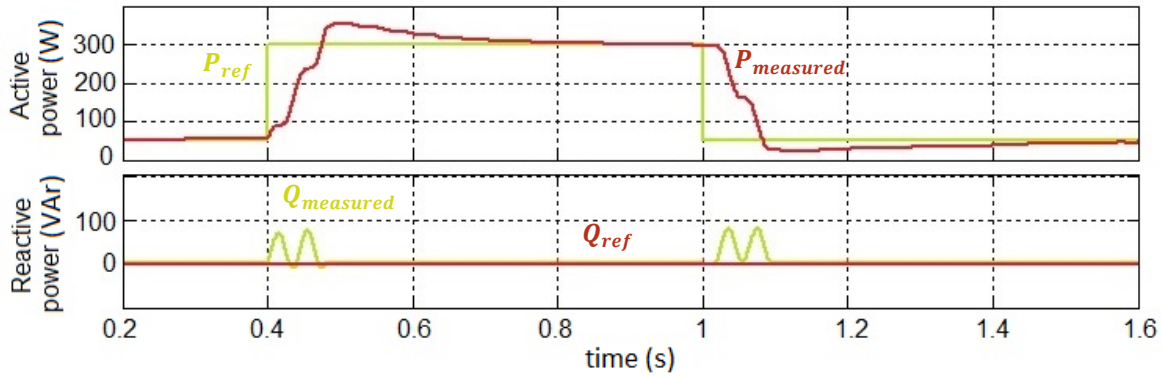


Figure 18. Active and reactive powers diagram.

9. Conclusions

This paper has presented a novel H7 architecture that was derived from the H6-type single-phase transformerless inverter to address the suppression of common mode current. In this topology, the number of components used on the current flow path is minimized, resulting in increased power conversion efficiency. In addition, the body diodes conduction in some not solicited time intervals is solved with appropriate placement of components. The prototype built for testing the concept was characterized at low power rating due to technical limitations in the laboratory infrastructure. The results in laboratory have shown high-efficiency conversion of 98.02% efficiency. Comparing to other common mode current mitigation structures, low CMC value was achieved below 40 mA without compromising high power quality output. A satisfactory THD measurement in relation to voltage output of 1.52% proves that is in line with other power conversion structures at disposable in single-phase grid connected inverters The proposed design is satisfied with low-size LC filter, allowing high power density with low weight. Due to elimination of the CMC, this paper recommends an appropriate switching pattern with a unipolar PWM modulation technique that decouples the i_{cm} flowing path. This results in the common mode voltage being constant.

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References

1. Manfredini, G.; Catania, A.; Benvenuti, L.; Cicalini, M.; Piotto, M.; Bruschi, P. Ultra-Low-Voltage Inverter-Based Amplifier with Novel Common-Mode Stabilization Loop. *Electronics* **2020**, *9*, 1019. [CrossRef]
2. Baik, J.; Yun, S.; Kim, D.; Kwon, C.; Yoo, J. Remote-State PWM with Minimum RMS Torque Ripple and Reduced Common-Mode Voltage for Three-Phase VSI-Fed BLAC Motor Drives. *Electronics* **2020**, *9*, 586. [CrossRef]
3. Jafrodi, S.T.; Ghanbari, M.; Mahmoudian, M.; Najafi, A.; Rodrigues, E.M.; Pouresmaeil, E. A Novel Control Strategy to Active Power Filter with Load Voltage Support Considering Current Harmonic Compensation. *Appl. Sci.* **2020**, *10*, 1664. [CrossRef]
4. Li, X.; Wang, N.; San, G.; Guo, X. Current source AC-Side clamped inverter for leakage current reduction in grid-connected PV system. *Electronics* **2019**, *8*, 1296. [CrossRef]
5. IEC Standard. *Photovoltaic (PV) Systems-Characteristics of the Utility Interface*; IEC: Geneva, Switzerland, 2004; IEC 61727.
6. VDE Standard. *Power Generation Systems Connected to the Low-Voltage Distribution Network*; VDE: Berlin, Germany, 2011; VDE-AR-N 4105.

7. Li, W.; Gu, Y.; Luo, H.; Cui, W.; He, X.; Xia, C. Topology review and derivation methodology of single-phase transformerless photovoltaic inverters for leakage current suppression. *IEEE Trans. Ind. Electron.* **2015**, *62*, 4537–4551. [CrossRef]
8. Dietrich, K. Wechselrichter. DE Patent DE19642522 (C1), 23 April 1998.
9. Xiao, H.; Xie, S. Transformerless split-inductor neutral point clamped three-level PV grid-connected inverter. *IEEE Trans. Power Electron.* **2011**, *27*, 1799–1808. [CrossRef]
10. Araújo, S.V.; Zacharias, P.; Mallwitz, R. Highly efficient single-phase transformerless inverters for grid-connected photovoltaic systems. *IEEE Trans. Ind. Electron.* **2009**, *57*, 3118–3128. [CrossRef]
11. González, R.; Gubía, E.; López, J.; Marroyo, L. Transformerless single-phase multilevel-based photovoltaic inverter. *IEEE Trans. Ind. Electron.* **2008**, *55*, 2694–2702. [CrossRef]
12. Luo, H.; Dong, Y.; Li, W.; He, X. Module Multilevel-Clamped Composited Multilevel Converter (M-MC^2) with Dual T-Type Modules and One Diode Module. *J. Power Electron.* **2014**, *14*, 1189–1196. [CrossRef]
13. Yu, W.; Lai, J.S.J.; Qian, H.; Hutchens, C. High-efficiency MOSFET inverter with H6-type configuration for photovoltaic non-isolated AC-module applications. *IEEE Trans. Power Electron.* **2010**, *26*, 1253–1260. [CrossRef]
14. Ji, B.; Wang, J.; Zhao, J. High-efficiency single-phase transformerless PV H6 inverter with hybrid modulation method. *IEEE Trans. Ind. Electron.* **2012**, *60*, 2104–2115. [CrossRef]
15. Victor, M.; Greizer, F.; Bremicker, S.; Hübler, U. SMA Solar Technology AG, Method of Converting a Direct Current Voltage from a Source of Direct Current Voltage, More Specifically from a Photovoltaic Source of Direct Current Voltage, into an Alternating Current Voltage. U.S. Patent 7411.802, 12 August 2008.
16. Yu, W.; Lai, J.S.; Qian, H.; Hutchens, C.; Zhang, J.; Lisi, G.; Djabbari, A.; Smith, G.; Hegarty, T. February. High-efficiency inverter with H6-type configuration for photovoltaic non-isolated ac module applications. In Proceedings of the 2010 Twenty-Fifth Annual IEEE Applied Power Electronics Conference and Exposition (APEC), Palm Springs, CA, USA, 21–25 February 2010; pp. 1056–1061.
17. Abdelhakim, A.; Mattavelli, P.; Yang, D.; Blaabjerg, F. Coupled-inductor-based DC current measurement technique for transformerless grid-tied inverters. *IEEE Trans. Power Electron.* **2017**, *33*, 18–23. [CrossRef]
18. Liu, H.; Ran, Y.; Liu, K.; Wang, W.; Xu, D. A modified single-phase transformerless Y-source PV grid-connected inverter. *IEEE Access* **2018**, *6*, 18561–18569. [CrossRef]
19. Melkebeek, J.A. *Power Electronic Components*, 1st ed.; Springer: Berlin/Heidelberg, Germany, 2018; pp. 211–232.
20. Litrán, S.P.; Durán, E.; Semião, J.; Barroso, R.S. Single-Switch Bipolar Output DC-DC Converter for Photovoltaic Application. *Electronics* **2020**, *9*, 1171. [CrossRef]
21. Quach, T.-H.; Do, D.-T.; Nguyen, M.-K. A PWM Scheme for Five-Level H-Bridge T-Type Inverter with Switching Loss Reduction. *Electronics* **2019**, *8*, 702. [CrossRef]
22. Chung, H.S.H.; Wang, H.; Blaabjerg, F.; Pecht, M. *Reliability of Power Electronic Converter Systems*, 1st ed.; IET Press: London, UK, 2015; pp. 8885–8993.
23. Erickson, R.W.; Maksimovic, D. *Fundamentals of Power Electronics*, 1st ed.; Springer: Berlin/Heidelberg, Germany, 2007.
24. Xiao, H.; Xie, S.; Chen, Y.; Huang, R. An optimized transformerless photovoltaic grid-connected inverter. *IEEE Trans. Ind. Electron.* **2010**, *58*, 1887–1895. [CrossRef]
25. Zhang, L.; Sun, K.; Xing, Y.; Xing, M. H6 transformerless full-bridge PV grid-tied inverters. *IEEE Trans. Power Electron.* **2013**, *29*, 1229–1238. [CrossRef]
26. Cui, W.; Yang, B.; Zhao, Y.; Li, W.; He, X. A novel single-phase transformerless grid-connected inverter. In Proceedings of the IECON 2011-37th Annual Conference of the IEEE Industrial Electronics Society, Melbourne, Australia, 7–10 November 2011; pp. 1126–1130.
27. Kerekes, T.; Teodorescu, R.; Rodríguez, P.; Vázquez, G.; Aldabas, E. A new high-efficiency single-phase transformerless PV inverter topology. *IEEE Trans. Ind. Electron.* **2009**, *58*, 184–191. [CrossRef]
28. Yang, B.; Li, W.; Gu, Y.; Cui, W.; He, X. Improved transformerless inverter with common-mode leakage current elimination for a photovoltaic grid-connected power system. *IEEE Trans. Power Electron.* **2011**, *27*, 752–762. [CrossRef]