

Article

RST Digital Robust Control for DC/DC Buck Converter Feeding Constant Power Load

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Abstract: The instability of DC microgrids is the most prominent problem that limits the expansion of their use, and one of the most important causes of instability is constant power load CPLs. In this paper, a robust RST digital feedback controller is proposed to overcome the instability issues caused by the negative-resistance effect of CPLs and to improve robustness against the perturbations of power load and input voltage fluctuations, as well as to achieve a good tracking performance. To develop the proposed controller, it is necessary to first identify the dynamic model of the DC/DC buck converter with CPL. Second, based on the pole placement and sensitivity function shaping technique, a controller is designed and applied to the buck converter system. Then, validation of the proposed controller using Matlab/Simulink was achieved. Finally, the experimental validation of the RST controller was performed on a DC/DC buck converter with CPL using a real-time Hardware-in-the-loop (HIL). The OPAL-RT OP4510 RCP/HIL and dSPACE DS1104 controller board are used to model the DC/DC buck converter and to implement the suggested RST controller, respectively. The simulation and HIL experimental results indicate that the suggested RST controller has high efficiency.



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Keywords: DC microgrids; robust RST digital controller; DC/DC buck converter; constant power load (CPL); hardware-in-the-loop (HIL)

MSC: 93D09; 93D15; 93C10

1. Introduction

Microgrids are increasingly being used as a result of environmental concerns such as CO₂ emissions and global climate change [1]. A microgrid is a small power grid that connects various sources and loads. A microgrid is composed of several components, including renewable energy sources such as solar, wind, and fuel cells, as well as energy storage technologies such as super capacitors, batteries, and power electronic converters [2]. The architecture of the microgrid can be classified into three types: AC, DC, and hybrid microgrid. DC microgrids are preferred over AC microgrids due to higher reliability, no reactive power losses, no harmonics, no requirement for synchronization, no frequency challenges, good compatibility, high efficiency, and direct connection of DC loads [3,4]. In DC microgrids, the DC/DC converters is critical for connecting distributed renewable sources and energy storage systems (ESSs) to loads [5]. The typical construction of a DC microgrid is depicted in Figure 1. Despite the advantages of DC microgrids, stability is a critical problem that might bring the entire system down. The main cause of stability issue in DC microgrids is the constant power loads (CPLs). The CPL is a nonlinear load with an incremental negative impedance (INI) characteristic, which implies the load current decrease/increase with the increase/decrease in its terminal voltage. Various CPLs, such as electric motors, actuators, and power electronic converters, should be regulated to maintain a constant output power [6]. A CPL has the ability to reduce system damping and make DC microgrids unstable [7,8].

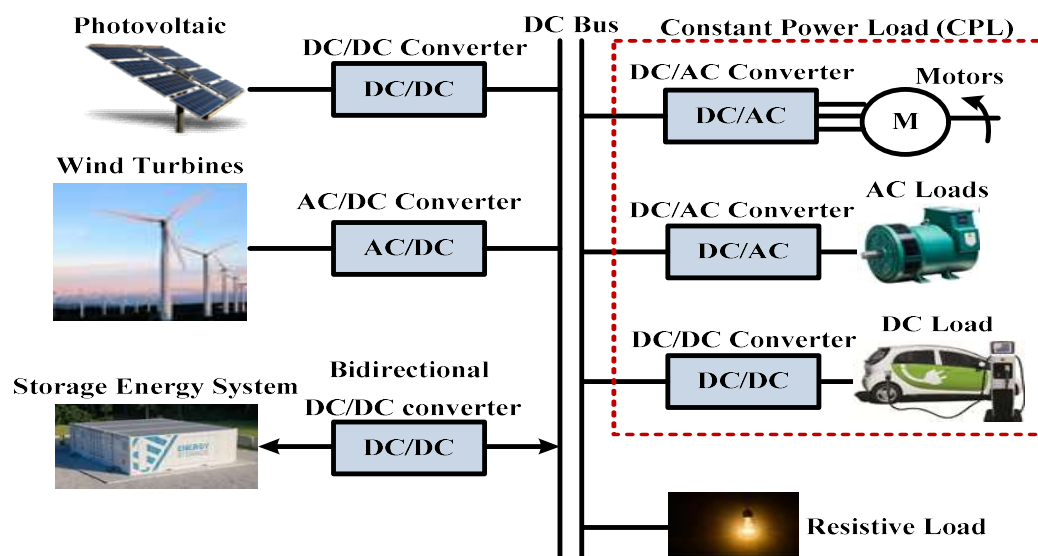


Figure 1. The structure of a DC microgrid with various loads and sources.

Numerous control strategies have been suggested for addressing the instability problem in DC microgrids with CPLs. In [8–10], the authors proposed passive-damping methods to increase the damping factor by adding passive components such as resistors, capacitors, or inductors, to the DC/DC converter. However, this approach diminishes system efficiency by producing excessive power losses. The authors in [11–13] developed active-damping approaches by modifying control loops with virtual impedance to allow the system poles to lie on the left side without changing the system hardware. This approach is effective in ensuring system stability when CPL is prevalent. However, the original control loop of the converter will be changed, affecting the dynamic responsiveness of the entire system. For both passive and active damping approaches, small-signal analysis is being used in the design and analysis process. When a broad range of operating conditions and disturbances are present, poor performance is inevitable [14]. Due to the non-linear nature of the DC/DC converters, several nonlinear controllers that are suggested to ensure the stability of DC microgrids in the presence of CPL have been implemented [15]. The authors of [16,17] presented model predictive control (MPC) to stabilize DC microgrids with CPLs. In [18], a nonlinear fuzzy MPC with effective control performance for nonlinear systems is formed by combining a Takagi-Sugeno (TS) fuzzy model with a linear model predictive controller (MPC). However, the computational burden of such controllers, which involve maximizing a predefined cost function, restricts their widespread application in real time. The authors in [19–23] proposed a robust based PWM slide mode controller (SMC) to stabilize a DC/DC boost converter system feeding CPLs, where the duty cycle of the boost converter is estimated using a nonlinear polynomial sliding surface. However, SMC has the disadvantage of driving the power converter at a variable switching frequency, which degrades power quality. In [24], a fixed frequency SMC with a novel double integral type sliding manifold is presented for voltage regulation of a DC microgrid. In [25], an adaptive backstepping controller is designed for a DC microgrid feeding non-ideal CPLs through a third-degree cubature kalman filter. The proposed controller is designed for large signal stabilization through the recursive lyapunov design procedure. The authors of [26] addressed the voltage regulation issue of the DC/DC converter with CPL by integrating a composite nonlinear controller with a backstepping approach and a disturbance observer. The most recent nonlinear control techniques for stabilizing DC microgrids and resolving the tracking problem are passivity-based controllers (PBCs) [27]. Two primary categories of PBC have been identified in the literature [28]. The traditional PBC selects the energy function to be assigned and then builds a controller to minimize the energy function. In the second category of PBC, an explicitly defined control structure, such as Euler-Lagrange (EL) or Port-Controlled Hamiltonian (PCH), should be chosen first, and then all assignable

energy and power functions should be characterized. In [29,30], an adaptive energy shaping algorithm combining standard PBC and immersion and invariance (I&I) parameter estimator was utilized to handle the difficult challenge of regulating the output voltage of a DC/DC buck-boost converters feeding an unknown power CPL. The I&I estimator is utilized to compute online the extracted load power, which is complicated to measure in practical applications. In [31], a standard PBC is presented to reshape the system energy and compensate for the negative impedance and a proportion-integration (PI) action is added around the passive output to boost disturbance rejection performance. In [32], an H-infinity robust controller based on the Glover Doyle optimization algorithm (GDOA) to prevent system instability due to the CPLs is proposed. However, in some cases, GDOA provides a robust controller with a higher order of the denominator, which may be challenging to implement.

To the best of our knowledge, no study has employed the RST digital robust controller to overcome instability problems in DC microgrid caused by CPL. As a result, this paper presents a new robust controller for stabilizing DC/DC buck converter fed a DC microgrid with CPLs. The main contributions to this article are the following:

1. An RST controller is proposed to stabilize the DC/DC buck converter with CPL;
2. All perturbations caused by changes in input voltage and current fluctuations are rejected, resulting in very good tracking;
3. Use hardware-in-the-loop (HIL) to model the DC/DC buck converter with CPL using OPAL-RT OP4510 RCP/HIL and to implement the proposed RST controller in dSPACE 1104.

The remainder of this paper is organized as follows: in Section 2, the modeling of a buck converter with CPL is presented. The RST robust controller is designed in Section 3. In Sections 4 and 5, the simulation and real-time HIL results are presented, respectively. Finally, the conclusion and some future work prospects are presented in Section 5.

2. Modeling of the DC/DC Buck Converter with CPL

The typical circuit for a DC/DC buck converter with a CPL is depicted in Figure 2, where the CPLs (such as cascaded DC/AC or DC/DC converter) can be modelled as controlled current source [33].

$$I_{CPL} = \frac{P_{CPL}}{V_{out}} \quad (1)$$

where I_{CPL} is current of CPL, P_{CPL} is power, and V_{out} is the output voltage of DC/DC buck converter. The state-space model of the converter with CPL is obtained by considering the continuous conduction mode (CCM) and by using Kirchhoff's current and voltage laws, as follows [34]:

$$d \frac{V_{in}}{L} - \frac{V_{out}}{L} = \frac{di_L}{dt} \quad (2)$$

$$\frac{i_L}{C} - \frac{V_{out}}{R_L C} - \frac{P_{CPL}}{V_{out} C} = \frac{dV_{out}}{dt} \quad (3)$$

where V_{in} , V_{out} , i_L , and $d \in [0, 1]$ are the input voltage, output voltage, inductor current, and duty ratio, respectively.

The design of the output LC filter for the DC/DC buck converter is designed on the basis of the following conditions: continuous-current conduction operation of the converter, ripple on the output voltage that does not exceed a few percent [35].

$$L \geq \frac{V_o(1-d)}{f \Delta i_L} \quad (4)$$

$$C \geq \frac{1-d}{8L \frac{\Delta V_o}{V_o} f^2} \quad (5)$$

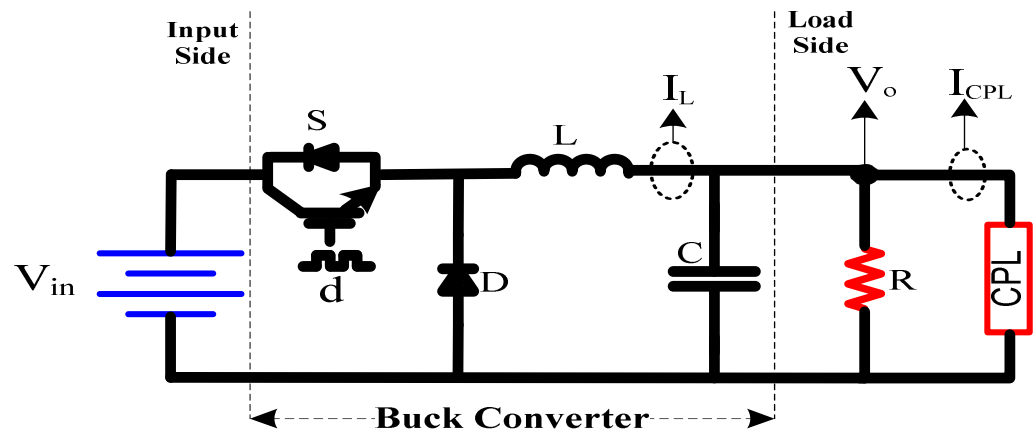


Figure 2. The typical circuit for a DC/DC buck converter with CPL.

By using average switch modeling, the transfer function of duty cycle to the output voltage of the buck converter in S domain is given as:

$$G(s) = \frac{V_{out}}{d} \quad (6)$$

$$G(s) = \frac{\frac{V_{in}}{L^2 C}}{s^2 + \left(\frac{1}{RC} - \frac{P_{CPL}}{V_{out}^2 C} \right) s + \frac{1}{LC}} \quad (7)$$

where d is the duty ratio and V_{out} is the output voltage.

Assuming that the system parameters are $C = 220 \mu\text{F}$, $L = 2.7 \text{ mH}$, $R_{CPL} = -9.6 \Omega$, $P = 20.4 \text{ W}$, $V_{out} = 14 \text{ V}$, $V_{in} = 28 \text{ V}$, $R = 470 \Omega$, and by substituting these values into the transfer function of the system given in (7), the result is as shown in (8).

$$G(s) = \frac{4.714 \times 10^7}{s^2 - 463.8 s + 1.684 \times 10^6} \quad (8)$$

The characteristic equation obtained from (7) demonstrates that the increment negative impedance (INI) of the CPL pushes poles to the right-half plane (RHP) and makes the system unstable, as indicated in (8). To improve the stability of the system and robustness to disturbances when changes occur in CPL, as well as to achieve good reference tracking performance, an RST digital robust controller is presented in the next section.

3. RST Robust Digital Controller Design

3.1. System Identification Workflow

Figure 3 illustrates the principle of discrete-time model identification. Using MATLAB identification toolbox, a discrete-time model with adjustable parameters is implemented. A parameter-adaptation technique uses the prediction error, the difference between the system output at time t , $y(t)$, and the output predicted by the model, $\hat{y}(t)$, to adjust the model parameters at each sampling time in order to reduce this error. The system is excited via the discrete sequence $u(t)$ $t = 0, 1, 2, \dots, n$. This discrete signal is made continuous by the Zero Order Hold (ZOH). After obtaining the model, statistical tests on the prediction error $e(t)$ and the predicted output y_L could be used to do objective validation (t). The validation test allows the optimum algorithm for parameter estimate to be determined.

The sampling frequency is set based on the bandwidth of the continuous-time plant and, more specifically, the bandwidth required for the closed loop. The general rule is:

$$f_s = (6 \text{ to } 25) f_B^{Cl} \quad (9)$$

where f_s is the sampling frequency and f_B^{Cl} is the desired bandwidth of the closed loop.

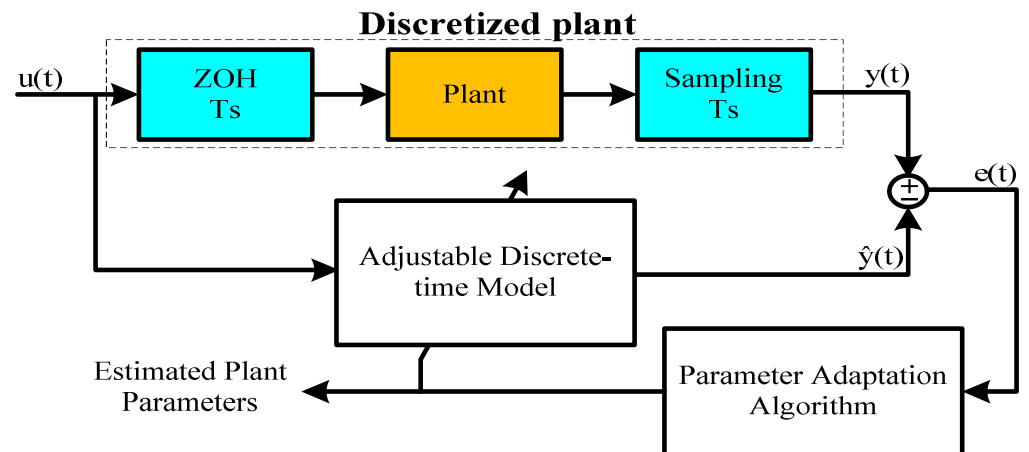


Figure 3. Parameter estimation of discrete-time models.

3.2. The R-S-T Digital Controller

To design the RST controller, a region of uncertainties must be defined based on the interval parameter variation of the plant model. To choose the RST polynomials that better fit the control system requirements can be a very difficult numerical problem, especially in auto- and self-tuning control systems. Due to these limitations, general RST controller design for industrial applications remains challenging [36]. In this section, the RST robust digital feedback controller is designed by integrating pole placement with sensitivity function shaping [37]. This design methodology is utilized here to improve the performance of the closed-loop system and disturbance rejection at the same time. The RST controller architecture is depicted in Figure 4.

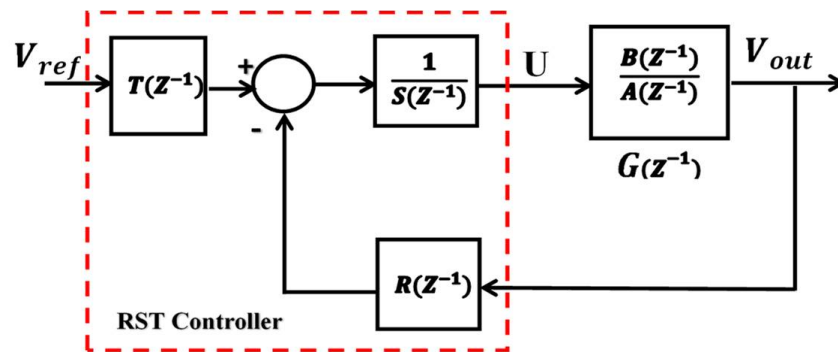


Figure 4. Block diagram of RST robust digital feedback controller with plant.

In Figure 4, the parameters R , S , and T represent polynomials of the controller and G represents the dynamic model of the buck converter. The discrete time plant model (G), which is utilized in the design of digital controllers, is obtained by the discretization of the model in (8) using the ZOH transformation as depicted in Figure 3. The discrete time plant model is rewritten in this case as shown in (10).

$$G(z^{-1}) = \frac{B(z^{-1})}{A(z^{-1})} = \frac{0.239 + 0.2428z^{-1}}{1 - 2.03z^{-1} + 1.047z^{-2}} \quad (10)$$

The R and S digital polynomials are designed to achieve the desired regulation performance, and the T is designed to provide the required tracking performance. The three polynomials of the proposed RST digital controller are as follows:

$$R(z^{-1}) = r_0 + r_1 z^{-1} + r_2 z^{-2} + \dots + r_{nR} z^{-nR} \quad (11)$$

$$S(z^{-1}) = s_0 + s_1 z^{-1} + s_2 z^{-2} + \dots + s_{ns} z^{-ns} \quad (12)$$

$$T(z^{-1}) = t_0 + t_1 z^{-1} + t_2 z^{-2} + \dots + t_{nt} z^{-nt} \quad (13)$$

However, $T(z^{-1})$ will be set equal to $R(1)$, implying that the gain of the $T(z^{-1})$ will equal to the sum of $R(z^{-1})$ coefficients in order to maintain a unit gain between the desired and actual outputs in steady state.

The desired performance of the DC/DC buck converter system is to achieve precise reference tracking while maintaining robustness and stability. These desired performances can be achieved using constraints on the shape of closed-loop sensitivity functions [38,39]. The output sensitivity function (S_0) between the load variation disturbance and plant output is given by:

$$S_0(z^{-1}) = \frac{A(z^{-1})S(z^{-1})}{A(z^{-1})S(z^{-1}) + B(z^{-1})R(z^{-1})} \quad (14)$$

The complementary sensitivity function (T_0) between the disturbance measurement noise and plant output is given by:

$$T_0(z^{-1}) = \frac{B(z^{-1})T(z^{-1})}{A(z^{-1})S(z^{-1}) + B(z^{-1})R(z^{-1})} \quad (15)$$

The input sensitivity function (S_i) between the disturbance of control signal and plant input is given by:

$$S_i(z^{-1}) = \frac{A(z^{-1})R(z^{-1})}{A(z^{-1})S(z^{-1}) + B(z^{-1})R(z^{-1})} \quad (16)$$

Table 1 summarizes the limits on the shapes of closed-loop sensitivity functions that have been addressed [37,39].

Table 1. Constraints on sensitivity function shapes.

Constraints	Conditions	Condition Description	Purpose
Constraint 1	$\ S_0(z^{-1})\ _{\infty} < 6 \text{ dB}, \forall \omega$	The maximum output sensitivity function should be less than 6 dB.	For ensure adequate stability margins and robustness margins.
Constraint 2	$\ T_0(z^{-1})\ _{\infty} < 3.5 \text{ dB}, \forall \omega$	The maximum of the complementary sensitivity function should be less than 3.5 dB.	For ensure adequate stability margins, as this will also maintain a good robustness margin.
Constraint 3	$\ S_i(z^{-1})\ _{\infty} \leq 0 \text{ dB}, \forall \omega$	The maximum of input sensitivity function should be equal or less than 0 dB.	To ensure the output of controller between zero and one.

The closed-loop sensitivity function is shaped by selecting desired closed loop poles and introducing pre-specified polynomials into the controller. From the expressions of sensitivity functions, it can be noted that the 3 sensitivity functions have the same denominator $P(z^{-1}) = A(z^{-1})S(z^{-1}) + B(z^{-1})R(z^{-1})$ which determines the closed-loop poles and can be distinguished to the dominant and auxiliary closed-loop poles as given in (17).

$$P(z^{-1}) = P_A(z^{-1})P_D(z^{-1}) \quad (17)$$

where $P_A(z^{-1})$ denotes the auxiliary poles and $P_D(z^{-1})$ denotes the desired dominant poles of the closed loop system. The pre-specified polynomials of the $R(z^{-1})$ and $S(z^{-1})$ are introduced as shown in (18) and (19):

$$R(z^{-1}) = H_R(z^{-1})R'(z^{-1}) \quad (18)$$

$$S(z^{-1}) = H_S(z^{-1})S'(z^{-1}) \quad (19)$$

where $H_R(z^{-1})$ and $H_S(z^{-1})$ are polynomials that have been pre-specified. The anonymous polynomials of the controller $R'(z^{-1})$ and $S'(z^{-1})$ produced by solving the following equations:

$$P(z^{-1}) = A(z^{-1})S(z^{-1}) + B(z^{-1})R(z^{-1}) \quad (20)$$

$$P_D(z^{-1}) \cdot P_A(z^{-1}) = A(z^{-1})H_S(z^{-1})S'(z^{-1}) + B(z^{-1})H_S(z^{-1})R'(z^{-1}) \quad (21)$$

Figure 5 displays the required steps that must be performed in order to build the RST controller [36].

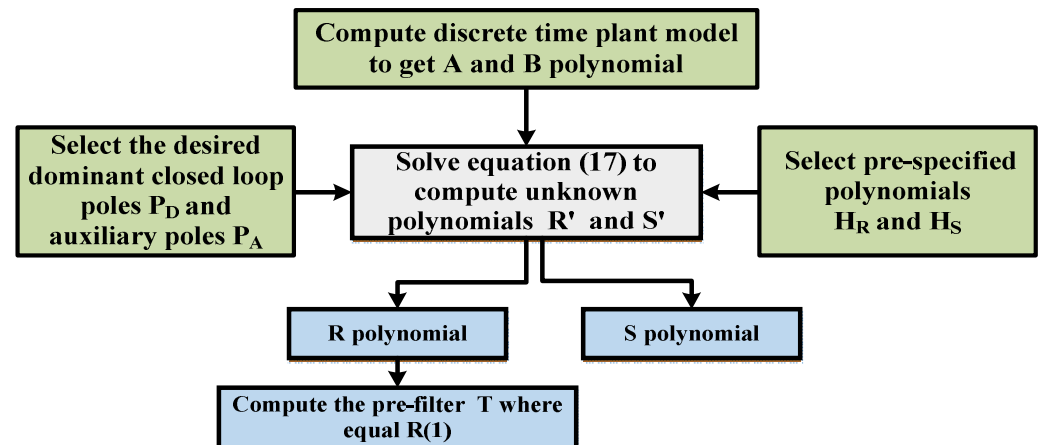


Figure 5. Block diagram of the controller design steps.

The polynomials for the RST controller derived by solving (20) are as follows:

$$R(z^{-1}) = 0.2923 - 0.3061z^{-1} - 0.2624z^{-2} + 0.3076z^{-3} - 0.0284z^{-4} \quad (22)$$

$$S(z^{-1}) = 1 - 1.1640z^{-1} - 0.2094z^{-2} - 0.0520z^{-3} + 0.0066z^{-4} \quad (23)$$

$$T(z^{-1}) = 0.003 \quad (24)$$

Figure 6 demonstrates all of the considered sensitivity functions with the RST digital controller. It can be observed that the recommended RST digital controller completely fits all three of the aforementioned restrictions in Table 1.

4. Simulation Results and Discussion

In this section, the simulation study was carried out to validate the efficacy of the suggested controller for DC/DC buck converter with CPL using the Matlab/Simulink (2016). The CPL is modeled as a current-controlled source, and the parameters of the system have been described and mentioned in Section 2. The switching frequency is set at 20 kHz. The simulation results in Figure 7 demonstrate how CPL affects the DC/DC buck converter, causing the system to become unstable in open loop. To mitigate this issue, the system is equipped with an RST digital robust controller. The output voltage in Figure 8 demonstrates the ability of the proposed controller to maintain system stability and keep the output voltage within the desired reference range. As shown in Figure 9, the tracking error between the desired reference and the output voltage of the buck converter is very small and negligible.

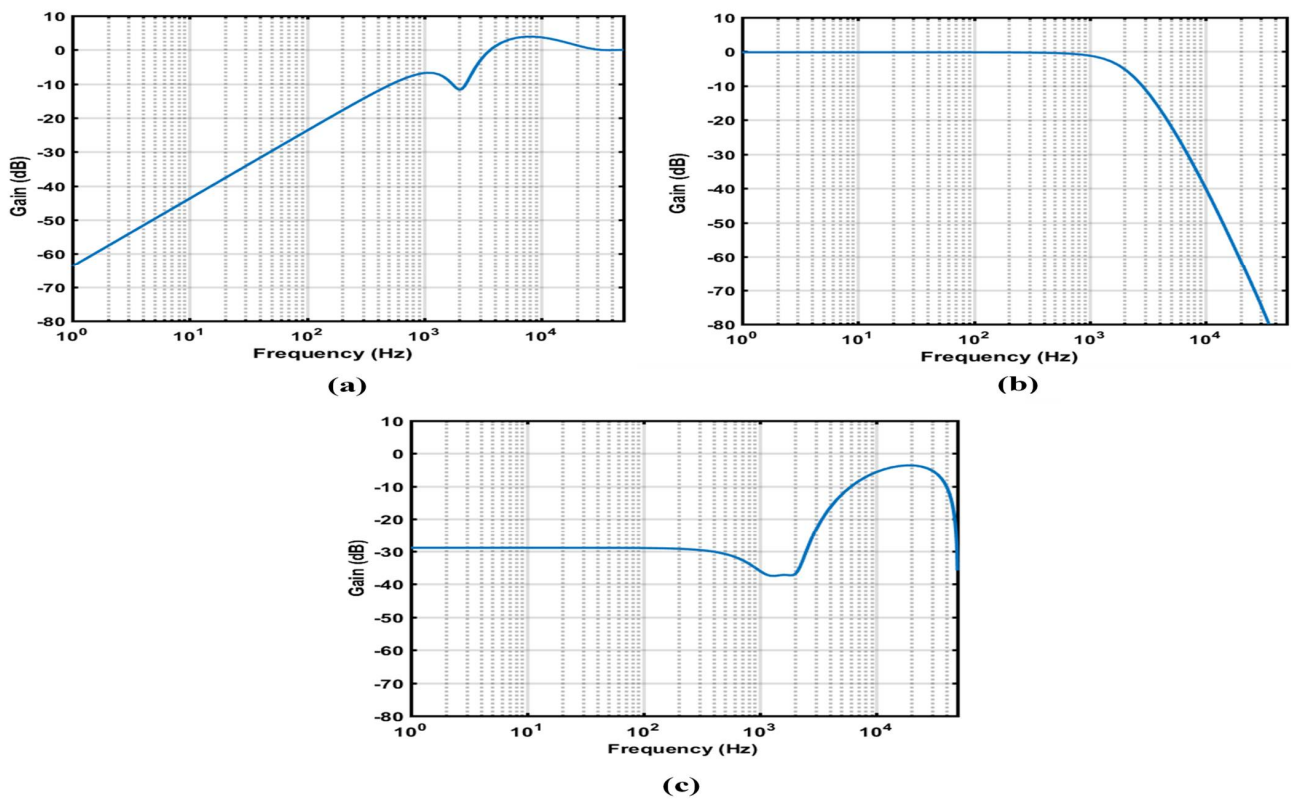


Figure 6. (a) Output sensitivity (S_0), (b) Complementary sensitivity (T_0), (c) Input sensitivity (S_i).

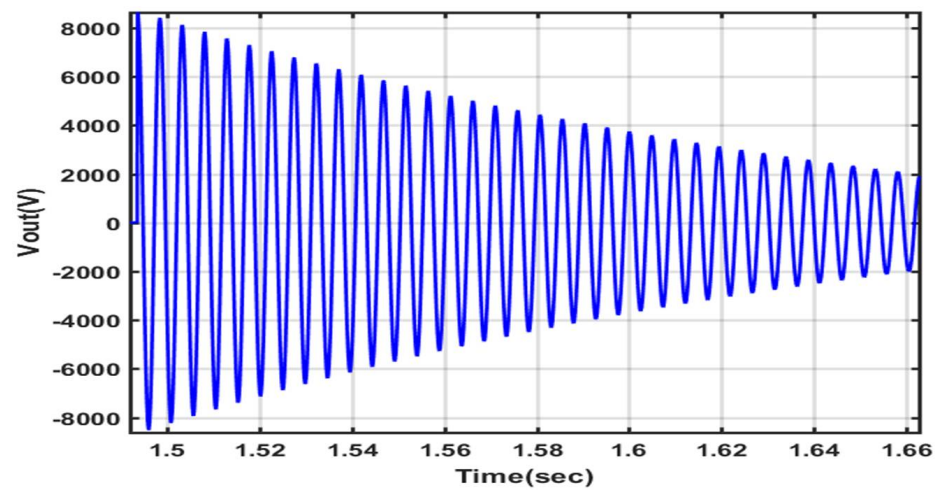


Figure 7. Dynamic response of the buck converter with CPL in an open loop mode.

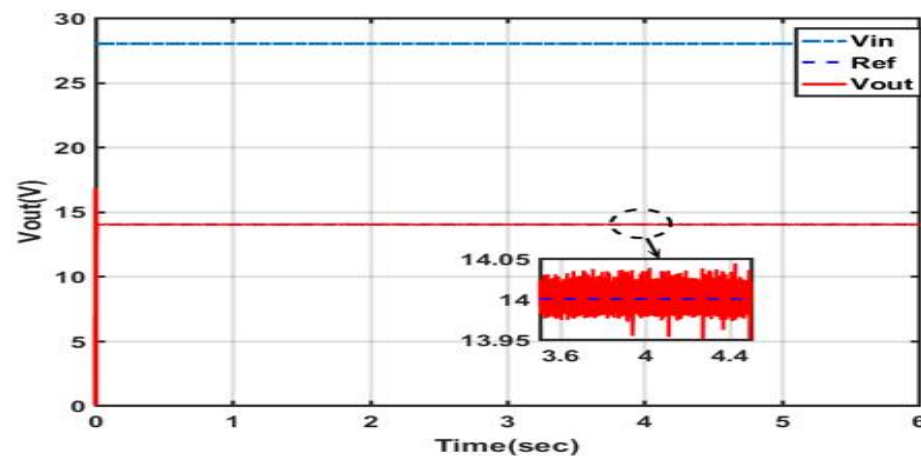


Figure 8. Dynamic response of the buck converter with CPL closed loop mode using RST controller.

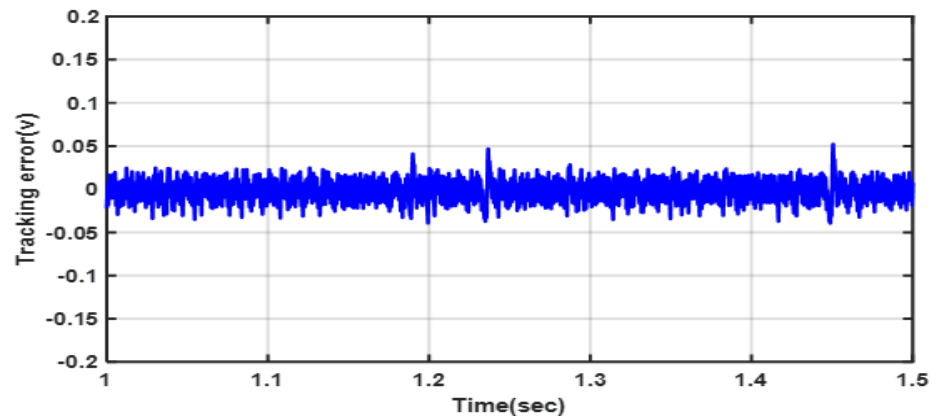


Figure 9. Tracking error between reference voltage and measured voltage.

The effectiveness and robustness of the proposed controller is depicted in Figure 10, where the desired voltage of the system is set at 14 V and the output voltage of the system remains stable despite changes in power consumed. The sudden change in power CPL causes a tiny transient variation in the output voltage, but after that, the output voltage is able to track the reference voltage with reasonable accuracy. Furthermore, the control signal (duty cycle) remains constant at 0.5 with a small fluctuation, but it is still within the range of 0 and 1. Figure 11 shows the effectiveness and robustness of the proposed controller in reducing the effects of a change in the source voltage on the output voltage where the influence is negligible.

5. HIL Experimental Results and Discussion

This section describes the HIL experimental testbed that is used to validate the MATLAB simulation findings achieved before. The OPAL-RT real-time simulator is used to connect the MATLAB Simulink model to the digital signal processor (DSP). The experimental setup and the block diagram are shown in Figures 12 and 13, respectively. This platform is consisting of OP4510 simulator, dSPACE DS1104 controller box, RT-LAB monitor console, dSPACE control desk monitor, and digital oscilloscope. In the HIL design of experiments, two cases are examined to validate the effectiveness of the proposed RST controller: one with a change in CPL and the other with a change in input voltage.

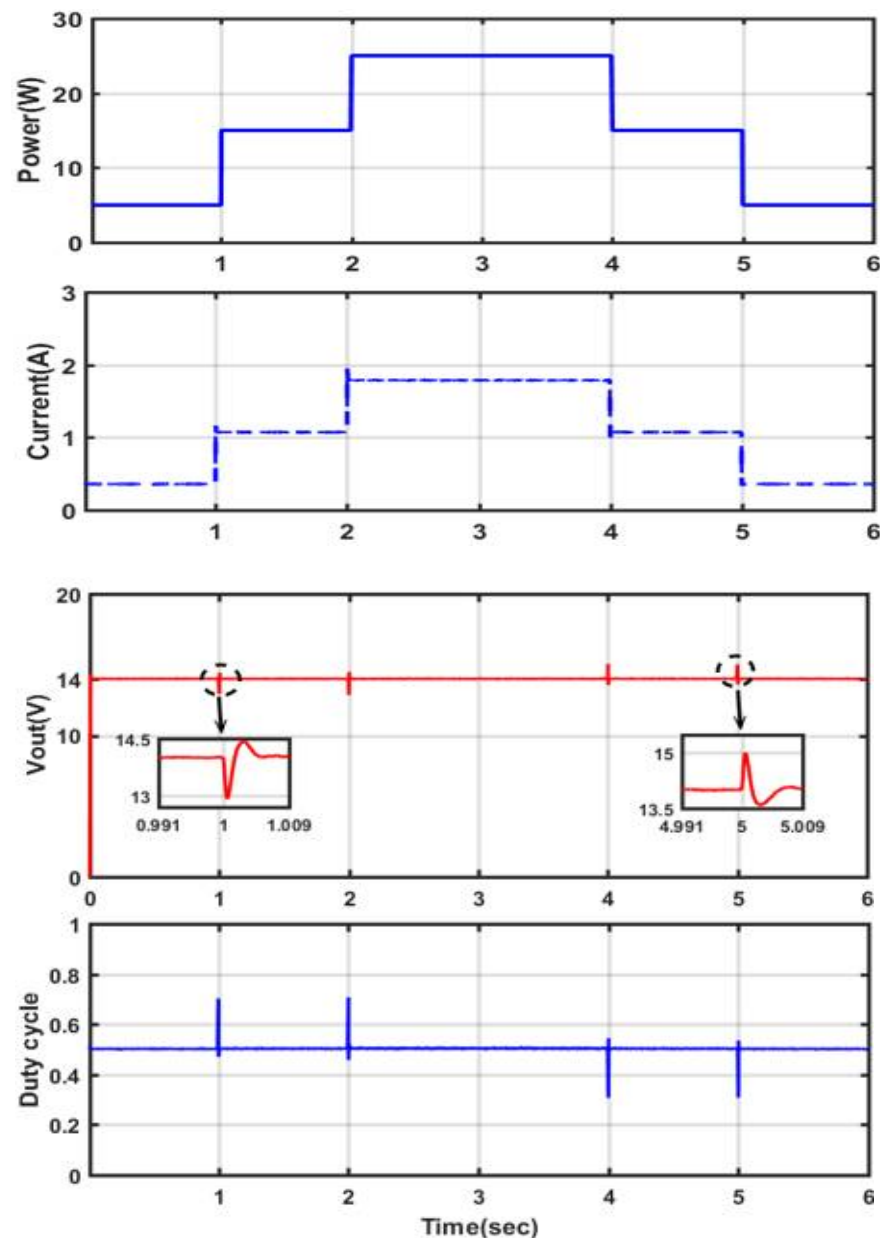


Figure 10. Changes in output voltage and duty cycle with an RST controller in response to CPL variation.

In this testbed, the RST controller is performed in the dSPACE DS1104 R&D controller board, while the DC/DC Buck converter with a CPL under MATLAB/Simulink operates in the OPAL-RT in real-time. The system output signal is sent from the analog port of the OPAL-RT to the ADC module of dSPACE DS1104. In order to keep the system running in the next cycle, the PWM signal is computed by the RST controller and supplied to the OPAL-RT through the digital input port. The analogue signals used in the experiments are scaled down since the output and input ranges of both the dSPACE and the OPAL-RT are constrained to -10 V to $+10$ V, and -16 V to $+16$ V, respectively. To achieve this limitation, the output and input voltages are divided by 4 V, and the CPL by 2 W. Meanwhile, due to the computational power of the OPAL-RT, the switching frequency is set to 20 kHz and the step size is set to 10^{-5} s.

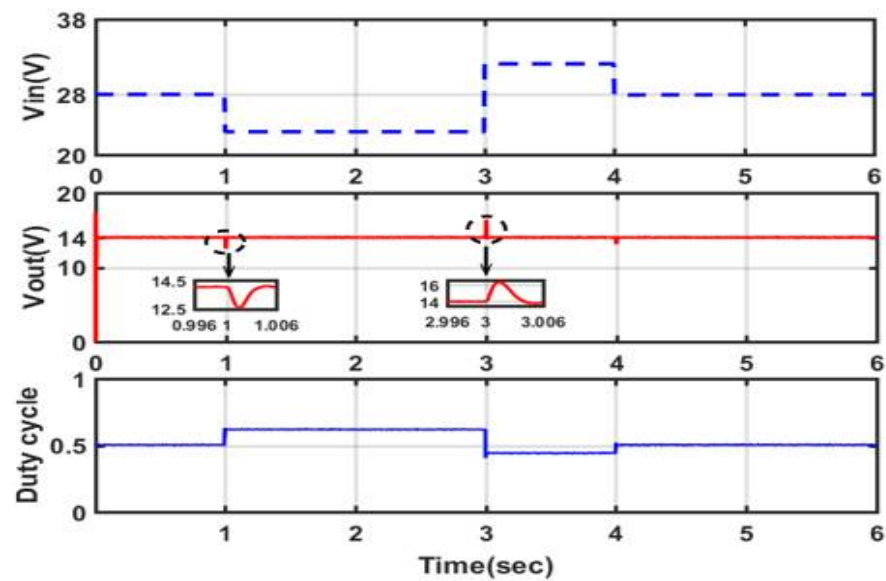


Figure 11. Changes in output voltage and duty cycle with an RST controller in response to input voltage variation.



Figure 12. The experimental testbed. 1—OP4510 simulator; 2—dSPACE ds1104 Controller Box; 3—RT-LAB monitor console; 4—dSPACE control desk monitor; 5—Digital oscilloscope.

The suggested RST controller has been proved to be both robust and dynamically efficient, using the HIL experimental findings presented in Figures 14 and 15. The impact of varying the CPL on the output voltage is depicted in Figure 14, where we can see that the suggested RST controller operates accurately throughout the CPL fluctuation, and the output voltage remains stable and fast-tracked to the reference voltage of the system at 14 V. The duty cycle signal, as can be observed, is stable at 0.5 V. Figure 14 illustrates the effect of input voltage fluctuation on the output voltage; it can be seen that the proposed RST controller performs quite correctly when the input voltage changes, while the output voltage remains stable and fast-tracked to the reference voltage of 14 V. When the input voltage changes, the duty cycle signal changes from 0.5 V to 0.62 V, then to 0.44 V, and finally back to 0.5.

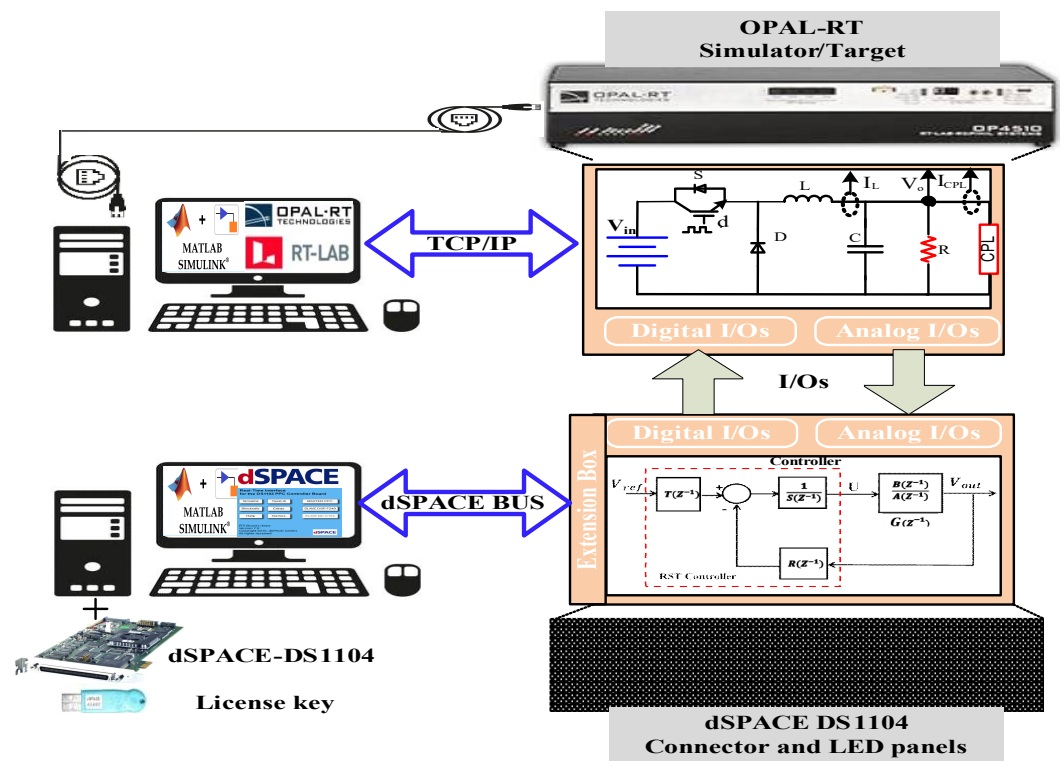


Figure 13. Block diagram of experimental HIL.

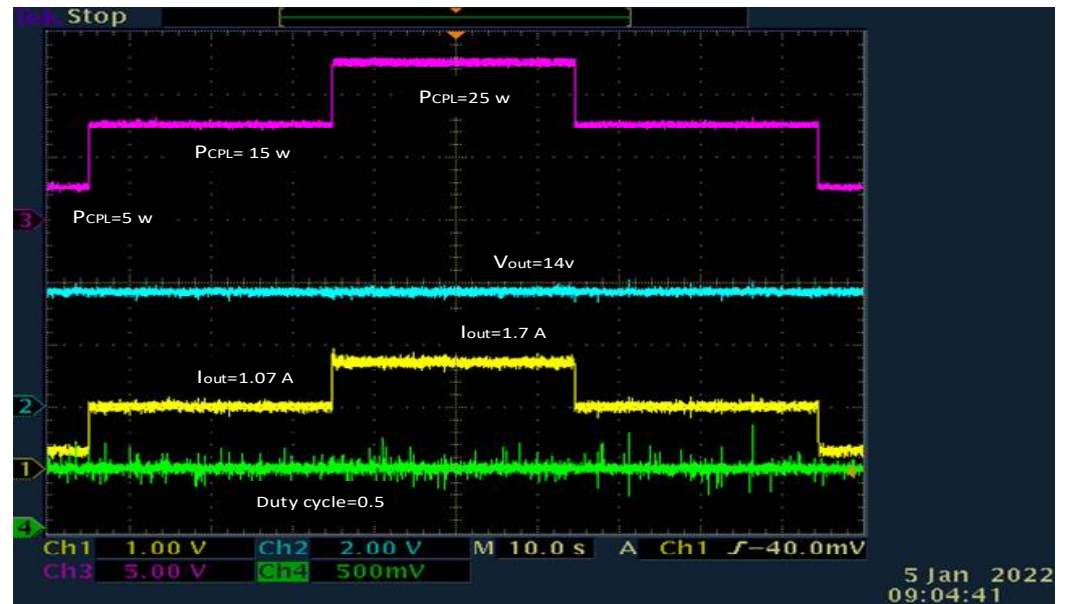


Figure 14. HIL experimental results of system with CPL variation.

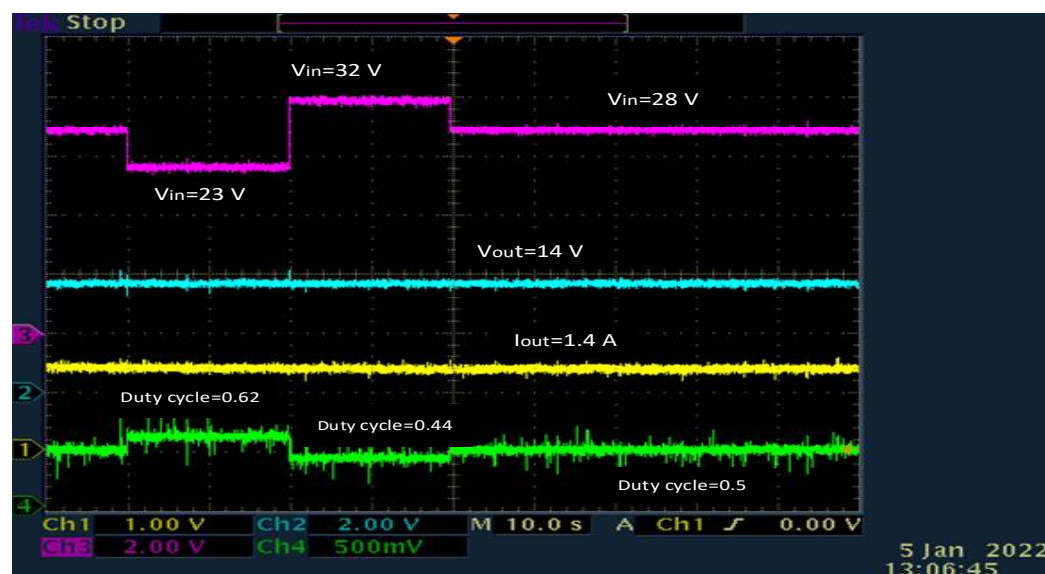


Figure 15. HIL experimental results of system with input voltage variation.

6. Conclusions

This article discussed the instability issue that arises when a DC/DC buck power converter is used to power a CPL in DC microgrid systems. The study proposed and implemented an RST digital feedback controller to stabilize the system and minimize steady-state error induced by system disturbances such as input voltage and load variations. To begin, a model of the system was developed. Then, to regulate the system, a robust digital RST controller was built by combining pole placement with a sensitivity function shaping method. To evaluate the control performance, MATLAB/Simulink simulations were used to compare the conventional closed loop PI linear controller to the proposed RST. Additionally, the RST controller was validated on the and HIL real-time experimental platforms to be both robust and dynamically efficient. According to the findings, the proposed control strategy may demonstrate good performance in terms of recovery, settling time, and overshoot when the load and input voltage are changed. The droop control scheme for DC microgrids with multiple energy storage devices to assure both voltage regulation and equal load sharing might be a useful study area for future work.

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