

Article

# A New Hybrid Synchronization PLL Scheme for Interconnecting Renewable Energy Sources to an Abnormal Electric Grid

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**Abstract:** Today, and especially with the growing interest in distributed renewable energy sources (DRESs), modern electric power systems are becoming more and more complex. In order to increase DRES penetration, grid side converter (GSC) control techniques require appropriate synchronization algorithms that are able to detect the grid voltage status as fast and accurately as possible. The drawbacks of the published synchronization phase-locked loop (PLL) techniques were structured mainly around the slow dynamic responses, the inaccuracy of extracting the fundamental components of the grid voltages when they contain a DC offset, and the worsening of the imbalance rejection ability facing significant frequency changing. This paper proposes a new synchronization PLL technique ensuring efficient and reliable integration of DRESs under normal, abnormal, and harmonically distorted grid conditions. The proposed PLL uses the mixed second- and third-order generalized integrator (MSTOGI) in the prefiltering stage through its adaptability to power quality and numerous grid conditions and its low sensitivity to input DC and inter-harmonics. Moreover, a modified quasi type-1 PLL (MQT1-PLL), which integrates two compensation blocks for phase and amplitude errors, respectively, has been used in the control loop. The discussion of sizing requirements and the effectiveness of the so-called MSTOGI-MQT1-PLL are tested under grid voltage imbalances and distortions and confirmed through simulation results compared to double second-order generalized integrator PLL (DSOGI-PLL), cascaded delayed signal cancellation PLL (CDSC-PLL), and multiple delayed-signal cancellation PLL (MDSC-PLL).

**Keywords:** synchronization; phase locked loop (PLL); mixed second- and third-order generalized integrator (MSTOGI); delayed-signal cancellation (DSC); moving average filter (MAF); distorted grid conditions; MQT1-PLL

**MSC:** 93C95



**Citation:** Alturki, M.; Abbassi, R.; Albaker, A.; Jerbi, H. A New Hybrid Synchronization PLL Scheme for Interconnecting Renewable Energy Sources to an Abnormal Electric Grid. *Mathematics* **2022**, *10*, 1101. <https://doi.org/10.3390/math10071101>

Academic Editors: Haitao Li, June Feng, Ben Niu and Shihua Fu

Received: 16 February 2022

Accepted: 26 March 2022

Published: 29 March 2022

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## 1. Introduction

Renewable energy sources (RESs), energy sources that are generally placed close to local loads and which may, in some cases, offer complete power to the local system, have been seen primarily as an energy solution for remote areas or as an emergency alternative energy [1]. Today, these sources of energy are seen not only as an important solution to improve the capacity and energy availability of the planet but also as a means of countering current issues such as climate change and greenhouse gas emissions (GHG) [2,3]. The optimal use of distributed energy resources (DER) requires the integration of these

resources with the local network or even the parallelization of decentralized energy sources with those of the network [4,5]. In this context, today's electric power system is undergoing rapid changes due to the integration of DRESs [6–11]. This integration, mainly ensured by the grid side converter (GSC), is limited by significant technical barriers, including the unintentional island mode operation of decentralized generation units following grid imbalance, loss, or disconnection [12,13].

In accordance with modern power system regulations and the growth of the recent control systems [14,15], the GSCs and their control algorithms must be equipped with advanced functionalities to allow them to operate regardless of grid conditions [16,17]. To accomplish this task, the GSC converter control system is split into three main modules: the external control loop module taking care of the regulation of the active/reactive power exchanged, the internal control loop module of the currents, and the synchronization module [18].

The active and reactive power controller performs the generation of the current references, which are then processed by the current controller to generate the required powers [19]. Furthermore, the synchronization module is responsible for instantaneously extracting information relating to the phase angle and frequency of the grid voltage, which are essential for the accurate functioning of control loops [20]. During significant grid disturbances, the GSC converter is found to be incompatible with remaining interconnected, without well-designed control strategies relying upon vigorous synchronization techniques [21]. The phase-locked loop synchronization technique is recognized as an indispensable process for detecting the phase, amplitude, and frequency of the grid voltage in a fast and accurate way [12,22]. This is crucial for the design of a control system capable of enabling the GSC to contribute appropriately to global grid stability, even in the event of the occurrence of disturbances.

This issue is becoming more and more paramount to allow energy sector operators and managers to ensure short- and long-term energy efficiency and the management of bidirectional energy flows between electrical energy production sources and coordinated consumption. The growing interest in distributed power generation systems (DPGSs) based on renewable energy has increased the number of topologies that have appeared for integrating renewable power source-based systems into the electricity grid [23,24]. In applications connected to the power supply network, the interfacing of the electricity production from renewable energy sources to the grid is ensured mainly by a DC-AC converter and a filter attenuating the harmonics of the currents injected at the grid [25–27].

It is obvious that the power electronics converters are a key and strategic point for energy production and management [28]. Similar to renewable energy productions, advanced studies in the field of power electronics converters are also growing faster than foreseen [29]. More and more demanding specifications in power electronics dictate that the GSC should have an excess capacity that can be exploited to participate in ancillary services to the main grid [30,31]. These requirements are prescribed by restrictive standards on the quality of the energy produced and distributed (IEEE\_1547, 2018), in particular on the harmonics induced by the GSC switching [32]. To achieve these objectives, recent research works have considered two methods, namely the development of new control strategies and the implementation of new structures or topologies of the GSC converter [27,28,31]. However, with a view to developing such converter control strategies, particular attention has been paid to techniques of synchronization with the network. In recent years, these techniques have experienced exponential development [33–35]. This development is mainly motivated both by the increase in the rate of integrating RESs into the modern electricity system, its harmful consequences for the stability of the network, and by the increasingly stringent requirements of power quality [36].

In modern electrical networks, the voltage may vary temporarily due to fluctuations in production, load, or a short circuit. Sudden fluctuations cause a voltage dip, the depth and duration of which vary according to the characteristics of the network and the production groups concerned [37]. In particular, the behavior of RES systems in the face of voltage dips and their resistance to disturbances under fault conditions have attracted several studies

from around the world [38]. It has been shown that GSC inverters have a high sensitivity to imbalances in the network voltage, which can cause their untimely disconnection. In [39], it has been shown that this sensitivity systematically depends on the types of faults, its position, the protection systems, and especially on the topology of the inverter and its control/command system (e.g., PLL, limit current of its control system).

In recent years, several published works have been suggested and investigated for improvement of the stability of grid-connected voltage source inverters (VSIs) interfacing renewable energy sources [34]. Among the published works, the majority of them emphasize the vital role of grid synchronization in grid-connected VSIs [37,38].

A precise PLL necessarily contributes to the enhancement of the stability of the RES-based systems connected to the network by guaranteeing that the currents injected into the network are in phase with the grid voltages. A PLL can also decrease total harmonic distortion (THD) and significantly advance the quality of the waveform of currents injected into the grid [36,39].

In the literature, several PLLs have been proposed; the main drawbacks of them are related to some issues in power quality such as frequency variations and voltage waveform distortions. Under balanced grid conditions, the synchronous reference frame (SRF) phase-locked loop (SRF-PLL) [40,41] has been a reasonable candidate due to its fast dynamic response, simple structure, and feasible software implementation.

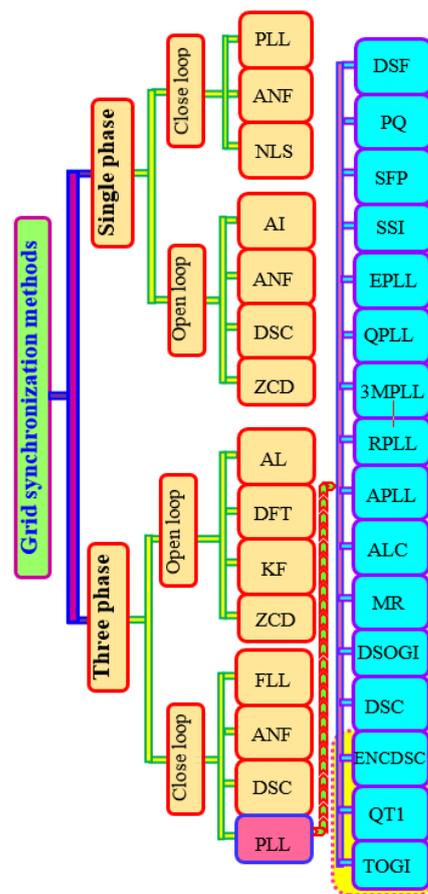
Nevertheless, the SRF-PLL method performance is severely degraded under off-nominal grid voltage conditions. Errors appear in tracking the fundamental component of the positive sequence voltages and disturb the whole control system of the grid-connected inverter.

In order to address the limitations of SRF-PLL when an imbalance and/or harmonics occur at the grid voltages, another method called double-decoupled SRF-PLL (DDSRF-PLL) has been suggested in [42]. Because of the use of a decoupling network, it has been proven that the DDSRF-PLL has succeeded in extracting the components of the positive and negative sequences and eliminating the oscillations that arise during grid voltage disturbances. Along with its benefits to achieve accurate phase-locking, however, the DDSRF-PLL has a rather complicated software implementation and a slow dynamic response due to the integrated low-pass filters [37].

Still, in the enumeration of the efforts of researchers with regard to the techniques of PLLs, another method called SOGI-PLL has been proposed. This method is based on using second-order generalized integrators. It has been shown that SOGI-PLL is simple and efficient even under faulty conditions of the grid voltages since it succeeds in mitigating the delay caused by the low-pass filter introduced by the DDSRF-PLL. Nevertheless, it has been demonstrated that the performance of the third-order generalized integrator-PLL (TOGI-PLL) and the SOGI-PLL technique and its derivatives SSOGI-PLL [43] and DSOGI-PLL [44] deteriorate, especially when a DC offset is present in grid voltages.

To address the last issue, other attempts [45] have tried to exploit the strengths of PI integrators and the Kalman filter to remove the DC offset. In the same context of eliminating the adverse effects of the DC offset on PLL techniques, a cascaded generalized integrator PLL (CGI-PLL) has been recently proposed by N. Hui et al. [21].

Among the options of the PLL pre-filtering step, the delayed signal cancellation (DSC) theory has become popular for extracting the fundamental component of grid voltages that is used by the synchronous reference frame PLL (SRF-PLL) [46]. Several derived approaches, such as the generalized DSC (GDSC), the multiple DSC (MDSC) [47,48], the cascaded (CDSC) and the non-adaptive CDSC (NCDSC), have been used [49]. In particular, the NCDSCs have succeeded in resolving the instabilities that are engendered by the CDSCs. Conversely, the major drawbacks of DSC-based operators are linked to two challenges associated, in turn, to the dynamic response and the rejection of imbalances for large and rapid changes in frequency. Figure 1 classifies the synchronization up-to-date techniques.



**Figure 1.** Overview on synchronization methods.

Within this context, the present paper investigates the development of a well-designed synchronization technique of grid-tied inverters. On the basis of a bibliographic review of Section 1, a detailed analysis of the TOGI approach from the SOGI perspective is conducted, and the MSTOGI-MQT1-PLL method is suggested in Section 2 and validated through simulations in Section 3. Finally, Section 4 summarizes and concludes the paper.

The foremost contributions of the current paper that propose a new synchronization phase-locked loop for DRESs are summarized as follows:

- The structure of the dual-mixed integrator MSTOGI involves an additional branch whose main advantage is the elimination of the DC offset of the input voltages, which is a weakness of the SOGI and TOGI integrators, without the addition of any new parameter.
- The non-adaptive MSTOGI perfectly performing the pre-filtering task overcomes the sensitivity of the classical filtering techniques to the DC offset of the grid voltage and to harmonics and inter-harmonics.
- The MQT1 technique is suggested to achieve phase locking. This technique was supported by two blocks that are responsible for compensating the amplitude error and the phase shift and correcting them independently of the frequency variation of the grid voltages.
- The coherent structure of the MSTOGI-MQT1-PLL showed promising performances in terms of the speed and accuracy of phase locking by comparing to the well-cited techniques DSOGI-PLL, CDSC-PLL, and MDSC-PLL.

## 2. Methods and Materials

In this section, knowing that the proposed PLL technique is based on a mixed MSTOGI integrator, the primary focus has analyzed TOGI from the SOGI point of view. Here,

the basic principle of the SOGI structure and its limitations have been revealed before presenting the TOGI structure and its ability to eliminate the DC offset. Thereafter this introduction, the MSTOGI-MQT1-PLL structure is described in detail.

2.1. Analysis of TOGI from SOGI Perspective

2.1.1. Basic Principle of SOGI Structure

The standard SOGI has been widely used for controlling and synchronizing the grid-tied converters. Its structure (Figure 2a) is mainly referred to as the quadrature signal generator.

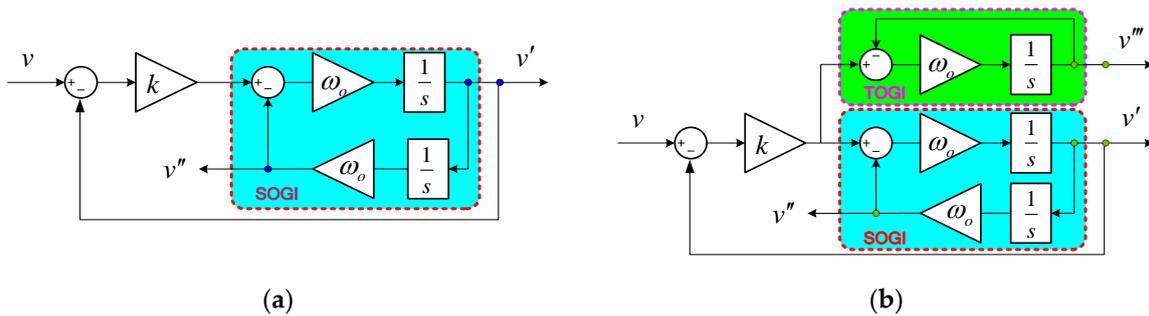


Figure 2. Block diagram of: SOGI structure(a) and MSTOGI structure (b) [45].

Assuming that the resonant frequency  $\omega_o$  is equal to that of the main grid (314 rad/s), and taking into account the orthogonal output signals  $v'$  and  $v''$ , the closed-loop transfer functions (CLTF) of SOGI are given by (1) and (2), respectively [43].

$$D_{\text{SOGI}}(s) = \frac{v'}{v}(s) = \frac{k \cdot \omega_o \cdot s}{s^2 + k \cdot \omega_o \cdot s + \omega_o^2} \tag{1}$$

$$Q_{\text{SOGI}}(s) = \frac{v''}{v}(s) = \frac{k \cdot \omega_o^2}{s^2 + k \cdot \omega_o \cdot s + \omega_o^2} \tag{2}$$

The Bode diagrams for various values of the damping factor  $k(0.5, 1, 1.5, 2)$  are provided in Figure 3.

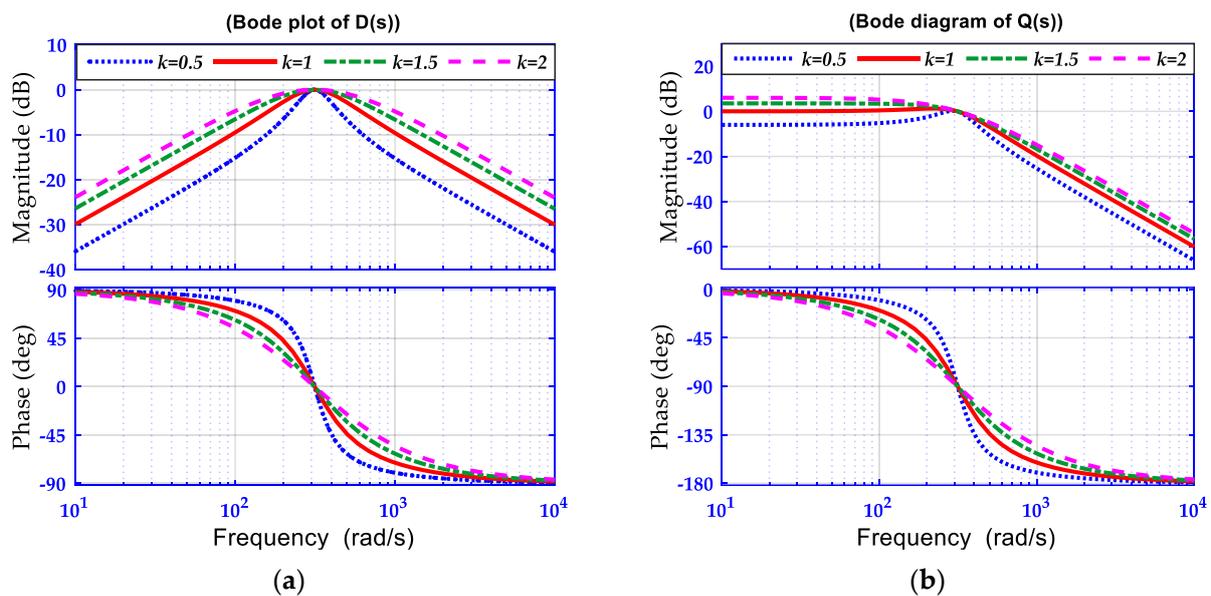


Figure 3. Bode diagrams of:  $D_{\text{SOGI}}(s)$  (a) and  $Q_{\text{SOGI}}(s)$  (b).

According to Bode’s plots of Figure 3a, it is shown that  $D_{\text{SOGI}}(s)$  is a second-order band-pass filter (SOBPF) with a phase shift of  $0^\circ$  at the resonance frequency  $\omega_o$  and unity gain. Pursuant to the different plots, the bandwidth strongly depends on the gain  $k$ . The filtering effect of  $D_{\text{SOGI}}(s)$  is better for a lower value of damping  $k$ , given that the more the parameter  $k$  weakens, the more the filtering capacity improves because the pass band becomes narrower.

Moreover, under these conditions, the reliance on the resonance frequency  $\omega_o$  is greatly increased. When the resonance frequency  $\omega_o$  is not the same as the input  $\omega_s$ , the output signal  $v'$  shows a significant phase shift and amplitude attenuation.

Likewise,  $Q_{\text{SOGI}}(s)$  is also a second-order low-pass filter (SOLPF) with a unitary gain but  $90^\circ$  out of phase at  $\omega_o$ . The static gain of  $Q_{\text{SOGI}}(s)$  is influenced in particular by the damping factor  $k$ . Because of that, for a lower value of  $k$ , the filtering effect is improved but the dynamics are deteriorated.

### 2.1.2. Problems Experienced by SOGI

Knowing that the band-pass filtering function of  $D_{\text{SOGI}}(s)$  results in the elimination of the DC offset from the input signal, this implies that the signal  $v'$ , as well, is devoid of the DC offset. Such a DC offset is removed by  $v'$  through the negative feed-forward loop returned to the incoming signal  $v$ . Conversely, taking into account the function of the low-pass filter played by  $Q_{\text{SOGI}}(s)$  and the event of the existence of a DC offset at the level of  $v$ , this gives rise to a DC offset with a gain of  $k$  at the level of  $v''$ . As a result, the detection of  $v$  signal amplitude and the PLL tracking on the grid voltages will be seriously affected.

To overcome these drawbacks and eliminate the DC offset of the SOGI inputs, the most promising solution is to exploit a third-order generalized integrator (TOGI) and combine it with the SOGI in a new structure called MSTOGI.

### 2.1.3. Structure of the TOGI

Aiming to improve the accuracy issues of the SOGI PLL, the developed TOGI-based PLL approach is depicted in Figure 2b. The transfer function of the TOGI is expressed in (3) [45].

$$\text{TOGI}(s) = \frac{v'''}{v}(s) = \frac{k \cdot \omega_o \cdot (s^2 + \omega_o^2)}{(s + \omega_o)(s^2 + k \cdot \omega_o \cdot s + \omega_o^2)} \tag{3}$$

In Figure 4, the Bode diagram of the third-order transfer function  $\text{TOGI}(s)$  is drawn for four values of the gain  $k$ .

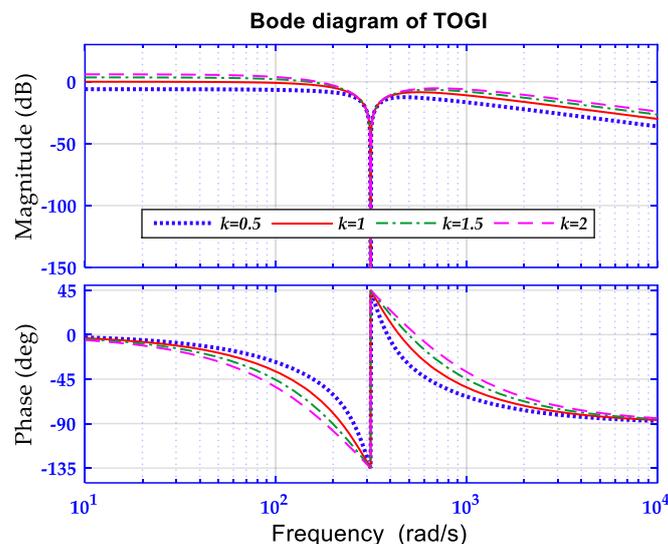


Figure 4. Bode diagram of the third-order transfer function  $\text{TOGI}(s)$ .

In accordance with the simulation results, it is clear that  $\text{TOGI}(s)$  is a notch filter (NF). It can be also deduced that the gain of this NF at  $\omega_o$  is zero and that its bandstop is centered at the same resonance frequency. Under these conditions,  $\text{TOGI}(s)$  is weakly able to mitigate the DC offset. In return,  $\text{TOGI}(s)$  makes it possible to act to deprive  $v'''$  of any component or effect of  $\omega_o$ , although the input signal contains it. In other words, this is because the component is blocked given that the magnitude (dB) of  $\text{TOGI}(s)$  at  $\omega_o$  is infinitely negative. This advantage can be a guarantee of the elimination of the input signal DC offset.

2.1.4. DC Offset Elimination Procedure Based on TOGI

Assuming that it is in a steady state, the input signal  $v$  is a sinusoidal voltage, of amplitude  $V_m$  volts and frequency  $\omega_g$ , on which a DC signal  $V_{dc}$  is superimposed as a DC offset. In the time domain and s-domain, the input signal can be expressed by (4) and (5), respectively.

$$v(t) = V_m \cdot \sin(\omega_g \cdot t + \varphi_g) + V_{dc} \tag{4}$$

$$v(s) = \frac{V_m \cdot (\omega_g \cdot \cos \varphi_g + s \cdot \sin \varphi_g)}{s^2 + \omega_g^2} + \frac{V_{dc}}{s} \tag{5}$$

Herein,  $\varphi_g$  is the phase angle jump that can be non-zero when the input signal is subjected to phase jump changes and zero otherwise.

Based on (1) and taking into account (5),  $v'(s)$  can be deduced as [45]:

$$\begin{aligned} v'(s) &= D(s) \cdot v(s) \\ &= \frac{k \cdot \omega_o \cdot s}{s^2 + k \cdot \omega_o \cdot s + \omega_o^2} \cdot \left[ \frac{V_m \cdot (\omega_g \cdot \cos \varphi_g + s \cdot \sin \varphi_g)}{s^2 + \omega_g^2} + \frac{V_{dc}}{s} \right] \end{aligned} \tag{6}$$

In order to compute the steady-state output in the time domain  $v'(t)$ , the application of the inverse Laplace transform leads to:

$$v'_\infty(t) = \frac{k \cdot \omega_o \cdot \omega_g}{\sqrt{k \cdot \omega_o^2 \cdot \omega_g^2 + (\omega_o^2 - \omega_g^2)^2}} \cdot V_m \cdot \sin\left(\omega_g \cdot t + \varphi_g + \arctan\left(\frac{\omega_o^2 - \omega_g^2}{k \cdot \omega_o \cdot \omega_g}\right)\right) \tag{7}$$

To ease the notation, two new parameters involved in the sine wave  $v'_\infty(t)$  are considered in (8):

$$\begin{cases} m = \frac{k \cdot \omega_o \cdot \omega_g}{\sqrt{k \cdot \omega_o^2 \cdot \omega_g^2 + (\omega_o^2 - \omega_g^2)^2}} \\ \varphi = \arctan\left(\frac{\omega_o^2 - \omega_g^2}{k \cdot \omega_o \cdot \omega_g}\right) \end{cases} \tag{8}$$

Accordingly, Equation (7) can be rewritten as:

$$v'_\infty(t) = m \cdot V_m \cdot \sin(\omega_g \cdot t + \varphi_g + \varphi) \tag{9}$$

Assuming the same notations,  $v''(t)$  and  $v'''(t)$  are obtained as:

$$v''_\infty(t) = k \cdot V_{dc} - m \cdot \frac{\omega_o}{\omega_g} \cdot V_m \cdot \cos(\omega_g \cdot t + \varphi_g + \varphi) \tag{10}$$

$$v'''_\infty(t) = k \cdot V_{dc} - k \cdot \omega_o \cdot V_m \cdot \sqrt{\frac{1 - m^2}{\omega_o^2 + \omega_g^2}} \cdot \cos(\omega_g \cdot t + \varphi_g + \varphi - \varphi_c) \tag{11}$$

The phase  $\varphi_c$  is defined as:

$$\varphi_c = \arctan\left(\frac{\omega_g}{\omega_o}\right) \tag{12}$$

In accordance with (7), the amplitude of the sinusoidal function  $v'_{\infty}(t)$  is imposed by the parameter  $m$ , while its phase angle is dictated by  $\varphi$ . According to (10), the expression of  $v'_{\infty}(t)$  shows the existence of a cosine component with a phase lag of  $90^\circ$  with respect to  $v'$ . On this cosine component, a DC offset proportional to  $V_{dc}$  is superimposed since the SOGI is not eligible to entirely mitigate it.

The same DC offset  $k \cdot V_{dc}$  is recorded in the expression for  $v'''_{\infty}(t)$ . For the three cases related to  $v'(t)$ ,  $v''(t)$ ,  $v'''(t)$  and for the different conditions of frequencies  $\omega_o$  and  $\omega_g$ , the parameters  $m$  and  $\varphi$  are determined as follows:

$$\begin{aligned}
 & \text{if } \omega_o = \omega_g, \quad \begin{cases} m = 1 \\ \varphi = 0 \end{cases} \\
 & \text{if } \omega_o \neq \omega_g, \quad \begin{cases} m < 1 \\ \varphi = +\arctan\left(\frac{\omega_o^2 - \omega_g^2}{k \cdot \omega_o \cdot \omega_g}\right) & \text{for } \omega_o < \omega_g \\ \varphi = -\arctan\left(\frac{\omega_o^2 - \omega_g^2}{k \cdot \omega_o \cdot \omega_g}\right) & \text{for } \omega_o > \omega_g \end{cases} \quad (13)
 \end{aligned}$$

In case  $\omega_o \neq \omega_g$ , the angle  $\varphi$  may lead to a phase shift and the attenuation factor  $m$  can act on the amplitudes of the signals  $v'(t)$ ,  $v''(t)$  and  $v'''(t)$ . Otherwise, when  $\omega_o = \omega_g$ ,  $m$  becomes unitary and has no influence on the amplitudes and the phase shift,  $\varphi$  becomes zero. Accordingly, Equation (9) can be re-established as:

$$v'_{\infty}(t)|_{\omega_o = \omega_g} = V_m \cdot \sin(\omega_g \cdot t + \varphi_g) \quad (14)$$

It is clear that the signal of the first output  $v'_{\infty}(t)$  is equal to the alternating part of the input signal  $v(t)$ . Assuming the same case ( $\omega_o = \omega_g$ ),  $v''_{\infty}(t)$  and  $v'''_{\infty}(t)$  are obtained:

$$v''_{\infty}(t)|_{\omega_o = \omega_g} = k \cdot V_{dc} - V_m \cdot \cos(\omega_g \cdot t + \varphi_g) \quad (15)$$

$v''_{\infty}(t)|_{\omega_o = \omega_g}$  is the sum of a cosine component at the same frequency and having the same amplitude as  $v(t)$  and the DC offset component  $k \cdot V_{dc}$ . When the phase angle jump  $\varphi_g$  is not zero, the expressions for  $v'_{\infty}(t)$  and  $v''_{\infty}(t)$  show an ability to follow closely any variation in the phase of the input signal  $v(t)$ .

As for the  $v'''_{\infty}(t)$ , this output signal is the only DC offset introduced in  $v''_{\infty}(t)|_{\omega_o = \omega_g}$ .

$$v'''_{\infty}(t)|_{\omega_o = \omega_g} = k \cdot V_{dc} \quad (16)$$

Based on the previous mathematical findings, the reconfiguration of the MSTOGI outputs allowing the elimination of the DC offset is depicted in Figure 5.

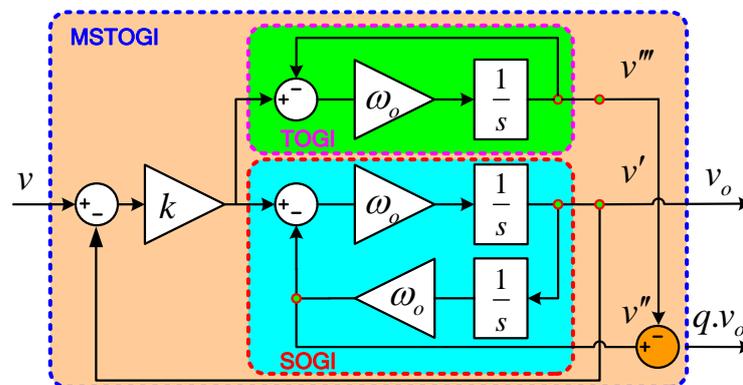


Figure 5. Block diagram of MSTOGI configuration.

Here, the output signals  $v_o$  and  $q \cdot v_o$  are orthogonal and their expressions are:

$$v_o = v' \tag{17}$$

and

$$q \cdot v_o = v'' - v''' \tag{18}$$

knowing that the transfer function from the input signal  $v(s)$  to the output  $v_o(s)$  is expressed in relation (1) and that from  $v(s)$  to  $q \cdot v_o(s)$  is called  $Q_{MSTOGI}(s)$  and is established by (19) [21].

$$Q_{MSTOGI}(s) = \frac{q \cdot v_o}{v}(s) = \frac{k \cdot \omega_o \cdot s \cdot (\omega_o - s)}{(s + \omega_o)(s^2 + k \cdot \omega_o \cdot s + \omega_o^2)} \tag{19}$$

Figure 6 shows four Bode plots of  $Q_{MSTOGI}(s)$  corresponding to four different values of the factor  $k$ . Because of the behavior of the MSTOGI structure, note the following important points:  $Q_{MSTOGI}(s)$  is a BPF whose gain and phase shift at the resonance frequency  $\omega_o$  are unity and  $90^\circ$ , respectively.

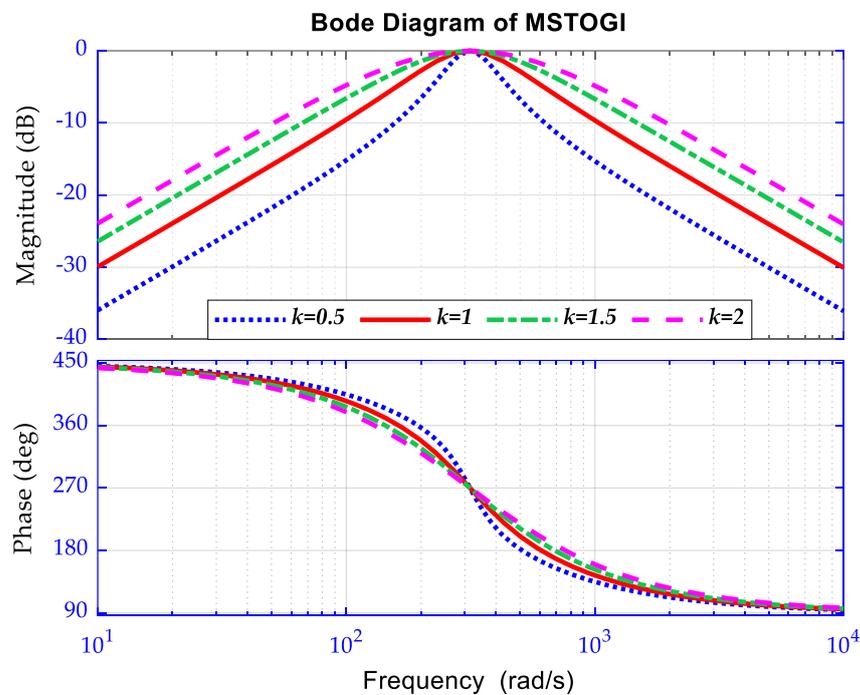


Figure 6. Bode diagrams of  $Q_{MSTOGI}(s)$ .

It can also be seen that the magnitude response in dB is similar to that of  $D(s)$ . The same plots show the important capability of MSTOGI to eliminate the high-frequency harmonics and, of course, the DC offset present in the input  $v$ . This is ensured due to the ability of the BPF filter to block components whose frequencies are much higher or lower than the two cutoff frequencies.

The pole-zero plots of the MSTOGI method are shown in Figure 7 for different values of the damping factor  $k$ . The stability is quite clear since all the poles are placed in the left half-plane. Moreover, when the parameter  $k$  increases, within the range of the chosen values 0.2 and 1.4, the dynamic response and the stability improve, but the quality of the filtering deteriorates. For  $k = 2.7$ , the location of the poles of  $D(s)$  shows that the dynamic response and the stability are less assured.

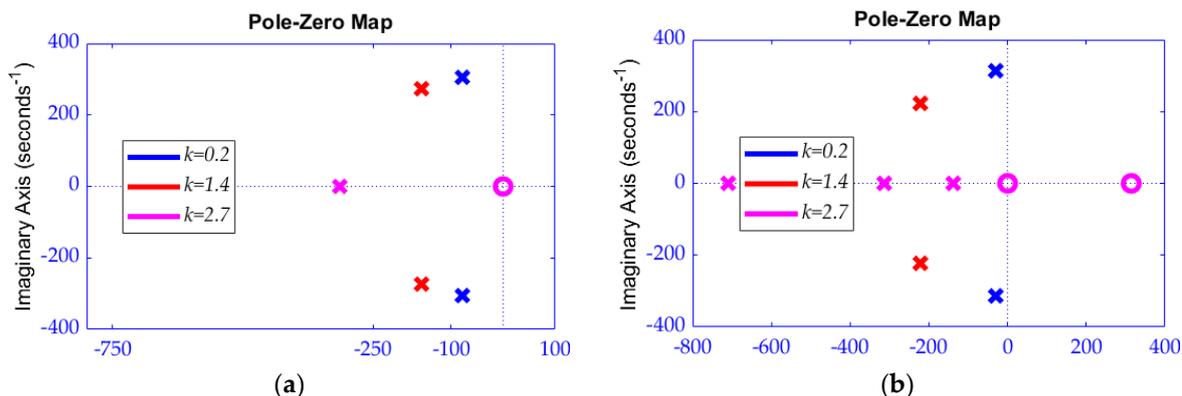


Figure 7. Pole-zero maps of MSTOGI:  $D(s)$  (a) and  $Q_{MSTOGI}(s)$  (b).

It can be seen from Figure 7b that the phase-frequency characteristics of  $Q_{MSTOGI}(s)$  are affected by the existence of a pair of symmetrical poles and zeros. Conversely, the amplitude-frequency plots of  $Q_{MSTOGI}(s)$  are not affected, although  $Q_{MSTOGI}(s)$  has the same drawings of amplitude-frequency curves, but distinct phase-frequency plots, as  $D(s)$ .

### 2.2. Suggested MSTOGI-MQT1-PLL

The proposed MSTOGI-MQT1-PLL is depicted in Figure 8. The pre-filtering structure introduces a dual MSTOGI structure. The voltages of the grid are transformed into their  $\alpha\beta$  components in the stationary reference frame. Such components are used as the inputs of two MSTOGI integrators to generate the orthogonal signals  $v_{o\alpha}, v_{o\beta}, q \cdot v_{o\alpha}$  and  $q \cdot v_{o\beta}$ . Knowing that the preceding signals are the fundamental components of the grid side voltages, they are then exploited by the block, calculating the fundamental positive sequence (FPSC) to take charge of the identification of the fundamental voltages of the positive sequence  $v_{\alpha}^{+}$  and  $v_{\beta}^{+}$ .

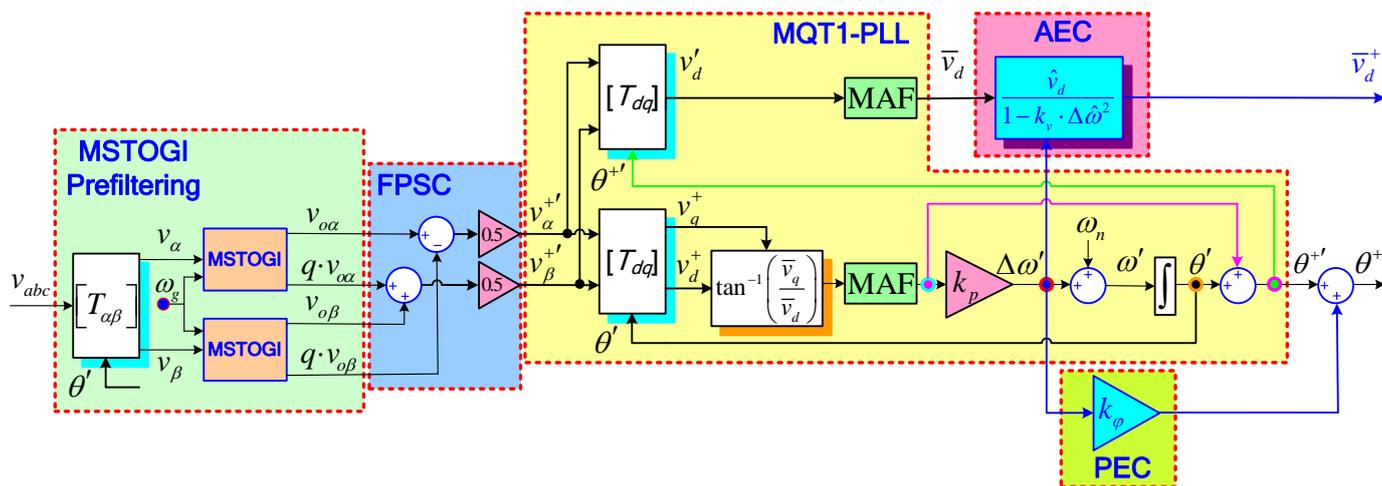


Figure 8. Bloc structure of proposed MSTOGI-MQT1-PLL.

Through the transformation  $[T_{\alpha\beta}]$ ,  $v_{\alpha}^{+}$  and  $v_{\beta}^{+}$  can be expressed according to (20) and (21), respectively:

$$v_{\alpha}^{+} = \frac{v_{\alpha} - q \cdot v_{\beta}}{2} \tag{20}$$

$$v_{\beta}^{+} = \frac{q \cdot v_{\alpha} + v_{\beta}}{2} \tag{21}$$

The operator  $q = e^{-\frac{j\pi}{2}}$  is responsible for creating a phase-shifted signal (in quadrature) from its original one. Taking into account the FPSC stage, the previous components  $v_{\alpha}^{+}$  and  $v_{\beta}^{+}$  can be rewritten as follows:

$$v_{\alpha}^{+} = \frac{v_{o\alpha} - q \cdot v_{o\beta}}{2} \quad (22)$$

$$v_{\beta}^{+} = \frac{q \cdot v_{o\alpha} + v_{o\beta}}{2} \quad (23)$$

### 2.2.1. Basic Principle of Modified Quasi Type-1 (MQT1) PLL Structure

The MQT1-PLL structure proposed in [50] was chosen to minimize the effect of the tracking error of low-order-type PLLs against network frequency changes [32]. It shows a satisfactory speed as regards the transient response and an important aptitude to reject disturbances.

The MQT1-PLL was recently proposed to overcome the shortcomings of the classic QT1-PLL, namely, the error generated during the assessment of the amplitude during the changes in the frequency of the grid voltages and the use of the real phase of the angle  $\theta$  necessary for the  $\alpha\beta/dq$  transformation, by taking into account the addition of the signal at the output of the integrator to that in the feedforward path.

Although greatly efficient, MQT1-PLL is not complex enough compared to QT1-PLL since only a Park conversion block ( $\alpha\beta/dq$ ), using the real-phase angle output, was added without imposing further filters. To minimize the number of filters used and not affecting the filtering capacity, the MAF filter was placed as shown in Figure 8.

### 2.2.2. Amplitude and Phase Error Compensation

Knowing that the precise tracking of the frequency of the grid is ensured due to the MAF filter and the non-adaptive DSC blocks, the estimation of the characteristic quantities of the grid voltage such as phase and amplitude can be deteriorated during rapid changes of the network frequency. To overcome this drawback, the two compensation blocks for phase (PEC) and amplitude (AEC) error compensation are used in the proposed structure to eliminate such errors.

## 3. Simulation Results and Discussion

In this section, the effectiveness of the proposed MSTOGI-MQT1-PLL as assessed through numerical simulation is shown. Simulations were carried out in a MATLAB/Simulink environment. The used MATLAB R2020a version was installed on a PC with an AMD Ryzen 7-3750H-RVM Gfx 2.30 GHz. Three different scenarios related to various grid voltage conditions were investigated. Throughout the simulations, the sampling frequency was considered to be equal to 8 kHz, the pulsation is 314 rad/s and the IEEE 1547–2018 standard was adopted [32].

### 3.1. First Scenario: Symmetrical Voltage Drop with Frequency Step Variation

The first scenario adopted for the simulations is as follows: at the instant  $t = 1$  s, a frequency step change of +2 Hz and symmetrical voltage drop of 0.4 of the grid voltage magnitude were imposed, as depicted in Figure 9.

Figure 10 shows the achieved simulation results for the DSOGI-PLL under the frequency step change and the adopted symmetrical voltage drop. The  $(\alpha, \beta)$  voltages in the stationary reference frame are shown in Figure 10a. The grid voltages estimating phase angle and frequency are shown in Figures 10b,c, respectively. It can be seen in Figure 10d that the frequency error becomes zero after many periods.

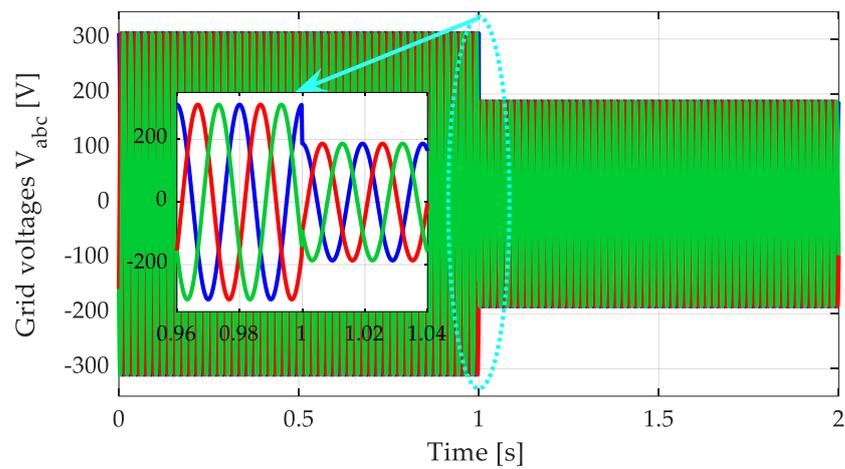


Figure 9. Grid voltages: scenario 1.

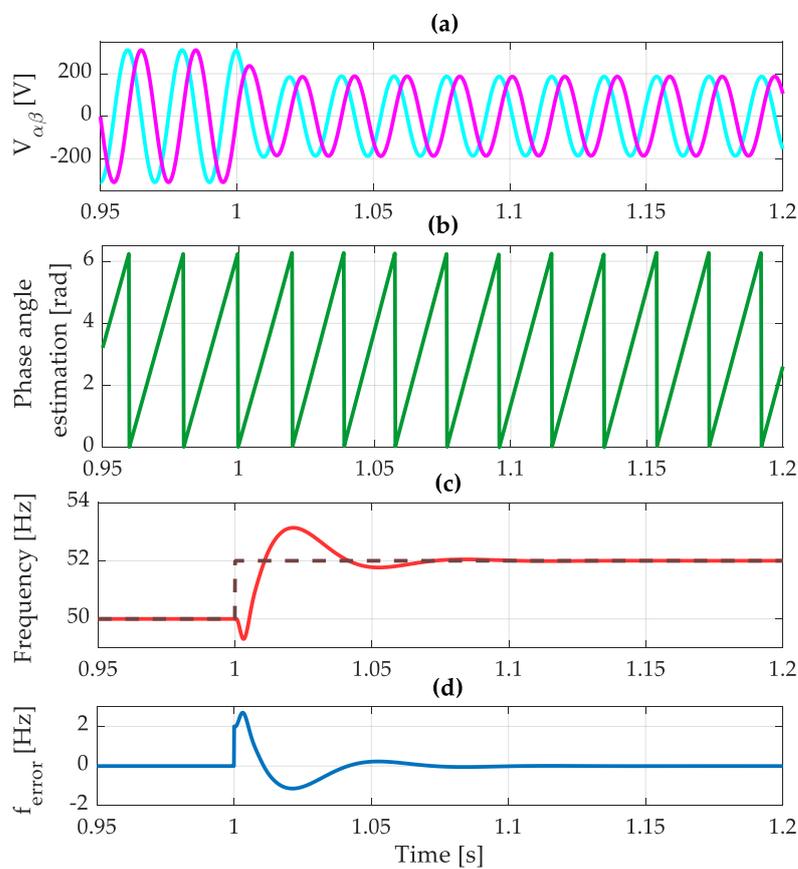
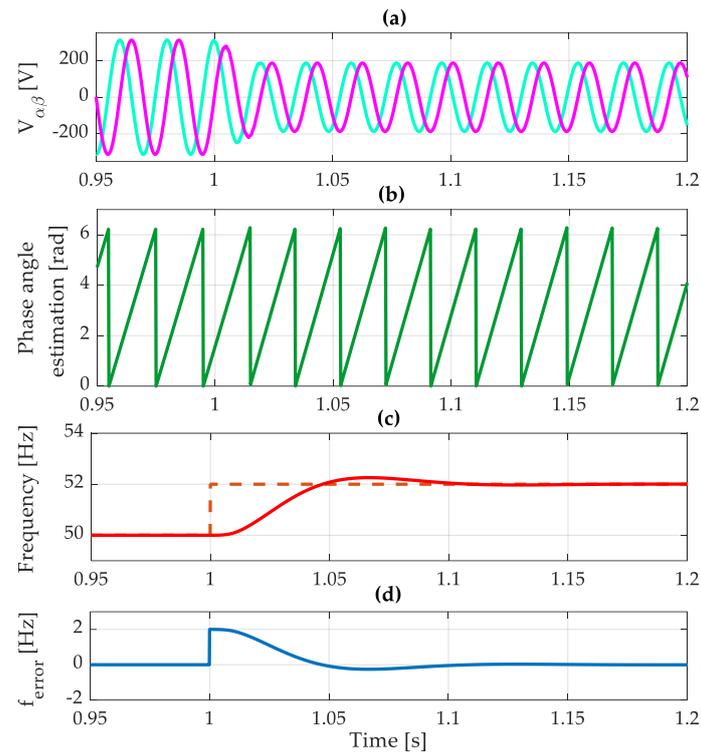


Figure 10. DSOGI-PLL performance for scenario 1:  $\alpha\beta$  voltages (a), phase angle (b), frequency (c), and frequency error (d).

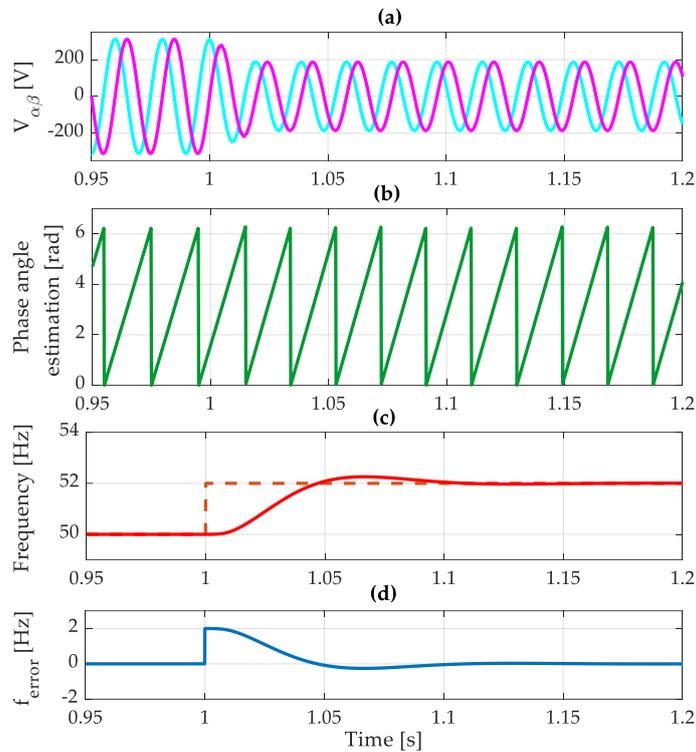
While the DSOGI-PLL succeeds in tracking the new angle of the grid voltages after a considerably long time, the error between the estimated frequency and the grid frequency shows an overshoot of the order of 2.6 Hz.

Under the same conditions of scenario 1 for the electrical grid, the performance of the CDSC-PLL technique was also questioned. Compared to DSOGI-PLL, Figure 11 shows that this technique has more performance in terms of accuracy because the overshoot does not exceed 2 Hz. However, CDSC-PLL is slower than DSOGI-PLL and manages to follow the angle of the grid voltages after a longer time.



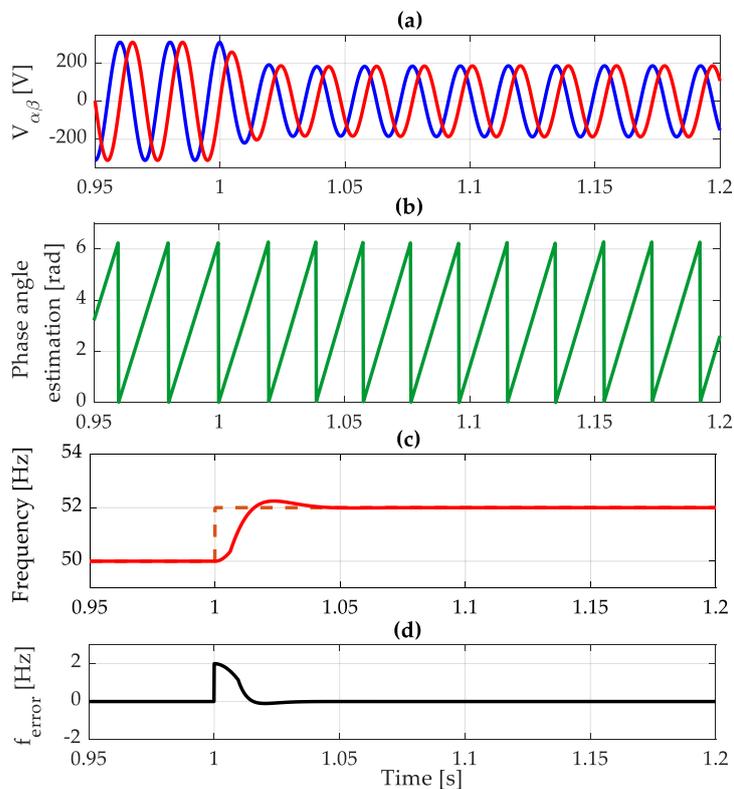
**Figure 11.** CDSC-PLL performance for scenario 1:  $\alpha\beta$  voltages (a), phase angle (b), frequency (c), and frequency error (d).

In terms of speed and precision, the CDSC-PLL and MDSC\_n-PLL techniques are similar, as shown in Figures 11 and 12.

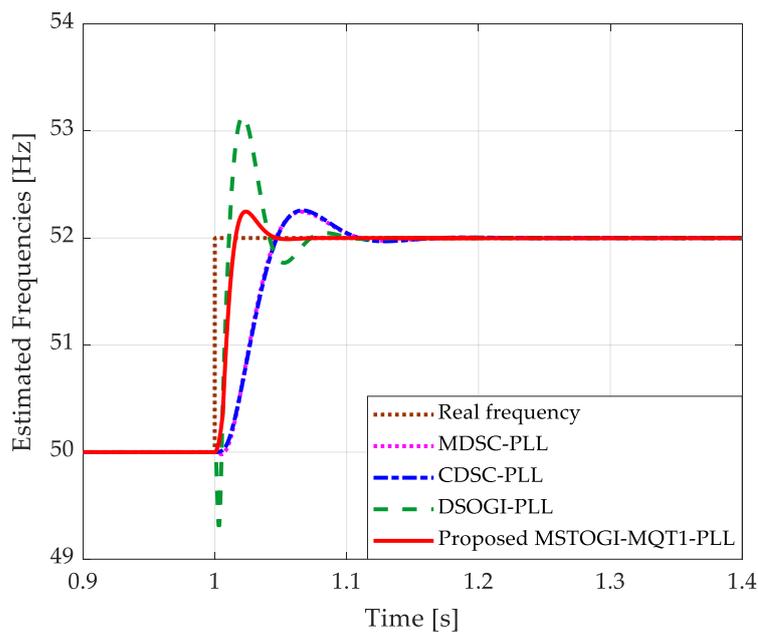


**Figure 12.** MDSC\_n-PLL performance for scenario 1:  $\alpha\beta$  voltages (a), phase angle (b), frequency (c), and frequency error (d).

Figure 13 shows that the MSTOGI-MQT1-PLL offers a zero steady-state frequency error and perfect tracking of the amplitude of the network voltages and frequency in the case of frequency variation. It can also be seen from the comparative simulations (Figures 10–14) that the MSTOGI-MQT1-PLL performs efficiently in terms of rapidity and accuracy of phase locking.



**Figure 13.** Proposed MSTOGI-MQT1-PLL performance for scenario 1:  $\alpha\beta$  voltages (a), phase angle (b), frequency (c), and frequency error (d).



**Figure 14.** Estimated frequency for all studied methods.

3.2. Second Scenario: Distorted Grid Condition

The results of the simulations dealing with the dynamic response of the proposed method in the presence of a frequency step of  $-1$  Hz of the grid voltages with the harmonic content shown in Table 1 are presented in Figure 15 [51]. It is shown that MSTOGI-MQT1-PLL is better than the other techniques in terms of filtering capacity and dynamic performance. The filtering achieved by the MAF is judged to be effective since it succeeds in blocking harmonics and greatly attenuates inter-harmonics.

Table 1. Harmonic composition of scenario 2.

Harmonic Order	THD (%)
5th harmonic	10
7th harmonic	10
11th harmonic	5
13th harmonic	5

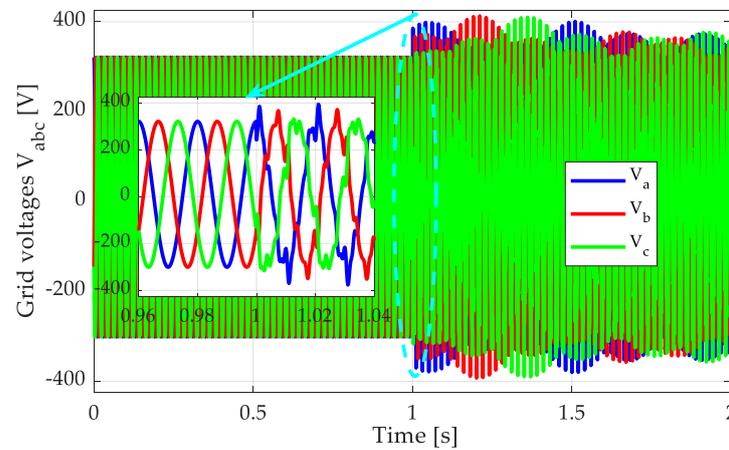


Figure 15. Grid voltages: scenario 2.

Figure 16 is focused on the dynamic performance of the proposed synchronization technique MSTOGI-MQT1-PLL, compared to the classic DSOGI-PLL, under the same conditions of scenario 2. The voltage  $V_a$  of the electrical grid is displayed on the same time axis with the output phase angle generated by the proposed method ( $\hat{\theta}_{\text{MSTOGI-MQT1-PLL}}^+$ ) and that achieved by the classical DSOGI technique ( $\hat{\theta}_{\text{DSOGI-PLL}}^+$ ). Here, it is noteworthy that a scale adjustment (in the form of multiplication by 0.02) has been applied to such a voltage waveform to stress the dynamic response of the two techniques with respect to the temporal evolution of the voltage and mainly during the zero crossings. It is shown that the reaction of the phase angle  $\hat{\theta}_{\text{MSTOGI-MQT1-PLL}}^+$  is manifested instantaneously from the instant  $t_0$ . This reaction results in the occurrence of an error due to the nonlinear increase in the estimated angle  $\hat{\theta}_{\text{MSTOGI-MQT1-PLL}}^+$  with a downward fluctuating bulge. Following this regime, precise tracking of the grid voltage is reached from  $t_1$ . Otherwise, the DSOGI-PLL achieves accurate tracking at  $t_2$ , which can be approximated to three grid periods. In other words, compared to those of DSOGI-PLL, the shown dynamic results verify that the output establishment time of MSTOGI-PLL is clearly faster and the dynamic response time of the phase lock in terms of accuracy is obviously better.

The performance of the MSTOGI-MQT1-PLL is assessed through simulation results and comparison with CDSC-PLL, MDSC-PLL, and DSOGI-PLL under scenario 2 conditions in the presence of a frequency variation and dominant harmonics of the grid voltages at the same time. Figure 17 proves that the MSTOGI-MQT1-PLL is efficient in terms of response dynamic, disturbance rejection and filtering ability.

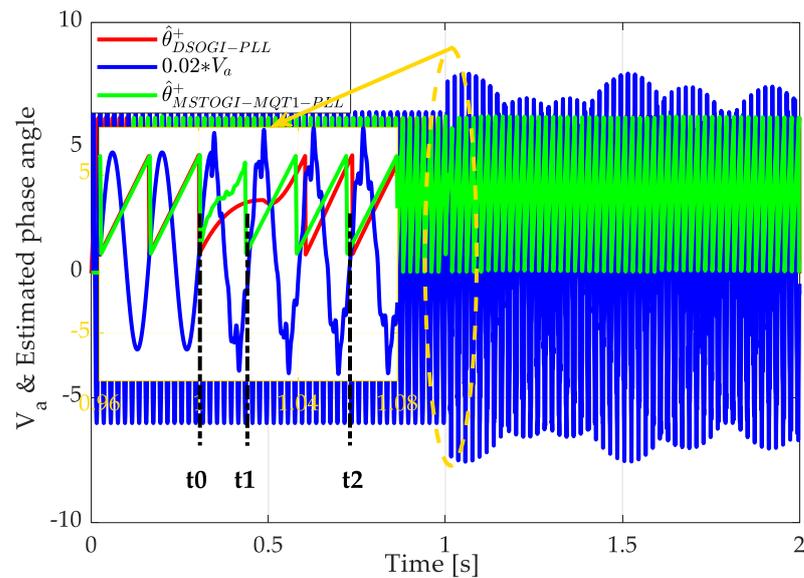


Figure 16. Dynamic performance of the proposed MSTOGI-MQT1-PLL and the DSOGI-PLL.

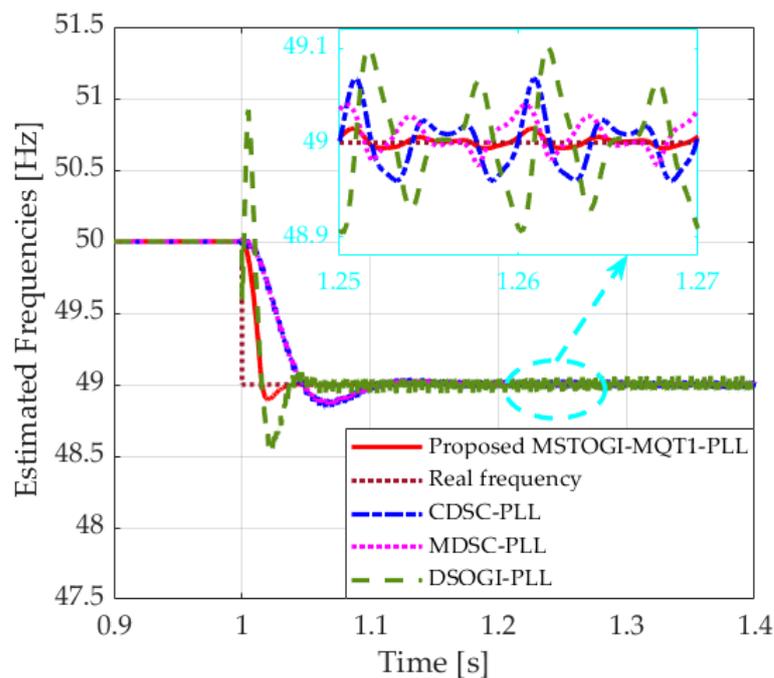


Figure 17. Estimated frequency for all studied methods for scenario 2.

### 3.3. Third Scenario: Asymmetrical Voltage Sag and Distorted Condition

This section is devoted to the assessment of the MSTOGI-MQT1-PLL performance under an asymmetrical voltage sag at the phase “a” of 50% of its amplitude and a frequency step change of  $-1$  Hz. The harmonic composition is similar to that of scenario 2 (See Table 1). The adopted scenario begins at the instant 1 s. Under these conditions, the magnitudes of the other two phases are unchanged, as shown in Figure 18.

The efficiency of the suggested method has been tested by simulations performed under the third scenario. Particular attention has been paid to the deviation of the grid frequency from the reference nominal value. The proposed MSTOGI-MQT1-PLL is compared to the three studied advanced synchronization PLLs.

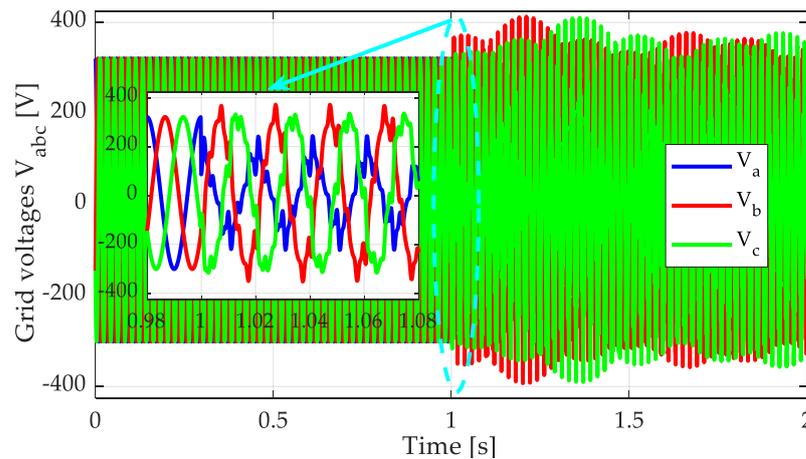


Figure 18. Grid voltages: scenario 3.

As shown in Figure 19, the proposed MSTOGI-MQT1-PLL reveals a perfect phase-locking ability. Particularly, it can be noticeably confirmed that the DSOGI-PLL technique suffers from double frequency fluctuations superimposed to the estimated frequency average value. Herein, the peak-to-peak frequency error of the MSTOGI-MQT1-PLL is negligible compared to those of CDSC-PLL, MDSC-PLL, and predominantly for that of the DSOGI-PLL.

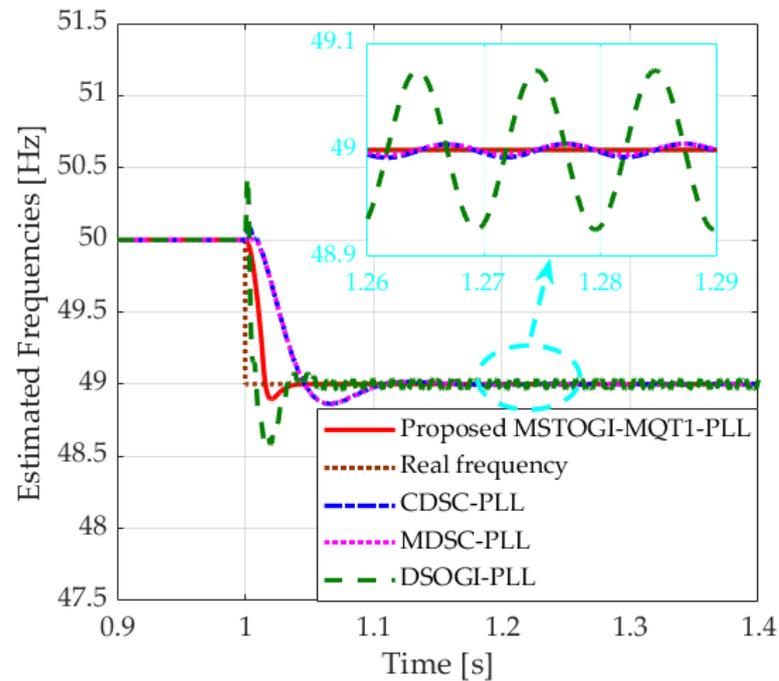


Figure 19. Estimated frequency for all studied methods for scenario 3.

It should also be particularly stressed that the results of scenario 3 show that, among all PLLs, only MSTOGI-MQT1-PLL wholly removes the double frequency fluctuations.

The detailed comparison of MSTOGI-MQT1-PLL with other PLL techniques such as DSOGI-PLL, MDSC-PLL, and CDSC-PLL is provided for different grid conditions. In Table 2, it is clearly shown that the proposed PLL achieves the most satisfactory performance for various power quality problems including symmetrical voltage sags, asymmetrical voltage sags and harmonics. As a further result, the MSTOGI-MQT1 PLL exhibits a good dynamic response and a steady state under such grid voltage conditions.

**Table 2.** Summary of results.

#	Grid Voltages			Frequency Overshoot			
	Voltage Sag	Frequency Step	Harmonics	DSOGI-PLL	MDSC-PLL	CDSC-PLL	MSTOGI-MQT1-PLL
Scenario 1	Symmetrical	+2 Hz	No	+1.1346 −0.6916	+0.2463 −0.0197	+0.2580 −0.0313	<b>+0.2272</b> <b>−0.1009</b>
Scenario 2	No	−1 Hz	Yes	+0.4325 −0.4165	+0.0085 −0.1196	+0.0908 −0.1302	<b>+0</b> <b>−0.1041</b>
Scenario 3	Asymmetrical	−1 Hz	Yes	+0.4424 −0.4275	+0.0097 −0.1373	+0.0917 −0.1369	<b>+0</b> <b>−0.1083</b>

In addition, the considerable superiority of the MSTOGI-MQT1-PLL among other PLLs is proven in terms of its speed and accuracy since it is the most performant technique in joining the grid frequency for the shortest period of time.

#### 4. Summary and Conclusions

In this paper, a new, accurate and fast MSTOGI-MQT1-PLL was suggested. The MSTOGI-MQT1-PLL structure relies on employing a non-adaptive dual MSTOGI integrator responsible for the PLL prefiltering stage and the MQT1 for the phase locking.

Unlike the SOGI and TOGI operators and their sensitivity to the grid voltage DC offset, harmonics, and inter-harmonics, the combination of them in an MSTOGI operator succeeds in performing as an ideal filter and removes the detrimental effects caused by such factors. A deep study into the frequency domain was also accomplished. In turn, the MQT1-PLL was proposed to fix the amplitude and phase detection errors. In the MQT1, two simple and efficient blocks charged for the compensation of the amplitude error and the phase shift, called AEC and PEC, respectively, were introduced. The main strength of the PEC compensator is that it manages to compensate the phase shift that can be generated, no matter the frequency of the grid voltages, since it is designed without being limited by any assumption on the choice of such frequency.

Through the simulation results and comparative study, the proposed MSTOGI-MQT1-PLL is a favorable PLL technique candidate since it has the highest performance in accomplishing fast and more accurate phase-locking than DSOGI-PLL, CDSC-PLL, and MDSC-PLL.

The obtained results clearly show that the proposed method, based on MSTOGI-MQT1, is promising and can be characterized as a valuable tool for the synchronization of DRESs to the power grid even under faulty and/or harmonic pollution conditions since it exhibits good achievements in terms of accuracy, speed, and in solving the nonlinear formulations of the synchronization problem. Regarding the limits of this method, its performance in some other grid scenarios, where the number of harmonics is greater and the computational burden is more enormous, remains to be practically verified.

Consequently, it is absolutely recommended for future works to experiment with the proposed method and validate its real performances to fulfill further benefits in the growing problem of integration of renewable energy-based generators in the power system.

**Author Contributions:** Conceptualization, R.A., M.A., A.A. and H.J.; methodology, R.A., M.A., A.A. and H.J.; software, R.A., M.A. and A.A.; validation, R.A., M.A., A.A. and H.J.; formal analysis, R.A., M.A., A.A. and H.J.; investigation, R.A., M.A., A.A. and H.J.; resources, R.A., M.A., A.A. and H.J.; data curation, R.A., M.A., A.A. and H.J.; writing—original draft preparation, R.A., M.A., A.A. and H.J.; writing—review and editing, R.A., M.A., A.A. and H.J.; visualization, R.A., M.A., A.A. and H.J.; supervision, R.A., M.A., A.A. and H.J.; project administration, R.A., M.A., A.A. and H.J.; funding acquisition, R.A., M.A., A.A. and H.J. All authors have read and agreed to the published version of the manuscript.

**Institutional Review Board Statement:** Not applicable.

**Informed Consent Statement:** Not applicable.

**Data Availability Statement:** Not applicable.

**Acknowledgments:** This research was funded by the Scientific Research Deanship at University of Ha'il—Saudi Arabia, through project number (BA-2106).

**Conflicts of Interest:** The authors declare no conflict of interest.

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