



Article Novel High-Efficiency High Step-Up DC–DC Converter with Soft Switching and Low Component Voltage Stress for Photovoltaic System

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Abstract: This study developed a novel, high-efficiency, high step-up DC–DC converter for photovoltaic (PV) systems. The converter can step-up the low output voltage of PV modules to the voltage level of the inverter and is used to feed into the grid. The converter can achieve a high step-up voltage through its architecture consisting of a three-winding coupled inductor common iron core on the low-voltage side and a half-wave voltage doubler circuit on the high-voltage side. The leakage inductance energy generated by the coupling inductor during the conversion process can be recovered by the capacitor on the low-voltage side to reduce the voltage surge on the power switch, which gives the power switch of the circuit a soft-switching effect. In addition, the half-wave voltage doubler circuit on the high-voltage side can recover the leakage inductance energy of the tertiary side and increase the output voltage. The advantages of the circuit are low loss, high efficiency, high conversion ratio, and low component voltage stress. Finally, a 500-W high step-up converter was experimentally tested to verify the feasibility and practicability of the proposed architecture. The results revealed that the highest efficiency of the circuit is 98%.

Keywords: step-up DC–DC converter; photovoltaic (PV) systems; three-winding coupled inductor; voltage doubler circuit

1. Introduction

With the rapid development of science and technology and the progress of human civilization, the demand for energy has also greatly increased. The energy employed has also changed from reliance on the kinetic energy produced by animals to the now-common use of coal and fossil fuels as energy sources. This evolution in the acquisition and use of energy has made daily life more convenient and comfortable [1].

However, because of rapid growth of the world's population, the demand for energy increases day by day, fossil fuels are gradually being depleted, and the excessive use of fossil fuels has severely damaged the environment, as indicated by extreme weather and global warming. This damage is the most urgent problem for humanity to address.

The field of green energy is experiencing a boom in Taiwan, with solar and wind power being the most widely used forms. However, these green energies are highly dependent on natural conditions and require high investment and maintenance costs, resulting in low power efficiency and high total power generation cost. In addition, the output voltage of reusable energies is low and unstable. Such energy must be converted using a first-stage step-up power converter before it can be used in households. Moreover, the output voltage of photovoltaic (PV) modules is too low at approximately 12–48 V. If PV modules are to be used effectively, the voltage must be increased to 380 ± 20 V through a high step-up converter, which enables the inverter to convert and connect to the grid, as illustrated in Figure 1. The conversion ratio of this type of high step-up converter must be at least 8. To satisfy this requirement, many high step-up converter structures have been recently



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Copyright: © 2021 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (https:// creativecommons.org/licenses/by/ 4.0/). researched and developed [2–9]. This study developed a novel high-efficiency high step-up converter with an input voltage of 48 V and output voltage of 380 V. After conversion by the inverter, the converter is connected to the grid and can function with high efficiency and at low cost.



Figure 1. Block diagram of green energy application.

2. Literature Review

The architecture of the converter proposed in this paper improves on that of the traditional Z-source step-up converter. This section details the converters with Z-source architecture that have been documented in the literature. Z-source step-up converters are divided into two categories: isolated and nonisolated. Figure 2 displays the circuit diagram of a traditional Z-source step-up converter [10–15]. The traditional Z-source step-up is achieved using the volt-second balance. The voltage gain of the converter is:

$$G_{Vo} = \frac{V_o}{V_{in}} = \frac{1}{1 - 2D}$$
(1)

However, the disadvantages of traditional Z-source step-up converters are the discontinuous input currents, high voltage stress of the capacitor, and the input and output terminals of nonisolated converters not sharing a common ground.

To compensate for the shortcomings of traditional Z-source step-up converters, the concept of the quasi-Z-source network was proposed [10,11,16–18]. This architecture has the same voltage gain as the Z-source architecture but solves the problems of discontinuous input currents, excessive capacitor voltage stress, and nonisolated converter input and output terminals not sharing a common ground.



Figure 2. Traditional Z-source converter [14].

In [10], the traditional quasi-Z-source step-up converter was used as the basic architecture and the architecture of a switched capacitor, and a switched inductor was added to increase the voltage gain of the converter. The advantage of this type of converter is that it is controlled by a single power switch and that the operation is relatively simple. In addition, the duty cycle does not need to be large to achieve high output voltage. However, the disadvantage is that having too many components leads to higher energy loss in the components, lower efficiency, and higher costs.

In [11], the traditional quasi-Z-source was again used as a step-up converter and one set of inductors was replaced with a series of switched-coupled-inductors in the architecture.

In [12], the authors proposed an isolated high step-up converter based on Z-source. This architecture uses a common core couple inductor, rather than two inductors, and includes a voltage doubler circuit on the secondary side. The architecture not only recovers the leakage inductance energy on the secondary side but also transfers the energy to the load to increase the output voltage. By using the volt-second balance of the circuit, the voltage gain can be obtained by:

$$G_{Vo} = \frac{V_o}{V_{in}} = \frac{2n(1+D)}{1-2D}$$
(2)

The advantage of this circuit architecture is that it does not require more components than the nonisolated type to achieve the circuit isolation effect. In addition, because the circuit has the function of inductance recovery, the voltage stress across the power switch and diode can be substantially reduced. Furthermore, the circuit does not require a high turns ratio to achieve a high voltage gain. However, the disadvantage is the discontinuous input current, which affects the stability of the device when used in green energy equipment.

In [13], an isolated high-boost converter based on quasi-Z-source architecture was proposed. The original energy storage inductor is replaced with a coupled inductor, and a voltage doubler circuit is added to the secondary side to achieve high voltage conversion. By using the volt-second balance, the voltage gain of the circuit can be obtained as follows:

$$G_{Vo} = \frac{V_o}{V_{in}} = \frac{n(1+D)}{1-2D}$$
(3)

The advantages of this circuit are similar to those of the circuit in [12], but the disadvantage of discontinuous input current is resolved, making the circuit more suitable for green energy systems than that of [12]. Unlike the Z-source architecture, the quasi-Z-source architecture uses only one set of coupled inductors to double the output voltage. The other coupled inductor is used to maintain a continuous input current, making voltage gain in the quasi-Z-source architecture lower than that in the Z-source architecture.

3. Circuit Architecture and Principle of Operation

Figure 3 displays the novel high step-up converter developed in this study. The circuit architecture consists of the following elements: two sets of switches, S_1 and S_2 ; a set of three-winding coupled inductors; two diodes, D_1 and D_2 ; and five capacitors, C_1 , C_2 , input capacitor C_i , output capacitor C_o , and the voltage doubler capacitor C_m . Figure 4 displays the operating waveforms of the main components of the operation mode. The circuit architecture proposed in this paper has 10 operating modes in a complete switching cycle. Each mode is analyzed below. To simplify the circuit analysis, the following assumptions were made:

- (1) The parasitic effect and internal resistance, which occur at high frequencies, are absent.
- (2) The switches and parasitic diodes of the switches are ideal, and the parasitic capacitance is considered.
- (3) The capacitance of C_1 , C_2 , C_i , C_o , and C_m is infinite.
- (4) The leakage inductance values L_{lk1} , L_{lk2} , and L_{lk3} are much lower than the magnetizing inductance L_m .



Figure 3. Circuit architecture of the proposed high step-up converter.



Figure 4. Key waveforms of the proposed topology.

(1) Mode I (t_0-t_1)

In this mode, switch S_1 is turned on in zero-voltage switching (ZVS), switch S_2 is turned off, and the power terminal stores energy to magnetize inductance L_m and leakage inductance L_{Lk1} through switch S_1 . Capacitors C_1 and C_2 discharge to leakage inductance L_{LK2} , increasing the currents of magnetizing inductance L_m and leakage inductance L_{LK2} . When the energy of leakage inductance L_{LK1} is released and becomes zero, the current of leakage inductance L_{LK1} begins to increase. The high-voltage side is freewheeling because of the leakage inductance L_{LK3} energy, and the leakage inductance energy and doubler voltage capacitor C_m are output to capacitor C_o and load R_o . Figure 5a indicates the operation of this mode.



Figure 5. Circuit diagram of operation (a-j) Modes I-X, respectively.

(2) Mode II $(t_1 - t_2)$

In this mode, switch S_1 is kept on, the currents of magnetizing inductance L_m and leakage inductance L_{LK1} continue to increase, and capacitors C_1 and C_2 resonate with leakage inductance L_{LK2} . The high-voltage side discharges leakage inductance L_{LK3} because the magnetizing inductance induces energy to the third winding, and the doubler voltage capacitor C_m stores energy through diode D_1 . The output capacitor C_0 is discharged to load R_0 . Figure 5b displays the operation of this mode.

(3) Mode III (t_2-t_3)

In this mode, switch S_1 is turned off. Because the inductance energy cannot be changed instantaneously, the primary side of leakage inductance L_{LK1} stores energy to parasitic capacitance C_{S1} of switch S_1 and capacitance C_1 and releases energy to parasitic

capacitance C_{S2} of switch S_2 ; leakage inductance L_{LK2} releases energy in reverse to capacitor C_2 . Figure 5c illustrates the operation of this mode.

(4) Mode IV (t_3-t_4)

In this mode, leakage inductance L_{LK1} continues to release energy to leakage inductance L_{LK2} and freewheel parasitic diode D_{S2} of switch S_2 . On the high-voltage side, the leakage inductance energy is greater than the energy of excitation inductance. Therefore, the current of leakage inductance L_{LK3} continues to store energy in doubler voltage capacitor C_m . When switch S_2 is turned on in ZVS, this mode ends. Figure 5d displays the operation of this mode.

(5) Mode V (t_4-t_5)

In this mode, switch S_2 is turned on in ZVS, switch S_1 is turned off, leakage inductance L_{LK1} continues to release energy to capacitors C_1 and C_2 , and leakage inductance L_{LK2} also releases energy. On the high-voltage side, leakage inductance L_{LK3} maintains the previous operating mode and continues to charge the doubler voltage capacitor C_m . When the energy of leakage inductance L_{LK3} is released and becomes zero, the mode ends. Figure 5e shows the operation of this mode.

(6) Mode VI (t_5-t_6)

In this mode, leakage inductance L_{LK1} continues to release energy to leakage inductance L_{LK2} and capacitors C_1 and C_2 . On the high-voltage side, the magnetizing inductance induces energy to the third winding and doubler voltage capacitor C_m and releases energy to output capacitor C_o and load R_o . When current I_{S2} changes from negative to zero, this mode ends. Figure 5f displays the operation of this mode.

(7) Mode VII (t_6 - t_7)

In this mode, the energy of L_{LK1} gradually decreases, and leakage inductance L_{LK2} releases energy through switch S_2 . On the high-voltage side, the previous operation mode is maintained. When the energy of leakage inductance L_{LK1} is released and becomes zero, this mode ends. Figure 5g illustrates the operation of this mode.

(8) Mode VIII (t_7-t_8)

In this mode, because the energy of L_{LK1} has been released and is now zero, capacitor C_1 discharges leakage inductance L_{LK1} in reverse. Leakage inductance L_{LK2} continues to release energy through switch S_2 . On the high-voltage side, the previous operation mode is maintained, and output capacitor C_0 releases to load R_0 . When switch S_2 is turned off, this mode ends. Figure 5h shows the operation of this mode.

(9) Mode IX (t_8-t_9)

In this mode, switch S_2 is turned off. Because the inductor current cannot be changed instantaneously, leakage inductance L_{LK1} charges parasitic capacitance C_{S2} of switch S_2 and discharges capacitance C_1 and parasitic capacitance C_{S1} of switch S_1 while leakage inductance L_{LK2} is freewheeling. On the high-voltage side, leakage inductance L_{LK3} maintains the previous mode, and doubler voltage capacitor C_m releases energy to output capacitor C_o and load R_o . Figure 5i indicates the operation of this mode.

(10) Mode X (t_9-t_{10})

In this mode, switch S_2 is turned off and the current of leakage inductance L_{LK1} is freewheeling through the parasitic diode of switch S_1 . The current of leakage inductance L_{LK2} is also freewheeling through the parasitic diode of switch S_1 and stores energy to capacitors C_1 and C_2 . On the high-voltage side, leakage inductance L_{LK3} maintains the previous mode, and doubler voltage capacitor C_m releases energy to output capacitor C_o and load R_o . When switch S_1 is turned on in ZVS and the energy of leakage inductance L_{LK2} is released and becomes zero, this mode ends. Figure 5j displays the operation of this mode.

4. Steady-State Analysis

The circuit analysis is performed in continuous current mode. The switching period is T_S , and the signal V_{gs1} is turned on for time D_1T_S (Mode II) and turned off for time $(1 - D_1)T_S$ (Mode VI) in the step-up mode. The following assumptions are made in the analysis of the proposed topology:

- (1) All components are ideal, and the internal resistance and parasitic effects are absent.
- (2) The capacitance of all capacitors is infinite, making the voltage of the capacitors constant.
- (3) The leakage inductance of the winging inductor is absent.
- (4) To make calculations easier, the ideal transformer is represented by $N = \frac{N_2}{N_1}$, and N is defined as the turns ratio of a transformer.

4.1. Voltage Gain Ratio

To derive the voltage gain ratio, switch S_1 is used as the main switch to analyze the voltage on the magnetizing inductance and calculate the voltage gain ratio. Figure 5b displays a circuit diagram for when switch S_1 is turned on. Because the purpose of the secondary side in the action mode is mainly to recover the leakage inductance, leakage inductance is ignored during the analysis. Therefore, when switch S_1 is turned on, the voltage across the magnetizing inductance can be obtained with Kirchhoff's voltage law as follows:

$$V_{Lm} = Lm \frac{\Delta \iota_{Lm}}{\Delta t} = V_{in} \tag{4}$$

The values obtained from (4) can be used to obtain the excitation current as follows:

$$\left(\Delta i_{Lm}\right)_{on} = \frac{V_{in}}{Lm} DT \tag{5}$$

The voltage of doubler voltage capacitor C_m is obtained as follows:

$$V_{Cm} = nV_{in}(n = \frac{N_3}{N_1}) \tag{6}$$

As illustrated by Figure 5f, when switch S_1 is turned off, (7) can be obtained with Kirchhoff's voltage law as follows:

$$V_{Lm} = Lm \frac{\Delta i_{Lm}}{\Delta t} = -\frac{(V_o - V_{Cm})}{n}$$
(7)

The values obtained from (7), can be used to obtain the excitation current as follows:

$$(\Delta i_{Lm})_{off} = -\frac{(V_o - V_{Cm})}{nLm} (1 - D)T$$
(8)

The voltage of doubler voltage capacitor C_m is:

$$V_{Cm} = nV_{in}(n = \frac{N_3}{N_1}) \tag{9}$$

Finally, the following equation can be obtained by using the volt-second balance:

$$(\Delta i_{Lm})_{on} + (\Delta i_{Lm})_{off} = 0 \tag{10}$$

By substituting (5), (6), and (8) into (10), the following equation can be obtained:

$$GV_o = \frac{V_o}{V_{in}} = \frac{n}{1-D} \tag{11}$$

4.2. Voltage Stress Analysis of Components

The components in the circuit can be derived and analyzed under the interactive action of the switch on and off. The voltage stress of switch S_1 is defined as the voltage stress when the switch is turned on in Mode II, as shown in Figure 5b:

$$V_{S1} = V_{in} - V_{Lm} = 0 (12)$$

Therefore:

$$V_{in} = V_{Lm} \tag{13}$$

When the switch is turned off in Mode VII, voltage stress can be obtained through the volt-second balance of magnetizing inductance L_m , as shown in Figure 5g:

$$V_{Lm}DT + V_{Lm}(1-D)T = 0 (14)$$

By substituting (13) and (14) into (15), the voltage stress of switch S_1 can be obtained:

$$V_{S1} = \frac{1}{1 - D} V_{in} \tag{15}$$

Capacitor C_1 can be used to calculate the voltage gain as $\frac{D}{1-D}V_{in}$, and the voltage stress of switch S_2 in Mode II can be analyzed, as shown in Figure 5b:

$$V_{in} + V_{C1} = V_{S2} \tag{16}$$

The voltage stress of switch S_2 is given by:

$$V_{S2} = \frac{1}{1 - D} V_{in} \tag{17}$$

The voltage stress of diode D_1 can be observed in Mode VIII, as shown in Figure 5h, and is defined as V_0 :

$$V_{D1} = V_o \tag{18}$$

The voltage stress of diode D_2 can be seen from Mode II, as shown in Figure 5b, and is defined as V_0 :

$$V_{D2} = V_o \tag{19}$$

The voltage stress of input capacitor C_{in} is V_{in} :

$$V_{Cin} = V_{in} \tag{20}$$

The voltage stress of output capacitor C_o is V_o :

$$V_{Co} = V_o \tag{21}$$

Capacitor C_1 is mainly used to recover leakage inductance energy in this circuit. Therefore, the circuit can be represented by the diagrams for operation modes I and V. Leakage inductance L_{LK1} is analyzed by turning the power switch on and off, and the voltage stress and voltage gain of capacitor C_1 can be calculated as follows:

$$V_{in}DT - V_{C1}(1-D)T = 0 (22)$$

$$GV_{C1} = \frac{D}{1 - D} V_{in} \tag{23}$$

The voltage stress of capacitor C_1 can be obtained as follows:

$$V_{\rm C1} = \frac{D}{1-D} V_{in} \tag{24}$$

The voltage gain and voltage stress of capacitor C_2 can be calculated by analyzing leakage inductance L_{LK2} when the power switches are turned off and on in Modes I and V:

$$-(V_{C1} + V_{C2})DT + (V_{in} - V_{C2})(1 - D)T = 0$$
(25)

By substituting (24) into (25), the voltage gain of capacitor C_2 can be obtained as follows:

$$-\frac{D^2}{1-D}V_{in} + V_{in}(1-D) = V_{C2}$$
(26)

$$GV_{C2} = \frac{1 - 2D}{1 - D} V_{in} \tag{27}$$

The voltage stress of capacitor C_2 is given by:

$$V_{C2} = \frac{1 - 2D}{1 - D} V_{in} \tag{28}$$

4.3. Literature Comparison

This section compares this study with others on isolated and nonisolated converters. Tables 1 and 2 list information including the number of parts used, input voltage, output voltage, output power, and efficiency. Table 1 presents a comparison of the proposed converter and nonisolated step-up converters, whereas Table 2 presents a comparison of the proposed converter with isolated step-up converters. The performance of the proposed converter was superior to that of the other converters.

Table 1. Comparison between the proposed converter and nonisolated step-up converters.

| References | Proposed Paper | Reference [10] | Reference [11] |
|-------------------------------|-----------------------|------------------------|---|
| Input voltage | 48 V | 24 V | 40 V |
| Output voltage | 380 V | 365 V | 200 V |
| Output power | 500 W | 200 W | 300 W |
| Number of switches | 2 | 1 | 1 |
| Number of diodes | 2 | 5 | 3 |
| Number of inductors | 0 | 3 | 1 |
| Number of coupled inductors | 1 | 0 | 1 |
| Voltage gain | $\frac{n}{1-D}$ | $\frac{2+D}{1-2D}$ | $rac{1+rac{1}{(1-n)}}{1-(2+rac{1}{1-n})}$ |
| Voltage stress on switch | $\frac{1}{1-D}V_{in}$ | $\frac{1}{1-2D}V_{in}$ | $\frac{1 + \frac{1}{(1-n)}}{1 - (2 + \frac{1}{1-n})}$ |
| Turn ratio | 4 | | 0.5 |
| Maximum conversion efficiency | 98% | 92.8% | 84.8% |
| Soft switching | Yes | No | No |

Table 2. Comparison between the proposed converter and isolated step-up converters.

| References | Proposed Paper | Reference [12] | Reference [13] |
|-------------------------------|-----------------------|------------------------|-----------------------|
| Input voltage | 48 V | 25 V | 25 V |
| Output voltage | 380 V | 400 V | 400 V |
| Output power | 500 W | 300 W | 300 W |
| Number of switches | 2 | 1 | 1 |
| Number of diodes | 2 | 4 | 4 |
| Number of inductors | 0 | 0 | 1 |
| Number of coupled inductors | 1 | 2 | 1 |
| Turn ratio | 4 | 2.9 | 3.8 |
| Voltage gain | $\frac{n}{1-D}$ | $\frac{2n(1+D)}{1-2D}$ | $\frac{n(1+D)}{1-2D}$ |
| Voltage stress on switch | $\frac{1}{1-D}V_{in}$ | $\frac{V_o}{2n(1+D)}$ | $\frac{V_o}{n(1+D)}$ |
| Maximum conversion efficiency | 98% | 95.6% | 93% |
| Soft switching | Yes | No | No |

5. Experiential Results

This study used a 500-W converter to verify the theories developed. First, Tables 3 and 4 summarize the electrical specifications and parameters of the components, respectively, of the high step-up DC–DC converter developed in this study. Then, the voltage and current waveforms of each component of the implemented circuit were measured to verify its feasibility.

Table 3. Electrical specifications of the proposed converter.

| Parameter | Specification |
|----------------------------------|-------------------------|
| Input DC Voltage V _{in} | 48 V |
| Output DC Voltage V_o | 380 V |
| Maximum output power P_o | 500 W |
| Switching frequency fs | 50 kHz |
| Coupled inductors turns ratio | $N_1: N_2: N_3 = 1:1:4$ |

Table 4. Component specifications of the proposed converter.

| Component | Model | Specification |
|---|------------------------|------------------|
| <i>S</i> ₁ , <i>S</i> ₂ | IRFP4768 | 250 V/93 A |
| C_{in} | Electrolytic Capacitor | 220 μF/250 V |
| C_o | Electrolytic Capacitor | 220 μF/450 V |
| <i>C</i> ₁ , <i>C</i> ₂ | MPP Film Capacitor | 9.4 μF/250 V |
| C_m | MPP Film Capacitor | 4.7 μF/250 V |
| L_m, L_{K1}, L_{K2} | MPP Ring core | 120 μH/2 μH/4 μH |
| D_1, D_2 | BYC10-600 | 600 V/10 A |

5.1. Experimental Waveforms

Figure 6a–k presents the measurements of the waveforms of the power switch and each component when the circuit was loaded with 500 W. Figure 6a,b presents the signal waveforms of switches S_1 and S_2 , respectively. The voltage stress was approximately 100 V, and the duty cycles of power switches S_1 and S_2 were 52% and 45%, respectively. Figure 6c,d presents the waveform of the current of the power switches. Figure 6e,f shows the waveforms of primary leakage inductances i_{Lk1} and i_{Lk2} . Figure 6g,h displays the voltage and current measurements of the waveforms of power switches S_1 and S_2 . Figure 6i,j displays the measurements of the circuit effectively reduced switching loss. Figure 6k displays the input and output voltage waveforms, which indicate that the output voltage was stable at 380 V under a heavy load.

5.2. Measured Efficiency

Figure 7 displays the efficiency curve of the proposed topology operating under output power P_0 . The input voltage was 48 V, and the output voltage was 380 V. The highest conversion efficiency was approximately 98% at 200 W, and the conversion efficiency was 95.3% at full load. The proposed topology possesses high conversion efficiency.

Figures 8 and 9 presents comparisons of the conversion efficiency between the proposed topology and the topologies proposed in [10–13]. The efficiency and output power of the proposed topology were higher than those of the topologies proposed in [10–13].

Figure 6. Experimental results of proposed topology operating at a full load of 500 W. (a) V_{gs1} and V_{ds1} of S_1 . (b) V_{gs2} and V_{ds2} of S_2 . (c) V_{gs1} and i_{ds1} of S_1 . (d) V_{gs2} and i_{ds2} of S_2 . (e) V_{gs1} and i_{lk1} . (f) V_{gs1} and i_{lk2} . (g) V_{ds1} and i_{ds1} of S_1 . (h) V_{ds2} and i_{ds2} of S_1 . (i) V_{ds1} and i_{ds1} of S_1 in ZVS. (j) V_{ds2} and i_{ds2} of S_2 in ZVS. (k) Input voltage V_{in} and output voltage V_{out} .

Figure 7. Efficiency curve of the proposed topology.

Figure 8. Efficiency of the proposed topology compared with that of the topologies proposed in [10] and [11] (nonisolated).

Figure 9. Efficiency of the proposed topology compared with that of the topologies proposed in [12] and [13] (isolated).

6. Conclusions

This study developed a novel, high-efficiency, high step-up DC–DC converter on the basis of an analysis and improvement of converters proposed in the literature. The converter has the following advantages: (1) higher conversion efficiency; (2) higher voltage gain; (3) soft switching; (4) leakage inductance recovery; (5) low component voltage stress; and (6) a simple structure. The feasibility and accuracy of the proposed topology was confirmed through theoretical analysis and experiments. The experimental results revealed that the efficiency of the converter is 95.3% at a full load of 500 W, and its highest efficiency is 98% at a load of 200 W.

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