instruments

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Review

Overview of CMOS Sensors for Future Tracking Detectors

Ricardo Marco-Hernández

Instituto de Física Corpuscular (CSIC-UV), 46980 Valencia, Spain; rmarco@ific.uv.es

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Abstract: Depleted Complementary Metal-Oxide-Semiconductor (CMOS) sensors are emerging as one of the main candidate technologies for future tracking detectors in high luminosity colliders. Their capability of integrating the sensing diode into the CMOS wafer hosting the front-end electronics allows for reduced noise and higher signal sensitivity, due to the direct collection of the sensor signal by the readout electronics. They are suitable for high radiation environments due to the possibility of applying high depletion voltage and the availability of relatively high resistivity substrates. The use of a CMOS commercial fabrication process leads to their cost reduction and allows faster construction of large area detectors. In this contribution, a general perspective of the state of the art of CMOS detectors for High Energy Physics experiments is given. The main developments carried out with regard to these devices in the framework of the CERN RD50 collaboration are summarized.

Keywords: DMAPS; CMOS; radiation sensors; electronics

1. Introduction

Current large pixel detectors in High Energy Physics, such as the ones which will be part of the A Toroidal LHC (Large Hadron Collider) ApparatuS (ATLAS) Tracker Detector [1] or the Compact Muon Solenoid (CMS) Tracker Detector [2] upgrades for the High-Luminosity Large Hadron Collider (HL-LHC), mostly follow a hybrid approach. In a hybrid pixel detector the sensor and the readout electronics are independent devices connected by means of bump-bonding, as can be seen in Figure 1. This fact allows for independent development of the sensor and readout electronics technologies to cope with high radiation environments and particle rates. However, bump-bonding is a complex and expensive assembly process with a limited output rate, due to the additional processing time required because of bump deposition and flip-chipping. Moreover, the overall material budget of several layers (i.e., pixel sensor, readout chip and bumps) may limit the accuracy of the particle trajectory measurement in hybrid pixel detectors.

A promising alternative to the current hybrid approach is the so-called depleted monolithic active pixel sensors (DMAPS). These kind of detectors integrate the sensing diode and the readout electronics in the same Complementary Metal-Oxide-Semiconductor (CMOS) wafer, as shown in Figure 2. The charge is mainly collected by drift in the depleted volume created by applying a reverse bias voltage to the sensor which generates a strong electric field. The main goal is to create a depleted region in the sensor with a sufficient thickness to collect a reasonably large signal. The thickness of the depleted volume follow will be proportional to the square root of the sensor resistivity times the reverse bias voltage applied ($d \propto \sqrt{\rho V}$). For instance, for a silicon sensor with a p-substrate resistivity of 10 Ω·cm and a bias voltage of 100 V, a depletion depth of about 10 µm would be reached and the collected signal for a MIP (Minimum Ionizing Particle) would be about 700 electrons. With a p-substrate resistivity of 1 kΩ·cm and the same bias voltage, a depletion depth of about 100 µm would be reached and the collected signal for a MIP would be about 7000 electrons. Therefore, the maximum

depletion thickness will depend on the CMOS process used to manufacture the DMAP sensor, with a given p-substrate resistivity and a maximum bias voltage limit. Totally depleted sensor operation will be preferred but this will depend on the total thickness of the DMAP sensor which is usually between 70 and 300 µm.

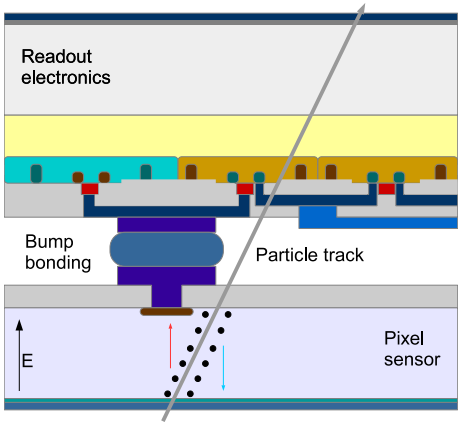

Figure 1. Diagram of a hybrid pixel detector.

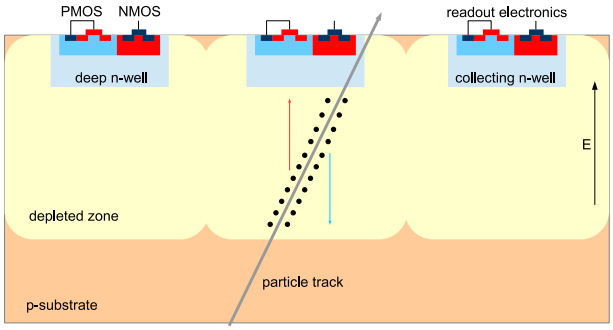

Figure 2. Diagram of a depleted Complementary Metal-Oxide-Semiconductor (CMOS) depleted monolithic active pixel sensors (DMAPS) sensor.

The pixel electronics is placed inside an isolated n-well. Electrons are collected in the n-well to have a faster charge collection. Depending on the sensor capacitance, a charge sensitive amplifier or a voltage amplifier (only for very low input capacitance) will be implemented to convert the collected charge to an equivalent voltage. The noise is proportional to the total capacitance at the input of the amplifier. Therefore, the detector capacitance is a very important parameter to keep the noise low. This sensor technology offers the possibility of noise reduction and higher signal sensitivity compared to the hybrid pixel detectors.

An important advantage of CMOS DMAPS is that their commercial CMOS fabrication process and their integration leads to an easier production, a large cost reduction and a faster fabrication. The size of DMAPS will be constrained by the wafer sizes used in the CMOS process to manufacture the sensors (standard sizes up to 200 and 300 mm can be used currently). Furthermore, this technology can save material budget due to its reduced thickness. Unfortunately, although the depleted CMOS sensor technology offers several clear advantages, there are some aspects which still have to be improved, as the radiation tolerance, the timing resolution and the readout capability to cope with high particle rates.

2. Large Versus Small Fill-Factor Structures

The two main n-on-p CMOS sensor design concepts according to their collection electrode size, known as the fill-factor, are depicted in Figures 3 and 4. In the large fill-factor structure (Figure 3)

the sensing diode is made up of the p-substrate and the deep n-well while the electronics are placed inside the charge collection well. High resistivity substrates, up to 3 kΩ·cm [3], are currently available for this structure. In the large fill-factor structure there will be on average shorter drift distances. Moreover, a high bias voltage can be applied to the device, up to 280 V [3], leading to a higher radiation tolerance capability. However, the sensor capacitance is large in this structure, up to hundreds of fF [4] depending on the pixel size, so the noise will be also large. The electronics will also have lower speed and will need more power to counterbalance this fact. Furthermore, this structure is more prone to cross talk from digital electronics into sensor.

On the other hand, the small fill-factor structure (Figure 3) is characterized by the fact that the sensor diode and the readout electronics are separated by the p-substrate. Higher resistivity substrates, up to 8 kΩ·cm [3], can be used with this structure but only low bias voltage, up to 20 V [3], can be applied to the substrate. Moreover, longer drift distances are required on average and consequently, this structure tends to a lower radiation tolerance. Nevertheless, the sensor capacitance is very small, a few fF [4], having a lower noise compared to the large fill-factor structure. Thus, the electronics implemented in the small fill-factor structure can be faster and less power-consuming. There is a fabrication method for sensors with small fill-factor structure to reduce the drift distances by using an additional low dose n-implant to ensure sensor depletion over the entire pixel area at low bias voltages [5].

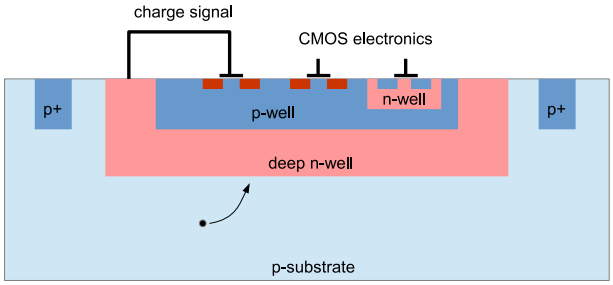

Figure 3. Diagram of a depleted CMOS DMAPS sensor with large fill-factor structure.

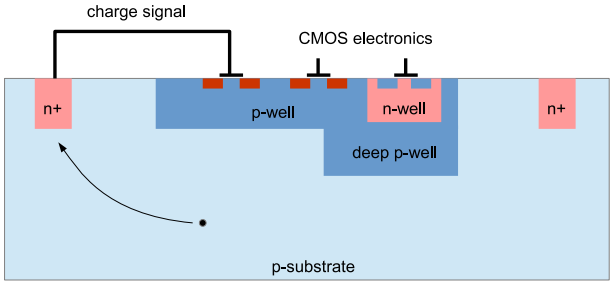

Figure 4. Diagram of a depleted CMOS DMAPS sensor with small fill-factor structure.

3. Challenges of the Depleted CMOS Sensors

As aforementioned, there are three important challenges that the depleted CMOS sensor technology has to face: the radiation hardness, the timing resolution and the data readout.

3.1. Radiation Tolerance

The first challenge is to increase the radiation hardness of this sensor technology, currently about 10^{15} 1 MeV n_{eq}/cm^2 [6], to reach the equivalent fluences expected, for instance, at the Future Circular Collider, which will be larger than $7{\cdot}10^{17}$ 1 MeV n_{eq}/cm^2 [7]. In order to meet this requirement, the CMOS sensors will need to increase the allowed substrate biasing as well as to access to higher resistivity substrates. In that sense, the effective doping concentration of the p-substrate varies with irradiation in a different way for high and low resistivities [8]: there is a increase of the depletion depth after irradiation for lower resistivities (up to equivalent fluences of about $2{\cdot}10^{15}$ 1 MeV n_{eq}/cm^2)

whereas the depletion depth decreases after irradiation for higher resistivities. This fact has to be considered in the sensor design process. The backside processing of CMOS sensors is also an important factor to increase their radiation tolerance since having a back-bias contact or thinned devices will improve their charge collection efficiency. Another relevant aspect for a better radiation hardness would be the possibility of implementing multiple nested wells in order to increase the isolation between the CMOS electronics and the substrate so that higher bias voltages could be applied to the devices. Finally, the use of CMOS technologies with smaller features sizes would also increase the radiation tolerance of the depleted CMOS sensors.

3.2. Timing Resolution

The second challenge is to improve the timing resolution of this kind of devices from the current one, lower than 10 ns [9,10], to an even better resolution, lower than 5 ns. There are different sources of time uncertainty such as the charge collection time, the delay in the readout electronics and the time-walk in the comparator. The reduction of the charge collection time is constrained by the sensor geometry and bias whereas the electronics delay improvement is limited by the readout electronics power consumption. There is more room for improvement in the reduction of the time-walk by applying new design methods for the discrimination of the analogue signals like using a time-walk compensated comparator [6], the two-threshold method or the ramp method [9].

3.3. Fast Readout

The third challenge for this technology is to be able to get a fast readout of the data to deal with high particle rates in future high luminosity colliders. For instance, a particle rate higher than 1000 MHz/cm^2 is foreseen in the inner pixel layers of the ATLAS tracker detector in the HL-LHC [1]. One of the advantages of the depleted CMOS sensor technology is the implementation of the full readout architecture in the same device to cope with detector demands, not only in terms of particle rates but also for triggering or time stamping. There are different readout architectures such as the column drain architecture implemented in the LF-Monopix device [11] or the parallel pixel to buffer architecture implemented in the ATLASPix M2 device [12]. In the former architecture, the address and time stamp is read out in each pixel and then the data are moved selectively to the chip periphery, whereas in the latter architecture the binary data of each pixel are moved immediately to the device periphery and processed there upon a trigger arrival. Another type of asynchronous readout architecture has been also implemented in the TJ-Malta device [13]. These readout architectures are being tested to optimize the integration, cross-talk and speed of the device.

4. Commercial CMOS Foundries

There is a number of commercial foundries available for the fabrication of depleted CMOS sensors. The CMOS sensors community has already a valuable experience with some of these vendors from several developments carried out. Large fill-factor structures have been produced in LFoundry Srl [14], ams AG [15] and TSI Semiconductors Corp [16], in the framework of the ATLAS upgrade and the Mu3e experiments, like the H35Demo device [17], implemented in the ams 350 nm process, the LF-Monopix device [11], implemented in the LFoundry 150 nm process, or the MuPix7 and MuPix8 devices [9], implemented in the ams and TSI 180 nm processes, to mention a few ones. Regarding the small fill-factor structures, some devices of this type have been also produced in TowerJazz Ltd. [18] following the TJ 180 nm process as the TJ-Monopix device [11] or the TJ-Malta device [13]. A special type of CMOS technology, the High Voltage Silicon On Insulator, is also available at X-FAB Semiconductor Foundries AG [19], several devices have been implemented in the XFAB 180 nm process, like the XTB01 device [20]. Finally, it must be emphasized that the current technologies available for CMOS sensors offer feature sizes larger than 130 nm, therefore the radiation tolerance and logic density of these devices can be further improved with smaller sizes in the future.

5. Summary of CMOS Activities in the Framework of the CERN RD50 Collaboration

The CERN RD50 [21] is an international collaboration with more than 300 members aimed at developing and characterizing radiation-hard semiconductor devices for high luminosity colliders. As it has been mentioned, semiconductor sensors will be exposed in the HL-LHC or FCC to hadron fluences not withstood by current LHC sensors. Among other research interests, the collaboration has a research line in new detector structures, such as n-on-p sensors, 3D sensors, low gain avalanche photodiodes and depleted CMOS sensors. The latter are a priority for RD50. In fact, several depletion depth and charge collection measurements have been already carried out with different CMOS devices [22,23]. Moreover, there is a new program within the RD50 collaboration to develop different matrices of pixels and test structures in depleted CMOS processes. This program covers different topics such as TCAD simulations, ASIC design, DAQ development and device characterization. About 36 people from 12 institutes are involved in this program. Two depleted CMOS sensor prototypes had been manufactured within the RD50 collaboration so far, the RD50-MPW1 and the RD50-MPW2, both as MPW (Multi-project Wafer) in the 150 nm LFoundry High-Voltage CMOS (HV-CMOS) process. Currently, there is a third device being designed using the same technology, the RD50-MPW3. After the RD50-MPW3 characterization, the manufacturing of a larger demonstrator, the RD50-ENGRUN1, is foreseen as an enginering run in the 150 nm LFoundry HV-CMOS process.

5.1. RD50-MPW1

The RD50-MPW1 chip [24] has a size of 5 mm by 5 mm and a total thickness of 280 µm. It was submitted in November 2017 and received in April 2014. The RD50-MPW1 was fabricated using substrates of two different resistivities, 500 Ω·cm and 1.9 kΩ·cm. The main goals of this design were to test the technology used and verify the validity of novel designs. Figure 5 shows a diagram of the RD50-MPW1 pixel cross-section, where it can be seen that the device has a large fill-factor structure. The RD50-MPW1 device has test structures for I-V and Edge-Transient Current Technique (E-TCT) measurements and two independent CMOS pixels matrices. One is a photon counting matrix with 28 by 52 pixels with embedded readout electronics, charge amplifier and discriminator, and a 16-bit counter. The other matrix has 40 by 78 pixels, with a size of 50 µm by 50 µm, with embedded readout electronics following a column drain readout architecture similar to the FEI3 readout chip [25].

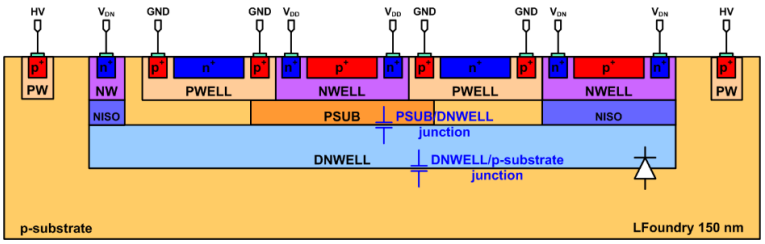

Figure 5. Diagram of the RD50-MPW1 depleted CMOS sensor pixel cross-section.

Concerning the RD50-MPW1 characterization, the leakage current and the breakdown voltage were measured in the pixels of the test structures. E-TCT measurements were also carried out using the test structures. A specific DAQ was developed in order to characterize both active CMOS pixel matrices [26]. The sensors are fully functional but the measured leakage current was found higher than expected [24,27]. Crosstalk was also detected in some digital readout lines from pixels of the matrix with column drain readout architecture [28,29].

5.2. RD50-MPW2

A second device, the RD50-MPW2 [30], was designed to test new design approaches to minimize the leakage current by preventing certain filling layers added by the foundry and adding a series of guard rings [31]. A new pixel readout electronics design was also implemented to improve the

speed of the readout electronics [32,33]. This is a smaller device, with a size of about 3 mm by 2 mm and a thickness of 280 µm. It was submitted for fabrication in January 2019 and received in February 2020. Different substrate resistivities have been used, 10 Ω·cm, 0.5–1.1 kΩ·cm, 1.9 kΩ·cm and between 2 and 3 kΩ·cm. The RD50-MPW2 floorplan can be seen in Figure 6. It consists of I-V and E-TCT test structures, an 8 by 8 pixel matrix of 60 µm by 60 µm pixels with analogue embedded readout, a bandgap voltage reference and a Single Event Upset (SEU) tolerant array.

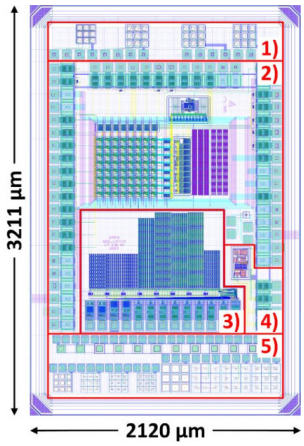

Figure 6. Floorplan of the RD50-MPW2 depleted CMOS sensor with its main blocks highlighted: I-V and E-TCT test structures (1 and 5), 8 by 8 pixel matrix (2), SEU tolerant arrray (3) and bandgap voltage reference (4).

The RD50-MPW2 characterization is still ongoing. The DAQ used to interface the RD50-MPW1 has been updated for this device [34]. Preliminary results show a drastic reduction of about six orders of magnitude of the RD50-MPW2 pixel leakage current, $\mathcal{O}$(100 pA), with respect to the RD50-MPW1 [35], $\mathcal{O}$(100 µA). They also show the correct operation of the pixel matrix [36].

5.3. RD50-MPW3 and RD50-ENGRUN1

A third depleted CMOS sensor prototype, the RD50-MPW3, is currently being designed within the RD50 collaboration. It will be manufactured in the second quarter of 2021 as a MPW in the 150 nm LFoundry HV-CMOS process. This device will have a size of 5 mm by 5 mm and a thickness of 280 µm. It will be manufactured using several substrates of different resistivities. The device will consist of few test structures for I-V and E-TCT measurements and, at least, a matrix of 40 by 78 CMOS pixels with column drain readout architecture. The pixels of this matrix will have the same design and embedded readout as the ones implemented in the RD50-MPW2 device. The matrix column layout is modified with respect to the RD50-MPW1 in order to avoid the crosstalk in some of the digital readout lines. The column drain readout architecture is also improved to optimize the data transmission.

The final objective of the RD50 collaboration depleted CMOS development program is the design of a large area demonstrator in the same technology, the so-called RD50-ENGRUN1 device. A diagram of the main blocks of the RD50-ENGRUN1 device can be seen in Figure 7. This device will consist of several independent depleted CMOS pixel matrices and test structures. The pixel matrices have different purposes and the main goals pursued in this design are the improvement of the current time resolution with dedicated readout circuits, the implementation of new sensor cross-sections, the assessment of pre-stitching options to increase the device size beyond the reticle size limitation and the increase of radiation tolerance by sensor design and backside processing.

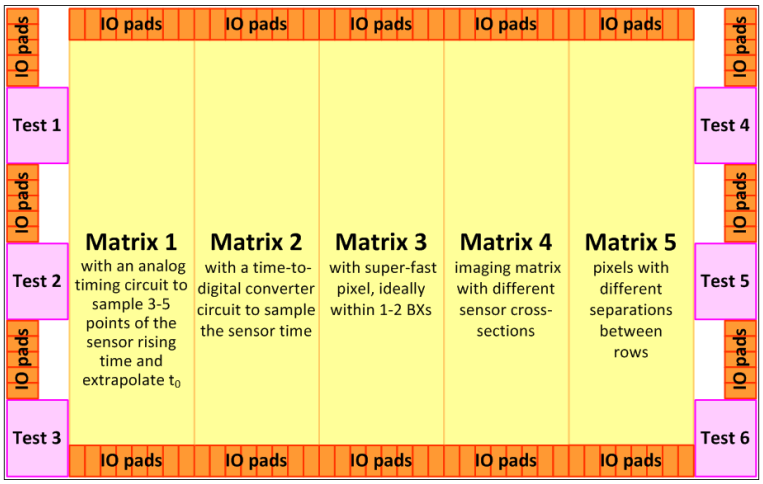

Figure 7. Diagram of the RD50-ENGRUN1 device main blocks.

6. Conclusions

It has been pointed out that the depleted CMOS sensor technology is very promising for future silicon tracking detectors due to its lower cost, easier and faster detector assembly, faster fabrication turn-around and larger material budget saving. However, some challenges must still be faced to cope with future tracking detectors requirements in terms of radiation hardness, timing resolution and data readout. This sensor technology is a priority for the CERN RD50 collaboration, which has been involved in the radiation tolerance study of depleted CMOS sensors. Within the CERN RD50 collaboration, a project to develop depleted CMOS sensors is being carried out. Two devices, the RD50-MPW1 and RD50-MPW2 have been already manufactured as MPW in the 150 nm LFoundry HV-CMOS process to test the technology and verify the validity of novel designs. The high leakage current of the RD50-MPW1 pixel, $\mathcal{O}$(100 µA), has been drastically reduced in the RD50-MPW2 device to $\mathcal{O}$(100 pA). The RD50-MPW2 includes faster pixel embedded readout electronics which is fully functional. A new RD50-MPW3 device is currently being designed with an improved matrix layout and optimized data transmission. The final goal is to apply the expertise gained with this technology to a larger RD50-ENGRUN1 device demonstrator with several matrices of pixels with the main objective of improving the timing resolution.

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Conflicts of Interest: The authors declare no conflict of interest.

Abbreviations

The following abbreviations are used in this manuscript:

CMOS	Complementary Metal-Oxide-Semiconductor
ATLAS	A Toroidal LHC ApparatuS
CMS	Compact Muon Solenoid
HL-LHC	High Luminosity Large Hadron Collider
DMAPS	Depleted Monolithic Active Pixel Sensors
CERN	Conseil Européen pour la Recherche Nucléaire
MPW	Multi-Project Wafer

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