

Miniaturized On-Chip NFC Antenna versus Screen-Printed Antenna for the Flexible Disposable Sensor Strips

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Abstract: With the ongoing trend toward miniaturization via system-on-chip (SoC), both radio-frequency (RF) SoCs and on-chip multi-sensory systems are gaining significance. This paper compares the inductance of a miniaturized on-chip near field communication (NFC) antenna versus the conventional screen-printed on-substrate ones that have been used for the transfer of sensory data from a chip to a cell phone reader. Furthermore, the transferred power efficiency in a coupled NFC system is calculated for various chip coil geometries and the results are compared. The proposed NFC antenna was fabricated via a lithography process for an application-specific integrated circuit (ASIC) chip. The chip had a small area of $2.4 \times 2.4 \text{ mm}^2$, therefore a miniaturized NFC antenna was designed, whereas the screen-printed on-substrate antennas had an area of $35 \times 51 \text{ mm}^2$. This paper investigates the effects of different parameters such as conductor thickness and materials, double layering, and employing ferrite layers with different thicknesses on the performance of the on-chip antennas using full-wave simulations. The presence of a ferrite layer to increase the inductance of the antenna and mitigate the interactions with backplates has proven useful. The best performance was obtained via double-layering of the coils, which was similar to on-substrate antennas, while a size reduction of 99.68% was gained. Consequently, the coupling factors and maximum achievable power transmission efficiency of the on-chip antenna and on-substrate antenna were studied and compared.

Keywords: NFC antenna; ferrite; on-chip antenna; internet of things

1. Introduction

The prospect of diagnostic point-of-care devices is to minimize their foot-print to a few square centimeters and to reduce their production cost to be affordable for end-users. The lab-on-chip (LOC) concept, by which several laboratory functions can be integrated into a chip, has already been adapted as a promising approach. In order to further minimize the size of smart devices, the radio-frequency antenna which occupies a large part of diagnostic kits can also be integrated into the complementary metal-oxide-semiconductor (CMOS) chip, as manifested in Figure 1. As seen, a typical intelligent sensor strip, which is often designed for one-time use, consists of a sensing area (e.g., ion-selective electrodes), an NFC powered application-specific integrated circuit (ASIC) chip and an antenna for communication. By integrating the antenna and sensing area into the chip, the substrate could even be completely omitted and the size of the NFC tag would be reduced to the size of the chip.

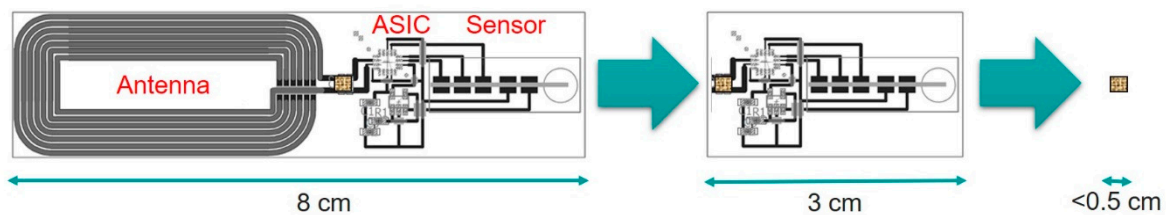


Figure 1. The trend towards miniaturization of point-of-care devices by integrating radio-frequency (RF) antenna and sensing area into the complementary metal-oxide-semiconductor (CMOS) chip.

Near field communication (NFC) antennas operate in the near field by coupling the magnetic field of a reader, such as a mobile phone, to the target. Ordinarily, the NFC antenna is a multi-turn loop of conductors connected to a capacitor that resonates at 13.56 MHz [1]. The use of NFC in medical applications such as blood potassium level measurement has been reported in [2]. In this work, the potassium level in the blood sample is measured via a chip integrated to the NFC antenna and is reported to the reader. For this purpose, a booster antenna is usually required for better detection of the small tag as well as increasing the reading distance [3]. The size of the NFC antenna is limited in most medical applications and will benefit from miniaturization due to lower price and convenience of usage [4]. In the conventional manufacturing of the NFC antenna, printing technology is the main fabrication method that is implemented, where conductive ink is printed on the substrate in a form of antenna pattern through printing equipment.

In this study, we have designed a small on-chip NFC antenna that can be integrated with the measuring chip. The size of the NFC antenna is indeed a critical parameter due to the maximum inductance that can be achieved in a limited area. In order to achieve the required inductance, a ferrite layer can be used under the loop. Ferrimagnetic materials or ferrites have higher resistivity and significant permeability [5]. Here the benefit of using the ferrite layer is twofold; first, the inductance of the loop will be increased due to the high permeability of the ferrite and second, the effect of the metal backplate will be mitigated [6]. The use of ferrites has been popular as the NFC antenna interacts with the metal backplate which is present in most mobile devices [7–9]. The ferrite attracts the vast majority of the magnetic field lines and thus gets rid of any unwanted eddy currents in the surrounding metal plates. Furthermore, a double layer chip coil design is presented and compared to the single-layer ferrite coil design in terms of power efficiency when coupled to a reader antenna. All kinds of coil designs are then compared as suitable improvements of standard on-chip coils.

The paper includes electromagnetic field simulations of the NFC antenna in the presence and without the ferrite layer. The conductivity of the ferrite is investigated due to sensitivity to the fabrication process [10]. The fabricated on-chip antenna and printed on-substrate antenna were characterized and compared with the simulation results.

2. Methods

In this paper, we have studied NFC antennas in four generations, as follows;

- On-chip antenna (fabricated and simulated)
- On-chip antenna with ferrite layer (simulated)
- On-substrate screen-printed Ag antenna on paper (fabricated and simulated)
- On-substrate Cu-etched antenna on PCB (fabricated and simulated)

Concerning on-chip antennas, since a limited area only (2.4×2.4 mm) was available, a miniaturized design for the NFC antenna was made in which the whole available area was covered by the antenna. The designed on-chip antenna, as shown in Figure 2, is an 8 μ m thick copper spiral loop on a 500 μ m thick silicon substrate. The substrate is insulated from the loop via a 0.5 μ m thick silicon-nitride layer. The dimensions are listed in Table 1. A high-frequency structure simulator (HFSS V.19.5), Ansys Corp., has been used for the full-wave analysis of the structures to calculate the electromagnetic fields and

impedances via port excitation. For simulating the structure, an airbox with radiating boundary condition has been used and the frequency of operation is set to 13.56 MHz.

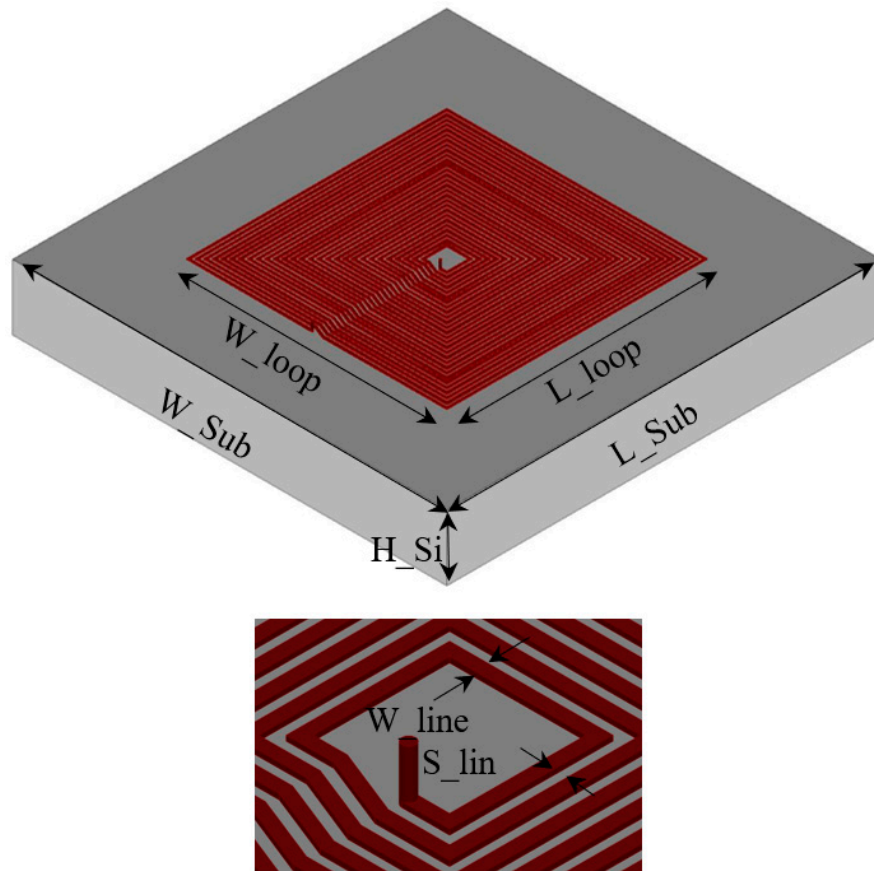


Figure 2. Near field communication (NFC) loop designed in a high-frequency structure simulator (HFSS).

Table 1. Design parameters of the simulated NFC antenna.

W_Sub	L_Sub	W_Loop	L_Loop	W_Line	S_Line	H_Si	H_SiNi	H_Copper
4 mm	4 mm	2.4 mm	2.4 mm	20 μ m	20 μ m	600 μ m	500 nm	8 μ m

For the sake of comparison, a printed NFC antenna was also fabricated using a screen-printing method. Uncoated paper sheets (Mondi AG) with a grammage of 120 g/m², a porosity of 50 mL/min, a thickness of 100 μ m and surface roughness of 1.2 μ m (Ra) were screen printed with Ag paste (Dupont 5029) and dried at 90 °C in an oven [11]. Moreover, as a benchmark, a similar antenna design was also realized by using the printed circuit board (PCB) technology. Here Cu tracks with a thickness of 35 μ m were used, whereas in screen-printed paper, Ag tracks with a thickness of 10 μ m were made.

A Keysight E4990A impedance analyzer with a frequency range from 20 Hz to 120 MHz was used to characterize the various NFC coils. The serial resistance R_s and inductance L_s of the NFC coils were measured at the NFC frequency of 13.56 MHz. The NFC antenna samples on the printed circuit boards were connected to the impedance analyzer through soldered wires. On the printed NFC coils, the contact was done using spring-loaded connectors directly on the traces. To minimize the effects of the connections, open-circuit and short-circuit calibration was done for all connections before measuring. The coil-on-chip antennas on the wafer were tested using the manual electric probe station PM5 from SÜSS MicroTec. The wafer was held on the chuck of the probe station using a vacuum, while the probes are manually positioned and lowered on to the pads of the coils through

the microscope. Again, the Keysight E4990A was used for the electrical measurements with the probe station.

3. Results and Discussion

3.1. The Performance of On-Chip NFC Antenna

The real and imaginary parts of simulated input impedance are used to report the resistance and effective inductance of the NFC loop. Here, the resistance of the antenna with an 8 μm Cu conductor loop was 15.76 Ω with 0.922 μH inductance. In order to make the NFC loop resonant, a 100 pF capacitor was used in parallel to the loop terminals. The input impedance of the structure, seen in Figure 3a, shows the parallel resonant behavior around 15 MHz. The quality factor for a parallel resonant circuit can be calculated by using the values for resistance, R_L , and inductance, L , using (1). For the proposed structure it will be about 5.

$$Q = X_L/R_L, \quad (1)$$

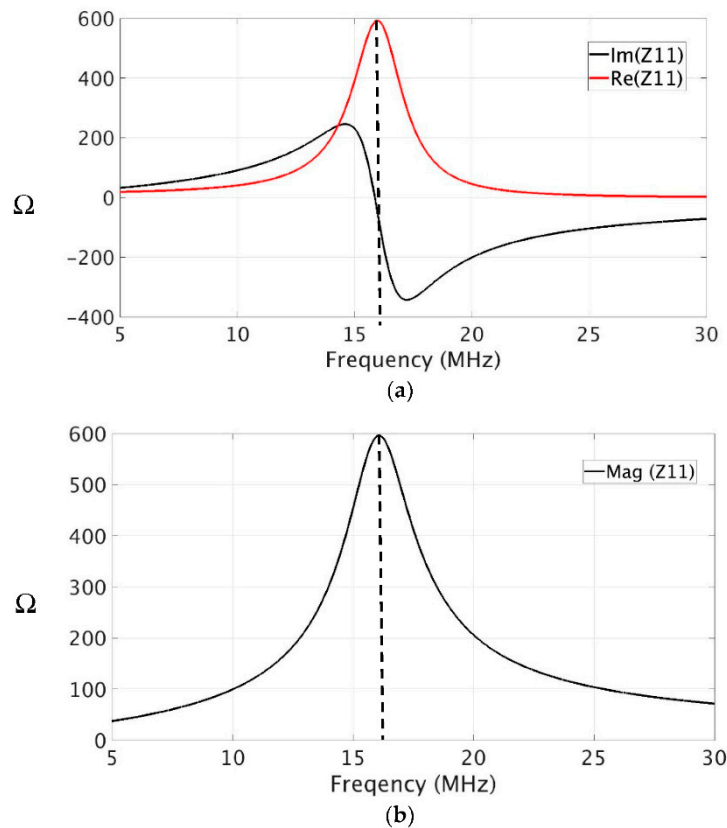


Figure 3. (a) Real and imaginary parts of the input impedance in ohms and (b) magnitude of the input impedance. The dashed line indicates the resonance.

3.2. The Effect of Conductor Materials and Thicknesses

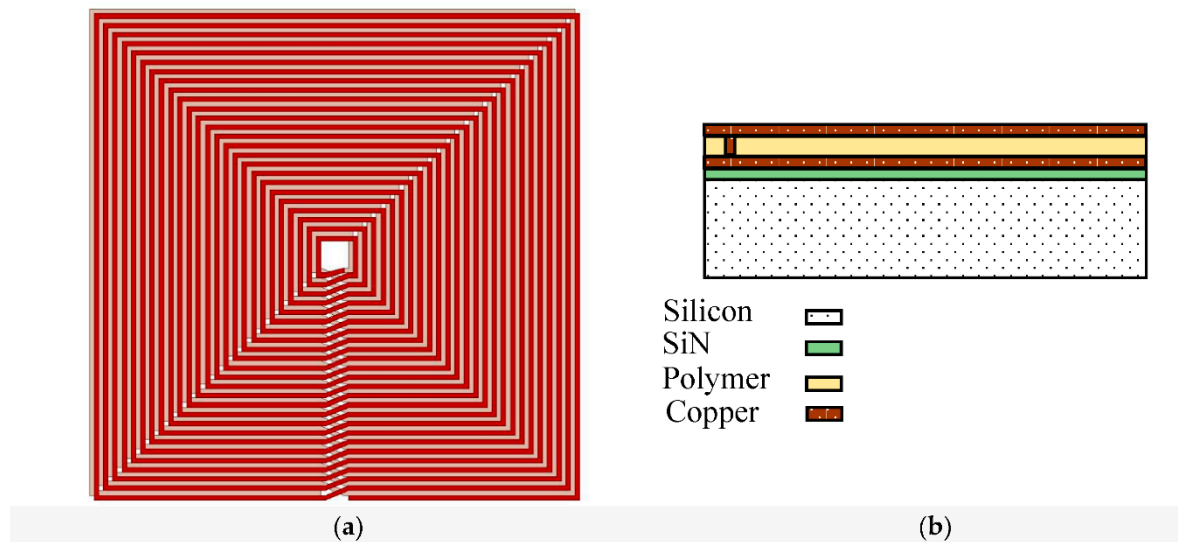
The effect of conductor type as well as the conductor thickness have been investigated by simulating copper and aluminum conductors with different thicknesses for the NFC loop and comparing the effective inductance and resistance. Shown in Table 2, it has been found that due to better conductivity of copper it presents lower resistance with similar inductance values. On the other hand, using a very thin conductor, e.g., 1 μm thick copper, significantly increases the resistance as expected. The optimal value for the thickness can be around 5–10 μm for minimal resistance.

Table 2. Comparison between different conductors and thickness.

	R (Ω)	L (μ H)
Aluminum 1 μ m	163	0.790
Aluminum 5 μ m	33	0.821
Aluminum 10 μ m	16.8	0.815
Copper 1 μ m	107	0.809

3.3. The Effect of Double-Layering

As the area of the NFC loop is very small (2.4×2.4 mm), the inductance that can be reached is limited. In order to increase the inductance, one way would be to use a second layer and extend the loop to the next layer, shown in Figure 4a. Here, a two-layer NFC loop has been simulated over the available area (2.4×2.4 mm). The next layer of conductor is separated from the first layer using a dielectric polymer layer with a dielectric constant of 4, as shown in Figure 4b.

**Figure 4.** Two layer NFC loop configuration (a) top view, (b) side view.

The simulation of the two-layer configuration with a Cu thickness of 8 μ m in each layer promised a superior inductance of 2.86 μ H and $R = 32.3 \Omega$.

3.4. Investigating the Effects of Ferrite

Using the ferrite layer under the NFC conductor is another method to miniaturize the structure. Ferrites have high permeability and as a result, increase the inductance of the NFC loop. In order to investigate the effects of ferrite, a 1 μ m thick ferrite layer between the NFC loop and the Si-Ni layer is inserted for a one-layer NFC loop that covers the whole area under the loop and extends to the silicon edges. The ferrite layer is chosen from the HFSS library with electromagnetic properties of (relative permeability) $\mu_r = 1000$ and (conductivity) $\sigma = 0.01$ S/m. As can be seen from Figure 5, the magnetic fields are more concentrated towards the ferrite layer as a result of high magnetic permeability.

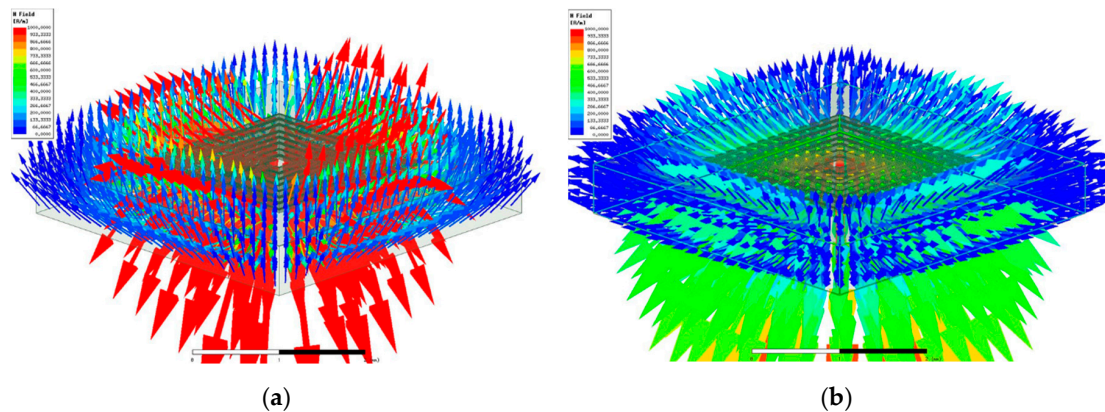


Figure 5. Magnetic field lines (a) without the ferrite layer (b) with the ferrite layer on a scale 0–1000 A/m.

The input impedance of the NFC loop in presence of the ferrite layer shows the increase of the inductance although the resistance increases slightly due to ferrite conductivity. Table 3 shows a comparison between cases with and without the ferrite layer. It is found that using this ferrite layer, the inductance has been increased by 1.54 times while the increase in resistance is marginal. Hence the NFC antenna in presence of the ferrite has been significantly miniaturized.

Table 3. Comparison between cases with and without ferrite.

	R (Ω)	L (μ H)
Without ferrite	15.7	0.922
1 μ m thick ferrite ($\sigma = 0.01$ S/m)	17.8	1.420
1 μ m thick ferrite ($\sigma = 0.1$ S/m)	19.5	1.414
10 μ m thick ferrite ($\sigma = 0.01$ S/m)	18.1	1.748

It must be mentioned that ferrite layers are very sensitive to the fabrication process and hence will show different electrical properties [12,13]. In order to investigate the effect of the ferrite conductivity, ferrites of different conductivities and its effects on losses are compared here. The loss mechanism in the current structure is a result of eddy currents induced in the silicon substrate, ferrite ohmic loss as well as the resistivity of the loop itself. It has been found, as shown in Table 3, that the effect of ferrite loss seems trivial compared to other loss sources such as conductors' resistance.

As expected, increasing the thickness of the ferrite will enhance the inductance further with a slight increase in resistivity.

3.5. On-Substrate Antennas

The fabricated test strips with the on-substrate NFC antenna are shown in Figure 6. The 6 turn NFC antenna occupied an area of 35×51 mm. The line width and spacing are 1 mm and 0.5 mm respectively. The PCB and paper substrates had a dielectric constant of 4 and 3.7, respectively. The measured inductance and resistance of the NFC antenna on both PCB and paper substrates were in good agreement to the simulated values which are shown in Table 4. The simulated values for the on-PCB antenna were 2.12 μ H inductance and resistance was 1.4 Ω , whereas for the on-paper antenna the values were 2.17 μ H and 20.34 Ω respectively.

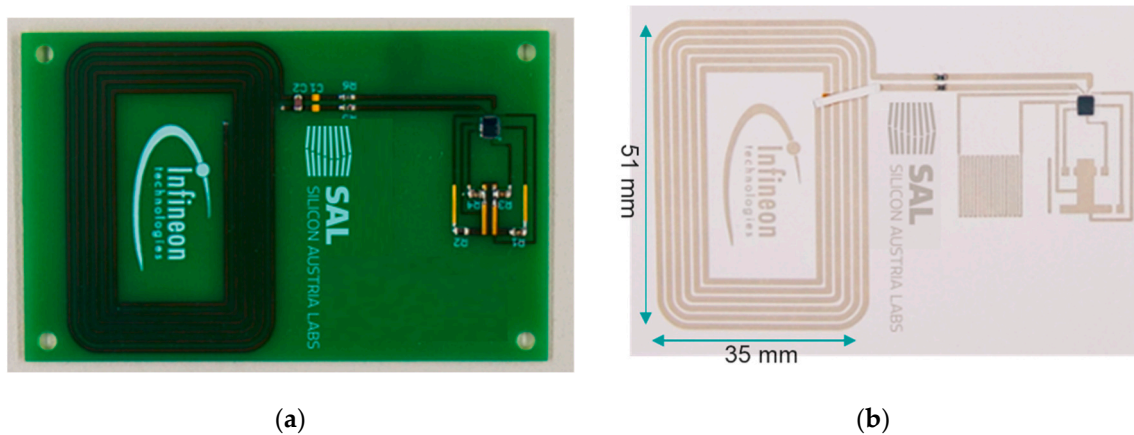


Figure 6. On-substrate antenna: 6-turn NFC antenna on printed circuit board (PCB) (a) and on screen-printed paper substrate (b).

Table 4. The properties of on-substrate NFC antennas.

	R (Ω)	L (μ H)
PCB (etched Cu antenna with the thickness of 35 μ m)	1.09	2.108
E-paper (screen-printed Ag antenna with a thickness of 10 μ m)	35	1.681

The performance of printed radio-frequency identification (RFID) antennas is highly dependent on the electrical conductivity of the conducting tracks forming the antennas. As a result, lower conductance and inductance were observed in the screen-printed NFC antenna compared to the Cu tracks on the PCB. The magnetic field lines of the screen-printed NFC antenna are also presented in Figure 7.

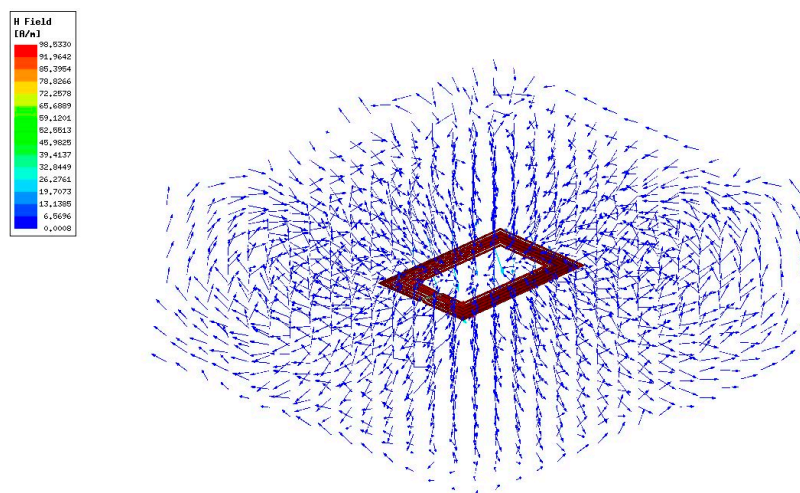


Figure 7. Magnetic field lines of the screen-printed Ag antenna in a scale 0–1000 A/m.

3.6. Coupling of Antennas

A different viewpoint for performance assessment is the transferred power efficiency between the antennas in the study and a reader antenna. To assess the potential for coupling the chip antenna to a standard-sized reader antenna, several assumptions have been made. Firstly, since every smartphone is different in its geometry internally, there does not exist a standardized reader antenna. We therefore compared antennas from several smartphones and came up with a reader antenna geometry that resembles the actual antennas as closely as possible. We assumed the size to be about $4 \times 4 \text{ cm}^2$, with 5 Planar turns and a ferrite sheet thickness of about 0.5 mm. This coil is then coupled to the

various antennas under investigation. Solid metrics for power efficiency are the coupling factor, as well as the total quality factors, which are calculated from the Z-parameters that are related to the port S-parameters. The coupling factor as well as the quality factors are defined as [14] respectively,

$$k = \sqrt{\frac{\text{Im}(Z_{12}) \cdot \text{Im}(Z_{21})}{\text{Im}(Z_{11}) \cdot \text{Im}(Z_{22})}} \quad (2)$$

$$Q_1 = \frac{\text{Im}(Z_{11})}{\text{Re}(Z_{11})} \quad (3)$$

$$Q_2 = \frac{\text{Im}(Z_{22})}{\text{Re}(Z_{22})} \quad (4)$$

where port 1 is defined at the reader side and port 2 at the chip side and $Z_{ij} = Z_{ji}$ for $i \neq j$, as this is a passive, and therefore reciprocal device. It should be noted that $\text{Re}(Z_{ii})$ includes all losses of the coil with port i, including the ohmic conductor losses and the eddy current losses inside the ferrite due to finite conductivity as well as dielectric losses, if applicable. $\text{Im}(Z_{ii})$ on the other hand includes inductive and capacitive contributions of the respective geometry, all at 13.56 MHz.

The maximum achievable efficiency of the transmission, assuming perfect power matching, can then be calculated from these quantities as [15]

$$\eta_{\max} = \frac{\chi}{(1 + \sqrt{1 + \chi})^2}, \quad (5)$$

where

$$\chi = k^2 Q_1 Q_2. \quad (6)$$

The results for the coupling factors and maximum achievable power transmission efficiency are shown in Table 5.

Table 5. Calculated coupling factors and efficiencies for different tag coil geometries at 5 mm distance.

Tag Coil Geometry	k [1]	η_{\max} [%]
Paper coil with silver conductor (Figure 6b)	0.53	78.6
Two-layer on-chip coil (Figure 4)	0.013	0.651
Single-layer on-chip coil	0.015	0.617
Single-layer on-chip coil with 1 μm ferrite	0.012	0.571

It shows that the large paper coil provides sufficiently high efficiency. The overall limit is the minimum threshold power of 4 mW that has to be transferred into the NFC chip to operate it, which can be achieved for large distances. However, this result is to be expected since reader and tag coil are of similar dimension. The two-layer chip coil on the other hand would need at least 614 mW of reader power to operate the tag chip. This, of course, infers the best possible power matching. Since the NFC chip also provides an on-chip matching capacitor, which is comparably small due to the chip size, the matching is far away from being perfect. The actual resonance is significantly above the 13.56 MHz. If no external additional matching capacitor can be used, then the fact that the self inductance of the tag chip coil is increased due to the inclusion of a second layer or a ferrite sheet helps the matching to perform better. Simulations with Keysight ADS using standard NFC matching circuitry, pictured in Figure 8, and the S-parameters from the HFSS simulations, showed improvement in the overall efficiency, but the improvements are still not high enough to directly couple the chip coil with a reader without the need of a booster antenna [3], and are of course below the optimal limit. As indicated above, the optimal efficiency limit at a coil distance of 5 mm is 0.65% for the dual-layer coil, that was

almost reached for optimized matching elements (0.6%). If the on-chip 78 pF capacitor is used for this configuration, the efficiency drops to about 0.12% for the dual-layer chip coil, while the single-layer chip coil and the 1 μm ferrite chip coil will drop to 0.11% and 0.16%, respectively. These results are presented in Table 6.

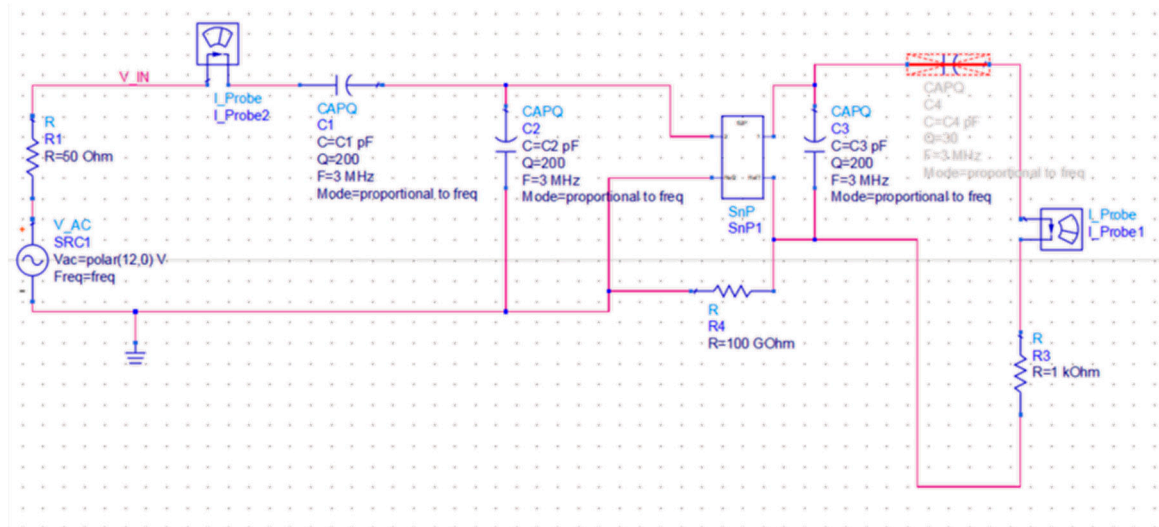


Figure 8. Matching the coupled-coils system for optimum power efficiency at 13.56 MHz.

Table 6. Effective power efficiency of different chip coil geometries using the on-chip matching capacitor at 5 mm distance.

Tag Coil Geometry	$\eta_{\text{effective}}$ [%]
Single-layer on-chip coil	0.11
Single-layer on-chip coil with 1 μm ferrite layer	0.16
Two-layer on-chip coil	0.12

As can be seen, the inductance of the dual-layer coil is already high enough (2.86 μH) that the on-chip matching capacitor becomes larger than the optimum value (78 vs. 48 pF) and therefore detunes the resonance in a different direction. This leads to worse performance compared to the single-layer chip coil with 1 μm ferrite, where the on-chip capacitor value comes closest to the optimum value (78 vs. 99.8 pF).

In terms of raw electrical performance, the ferrite coil should therefore be preferred over the double-layer coil if only on-chip matching can be applied. If different matching possibilities are available, then the double-layer coil outperforms the single-layer coil with ferrite by a small margin. From a manufacturing point of view, sputtering ferrite on the chip is more feasible than the addition of a second layer. Therefore, the ferrite approach appears to be more cost effective and less prone to low yield, while being the best performer using on-chip matching, and should be preferred. The easiest and cheapest version is the single-layer coil, but with the lowest power efficiency. In general, Equation (6) can be expressed in terms of electrical circuit parameters and results in

$$\chi = \frac{\omega^2 \cdot M^2}{R_1 \cdot R_2}, \quad (7)$$

where ω is the angular frequency, M is the mutual inductance ($\text{Im}(Z_{ij})/\omega$) between the reader and the tag coil and R_1 and R_2 are the respective ohmic losses of the coils. Since the maximum achievable power efficiency grows monotonously with χ , an optimization of χ automatically optimizes also the power efficiency.

4. Conclusions

These results prove the possibility of miniaturizing the NFC antenna by 99.68% by using an on-chip antenna approach. By comparing different effective parameters on the fabrication of the on-chip antenna, it was revealed that the two-layer conductor configuration can provide the best performance, while a superior inductance of 2.86 μH and resistance of 32.3 Ω could be obtained. These values are comparable to those of on-substrate antennas, where an inductance of 1.68 μH and resistance of 35 Ω were achieved. The subsequent analysis of the transferred power efficiency revealed that the maximum coupling efficiency of the on-chip two-layer antenna to the large standard-sized reader antenna is still significantly lower than that of the on-substrate antenna. The lower coupling efficiency of the on-chip antenna can be circumvented either by using a tailored smaller reader antenna or by implementing a booster antenna. If the on-chip matching capacitor is used, the chip coil with a 1 μm ferrite sheet seems the best solution, as its inductance comes closest to the ideal matching value. Therefore the transferred power efficiency is highest in this case, even better than that of the double-layer coil. Therefore, depending on the available matching capacitors, either the ferrite single-layer coil or the double-layer coil should be used for optimum operation in an NFC environment.

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