



## Article

# Impact of the Ferroelectric Stack Lamination in Si Doped Hafnium Oxide (HSO) and Hafnium Zirconium Oxide (HZO) Based FeFETs: Toward High-Density Multi-Level Cell and Synaptic Storage

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**Abstract:** A multi-level cell (MLC) operation as a 1–3 bit/cell of the FeFET emerging memory is reported by utilizing optimized Si doped hafnium oxide (HSO) and hafnium zirconium oxide (HZO) based on ferroelectric laminates. An alumina interlayer was used to achieve the thickness independent of the HSO and HZO-based stack with optimal ferroelectric properties. Various split thicknesses of the HSO and HZO were explored with lamination to increase the FeFET maximum memory window (MW) for a practical MLC operation. A higher MW occurred as the ferroelectric stack thickness increased with lamination. The maximum MW (3.5 V) was obtained for the HZO-based laminate; the FeFETs demonstrated a switching speed (300 ns), 10 years MLC retention, and  $10^4$  MLC endurance. The transition from instant switching to increased MLC levels was realized by ferroelectric lamination. This indicated an increased film granularity and a reduced variability through the interruption of ferroelectric columnar grains. The 2–3 bit/cell MLC levels and maximum MW were studied in terms of the size-dependent variability to indicate the impact of the ferroelectric area scaling. The impact of an alumina interlayer on the ferroelectric phase is outlined for HSO in comparison to the HZO material. For the same ferroelectric stack thickness with lamination, a lower maximum MW, and a pronounced wakeup effect was observed in HSO laminate compared to the HZO laminate. Both wakeup effect and charge trapping were studied in the context of an MLC operation. The merits of ferroelectric stack lamination are considered for an optimal FeFET-based synaptic device operation. The impact of the pulsing scheme was studied to modulate the FeFET current to mimic the synaptic weight update in long-term synaptic potentiation/depression.

**Keywords:** ferroelectric; hafnium oxide; laminate; FeFET; synaptic device

## 1. Introduction

Since the introduction of the computing architecture by Von-Neumann, the architecture bandwidth limitation causes a performance bottleneck due to the latency in the data shuttling between the main memory and the processor [1]. Through the long development of the computing architecture, this performance bottleneck was managed through hierarchical architecture of the memory storage. However, due to the different scaling goals between the processor and main memory, i.e., processor speed versus memory capacity, the processor and the main memory performance encountered over the years an accumulating gap [2]. The continuous increase in the processor speed is challenged by an incomparable shortening of the memory access time; this leads to an increased frequency of the local cache miss. This is further exacerbated due to the known scaling challenges for the nearest in the hierarchy to the processor yet volatile static random access memory (SRAM) and dynamic random access memory (DRAM) concepts. To reduce the cache miss, the increased capacity of the SRAM and DRAM storage is reduced due to the increased fraction of the utilized chip area. Today, the technological solutions for the Von-Neumann bottleneck cover broad concepts such as embedded nonvolatile memories [3], logic in-memory computing [4], or an alternative brain-inspired computing [5,6].

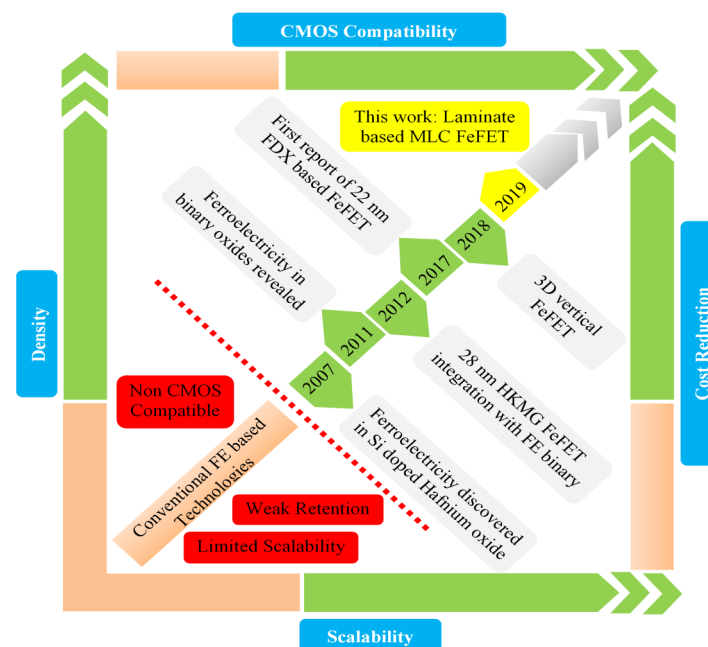
The discovery of ferroelectricity in the fluorite structure-based hafnium oxide materials [7,8] marked a change in FeFET technology development. It was promoted as an ideal low-cost embedded memory solution [9]. On a system level, the FeFET offers several merits as a low power operation: a fast-switching speed and a short access time. Furthermore, the pronounced ferroelectric properties for an ultra-thin film of hafnium oxide while using conformal deposition techniques enable highly scalable planar or vertical FeFETs [10,11]. In contrast, the conventional perovskite-based ferroelectric materials such as the strontium bismuth tantalate (SBT) or lead zirconium titanate (PZT) remained a challenge for high volume FeFET production due to the incompatibility of the CMOS material, limited scalability, and essentially the weak retention reliability [12]. Thereby, the key technological merits highlighted in Figure 1 such as non-volatility, density, speed, and cost at superior performance over the Flash memory are the key drivers for the CMOS-compatible fluorite structure-based FeFET memory development.

The multi-level cell (MLC) operation to increase the potential FeFET density beyond the single-level cell (SLC) is dependent on the achieved maximum of the memory window (MW) size. The MLC describes a memory cell with the capacity for storage beyond a single bit storage, i.e., beyond the single-level cell. For the MLC operation, multi-levels are required for storage. Typically, these storage levels are represented by the current readout; the increase in the maximum MW size enables a reliable distinction between the current levels to be made. In turn, the maximum MW requirement increases beyond the SLC as the MLC bit/cell capacity increases. To achieve a reliable separation margin between the levels, unlike the flash memory concept, a FeFET maximum MW is governed by the fundamental stack physics outlined in Equation (1) of the ferroelectric film thickness and properties [13]. At first glance, a higher MW, and thus the capacity of stored levels, becomes viable by increasing the ferroelectric film thickness. However, the optimal ferroelectric properties in the fluorite structure-based ferroelectrics are limited to a range of ferroelectric thin film thicknesses due to the thickness-dependent changes in film stress. An increase in the ferroelectric film thickness can induce a lower surface to volume ratio; this renders the stress effects of the metal electrodes less pronounced and thus provokes a monoclinic phase stabilization. In contrast, a decrease in the ferroelectric film thickness results in a higher film stress and tends to stabilize the tetragonal phase. The deviation from an optimal ferroelectric orthorhombic phase by a higher fraction of either the monoclinic or the tetragonal phase causes a lower ferroelectric remnant polarization ( $P_r$ ). In Equation (1), a lower  $P_r$  below a critical threshold value can cause a strong decrease in the practical maximum MW size [14]. Equation (1) shows the memory window dependence on the ferroelectric film properties such as, the coercive field ( $E_c$ ), the ferroelectric layer thickness ( $d_F$ ), the ferroelectric layer permittivity ( $\epsilon_F$ ), and the remanent/saturated polarization

( $P_r/P_s$ ). Essentially, the decrease in the ferroelectric  $P_r$  poses a challenge for achieving an MW increase upon a higher ferroelectric film thickness.

$$MW \approx 2E_c \cdot d_F \left[ 1 - \frac{2E_c \cdot \epsilon_F \cdot \epsilon_o}{P_s \cdot \ln\left(\frac{1+P_r/P_s}{1-P_r/P_s}\right)} \right] \quad (1)$$

One aim of this work was to stabilize the optimal ferroelectric properties at different total ferroelectric thicknesses by  $\text{Al}_2\text{O}_3$  (alumina) interlayers [15] to realize optimized, thickness independent, FeFET properties. The concept of ferroelectric lamination was recently reported for thick films of metal–ferroelectric–metal (MFM) in planar or 3D capacitor configuration [16] to optimize the ferroelectric stack properties for piezoelectric harvesters or the one-transistor–one-capacitor (1T–1C) FRAM concept, respectively. In this paper, the merits of the ferroelectric film lamination using an alumina interlayer are presented in relation to one transistor (1T) FeFET concept. This concept was recently reported in [17]. This paper aims to provide detailed insights into and an understanding of this novel device concept.



**Figure 1.** The FeFET memory development trend sparked by the discovery of ferroelectricity in fluorite structure hafnium oxide materials and driven by the key technological merits: cost, density, scalability, and CMOS compatibility. Reproduced with permission from [17] T. Ali et al., IEDM; published by IEEE, Copyright 2019, IEEE.

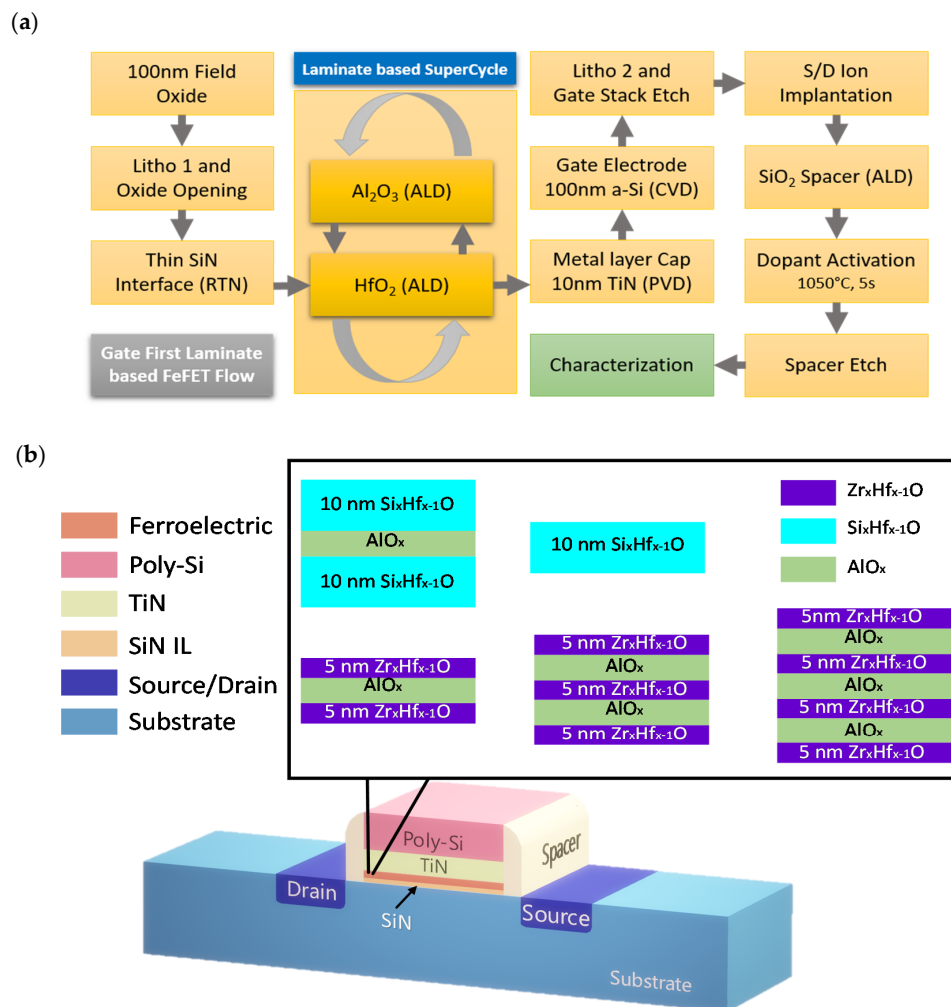
Another challenge for the emerging FeFET memory is a higher switching variability upon the area scaling. In a polycrystalline ferroelectric hafnium oxide-based film, the FeFETs encounter a transition from a gradual type of multi-level threshold voltage ( $V_T$ ) switching to an instant switching coupled to the limited grain count in a scaled device area [18]. As a result, the FeFET variability is increased and practically, the ferroelectric instant  $V_T$  switching hinders a potential MLC operation. This is mainly due to the absence of intermediate  $V_T$  storage levels. The second aim of this paper is to explore the potential of ferroelectric lamination for an area-independent MLC FeFET operation at an improved film granularity and hence a reduced variability.

A ferroelectric lamination such as that in an improved MLC operation becomes particularly beneficial for the FeFET based synaptic storage. The third aim of this paper is to study the different modes of the FeFET synaptic weight update and systematically

show the impact of the different modulation sequences as well as the effect of the FeFET area scaling.

## 2. Materials and Methods

The laminate FeFET devices were fabricated on 300 mm Si wafers using a gate first integration scheme as outlined in Figure 2a. Initial Si surface cleaning by DHF was followed by the controlled growth of a thin SiO<sub>2</sub>- (~1 nm) based native oxide using an SC1 based cleaning step. Afterward, a thin silicon nitride- (~1.8 nm) based interfacial layer (IL) was thermally grown by a rapid thermal nitridation (RTN) of the SiO<sub>2</sub> native oxide in ammonia (NH<sub>3</sub>) ambient to achieve a high permittivity IL [19]. The ferroelectric layer was deposited by atomic layer deposition (ALD) at 300 °C using the precursors (HfCl<sub>4</sub>:SiCl<sub>4</sub>) for Si doped hafnium oxide (HSO), (HfCl<sub>4</sub>:ZrCl<sub>4</sub>) for hafnium zirconium oxide (HZO). The H<sub>2</sub>O was used as an oxidizer. The basic ferroelectric layer thickness was chosen as 10 nm (16:1) of HSO and 5 nm (1:1) of HZO.



**Figure 2.** (a) The main steps of the FeFET integration with the laminate-based ferroelectric deposition step highlighted, (b) the laminate-based FeFET stack structure illustrated by the schematic view of the FeFET with, inset, the HSO and HZO stack flavors. Reproduced with permission from [17] T. Ali et al., IEDM; published by IEEE, Copyright 2019, IEEE.

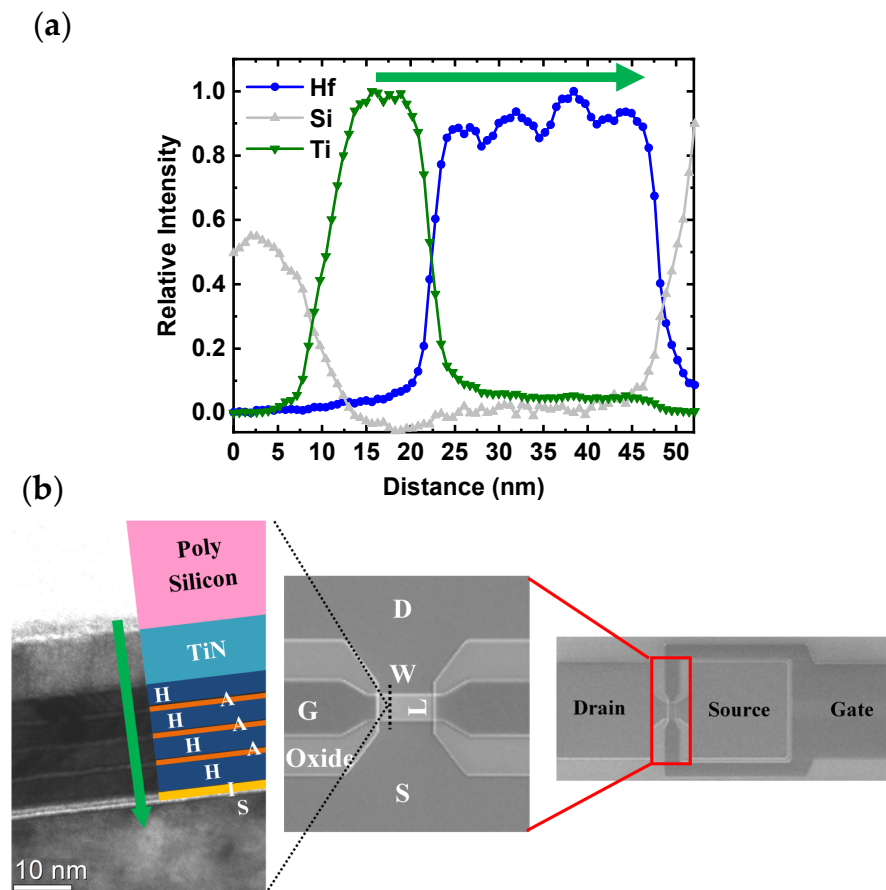
The single ferroelectric layer of HSO or HZO material was used to construct a ferroelectric stack (Figure 2b) with HSO as (2 × 10 nm) and HZO as (2 × 5 nm, 3 × 5 nm, 4 × 5 nm) using a thin Al<sub>2</sub>O<sub>3</sub> (alumina) interlayer. The (n × d) representation refers to the number of ferroelectric layers, (n) refers to the thickness of the individual layers and (d) refers to the lamination stack. Thereby, the total ferroelectric thickness of the stack was



20 nm for the HSO and (10 nm, 15 nm, 20 nm) for the HZO with lamination. As a reference, a non-laminated 10 nm HSO layer was deposited. The alumina interlayer was deposited using a Trimethylaluminium (TMA) precursor at a growth rate of 0.9 Å per cycle for five cycles after each HSO (10 nm) and HZO (5 nm) layer deposition.

A 10 nm TiN metal electrode was sputtered in a physical vapor deposition (PVD) process as a capping metal for the ferroelectric deposited stack. This was followed by chemical vapor deposition (CVD) of the 100 nm amorphous silicon (aSi) layer as the top gate electrode contact. The subsequent process steps were the same as reported earlier [19] while an additional SiO<sub>2</sub> spacer (13 nm) was used for the gate stack encapsulation. A gate first thermal budget of 1050 °C, 5 s was applied to the source and drain dopant activation and ferroelectric stack crystallization were completed in a single step.

The FeFET is shown in Figure 3 with an SEM top view and a TEM cross-section of the laminated ferroelectric layers of a 4 × 5 nm-based stack. This is further highlighted in Figure 3a by the EDX line-scan of the elemental distribution of the materials constructing the gate stack. In particular, the Hf line-plot shows multiple dips reflecting the position of the intercepting alumina layers inside the ferroelectric stack.



**Figure 3.** (a,b) The integrated FeFET scanning electron microscope (SEM) top view and transmission electron microscope (TEM) cross-section analysis of the stack with an inset of the high-k (H)/alumina (A) alternating layers along with the EDX line-scan of the stack elemental distribution. Reproduced with permission from [17] T. Ali et al., IEDM; published by IEEE, Copyright 2019, IEEE.

To separately study the thickness dependence of the ferroelectric properties as well as the role of the ferroelectric stack lamination, an MFM-based structure was fabricated. Initially, a highly doped n-type Si substrate was used where a bottom TiN electrode was deposited by ALD at 450 °C using TiCl<sub>4</sub> and NH<sub>3</sub> precursors. As in the FeFET, the HSO and HZO layers were deposited by ALD at 300 °C using (HfCl<sub>4</sub>:SiCl<sub>4</sub>), (HfCl<sub>4</sub>:ZrCl<sub>4</sub>) precursors, and H<sub>2</sub>O as an oxidizer. A thickness split of the HZO layer (5 nm, 10 nm, 15 nm, 20 nm)

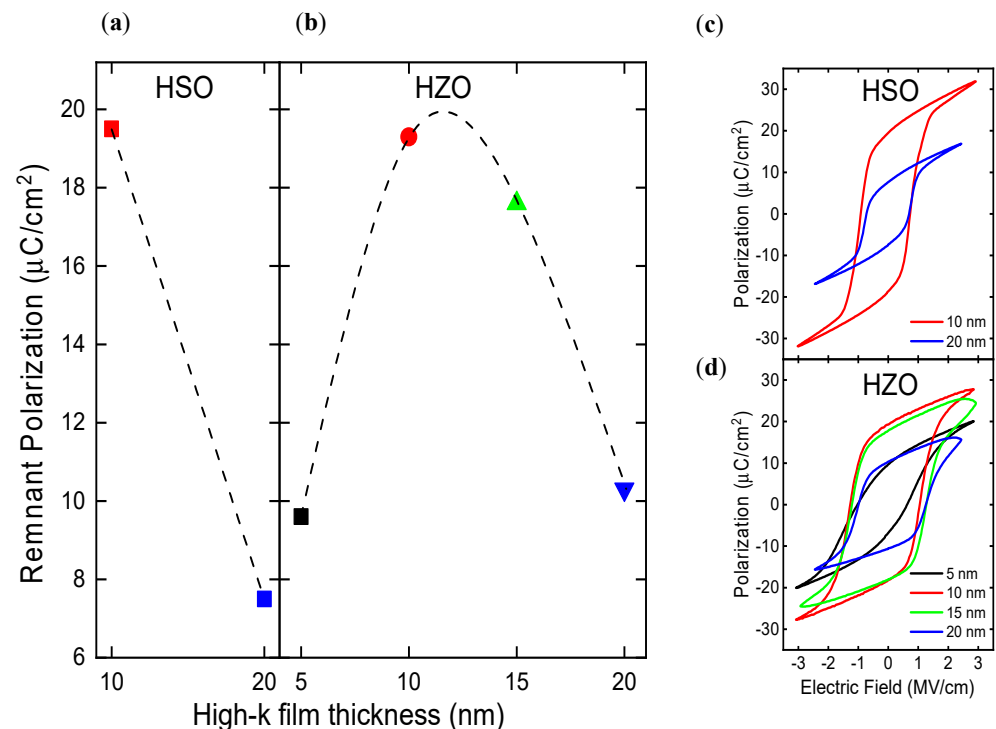
and the HSO layer (10 nm, 20 nm) was deposited without lamination and based on optimal Hf:Zr (1:1) and Hf:Si (16:1) content ratios.

As a benchmark, the role of ferroelectric layer lamination was outlined by depositing HSO ( $2 \times 10$  nm) ferroelectric layers where the single 10 nm HSO layer was similarly based on (16:1) optimal Si content. A top TiN electrode was fabricated by magnetron sputtering at room temperature to avoid uncontrolled crystallization of the ferroelectric stack. A thermal budget of 800 °C, 20 s, and 500 °C, 30 s was applied on the HSO and HZO-based MFM for ferroelectric crystallization, respectively. The MFMs were subsequently structured using Ti/Pt contact dots deposited by electron beam evaporation through a shadow mask. Finally, the electrically isolated MFM capacitors were formed by etching the top TiN electrode using an SC1 based process.

### 3. Results and Discussion

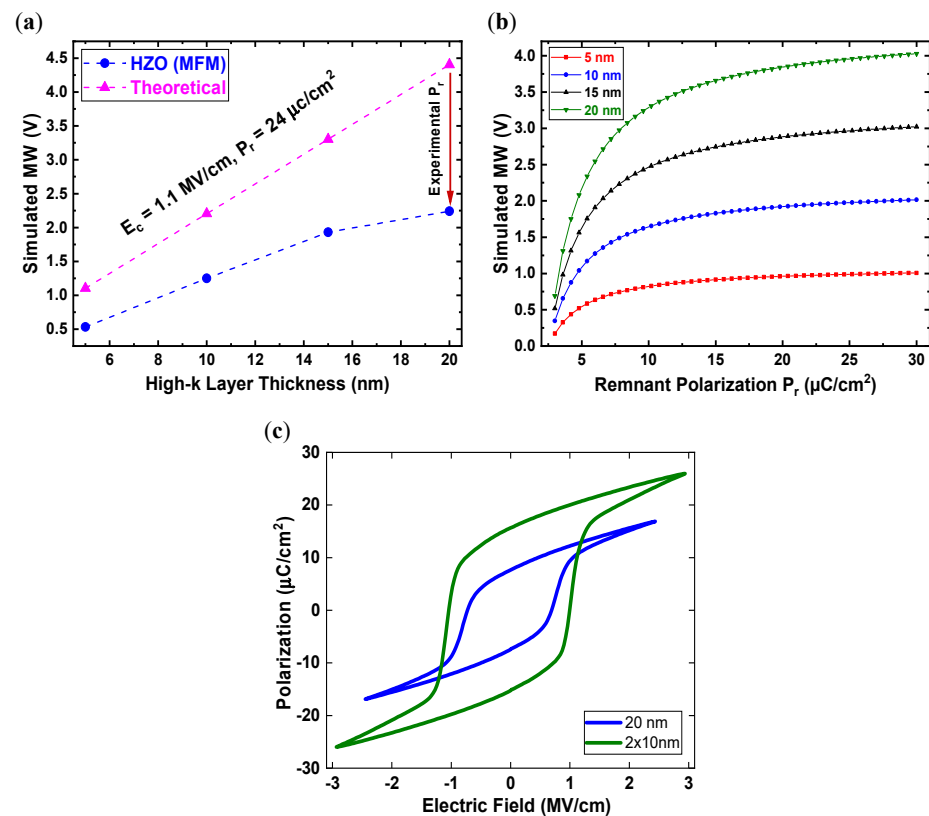
#### 3.1. The Laminated MFM and Stack Characteristics

In an MFM structure, the  $P_r$  change over the ferroelectric thickness reflects the strong role of the film stress on the stabilization of the ferroelectric phase. In a thin ferroelectric film, the crystallization and thus the stabilized crystallographic phase is affected by the film stress induced by the metal electrodes. The metal electrodes provide a mechanical capping to prevent the volume expansion of the basic unit cell; this reduces the monoclinic phase formation as indicated in the first report by Böschke et al. [7]. The ferroelectric thickness variation also affects the average grain size formation and hence the ferroelectric properties. For HSO and HZO ferroelectrics, the ferroelectric properties were studied as shown in Figure 4a,b for the  $P_r$  change in relation to the thickness and in Figure 4c,d with the corresponding P-E hysteresis. The transition toward a thicker ferroelectric film of 20 nm showed a decrease in  $P_r$ , which was a consequence of an increased average grain size thus favoring the monoclinic phase formation [20].



**Figure 4.** The  $P_r$  versus ferroelectric layer thickness for (a) HSO and (b) HZO using MFM-based capacitors. The corresponding polarization-electric field (P-E) hysteresis (c,d) shows a significant  $P_r$  decrease upon the increase in the ferroelectric thickness. Reproduced with permission from [17] T. Ali et al., IEDM; published by IEEE, Copyright 2019, IEEE.

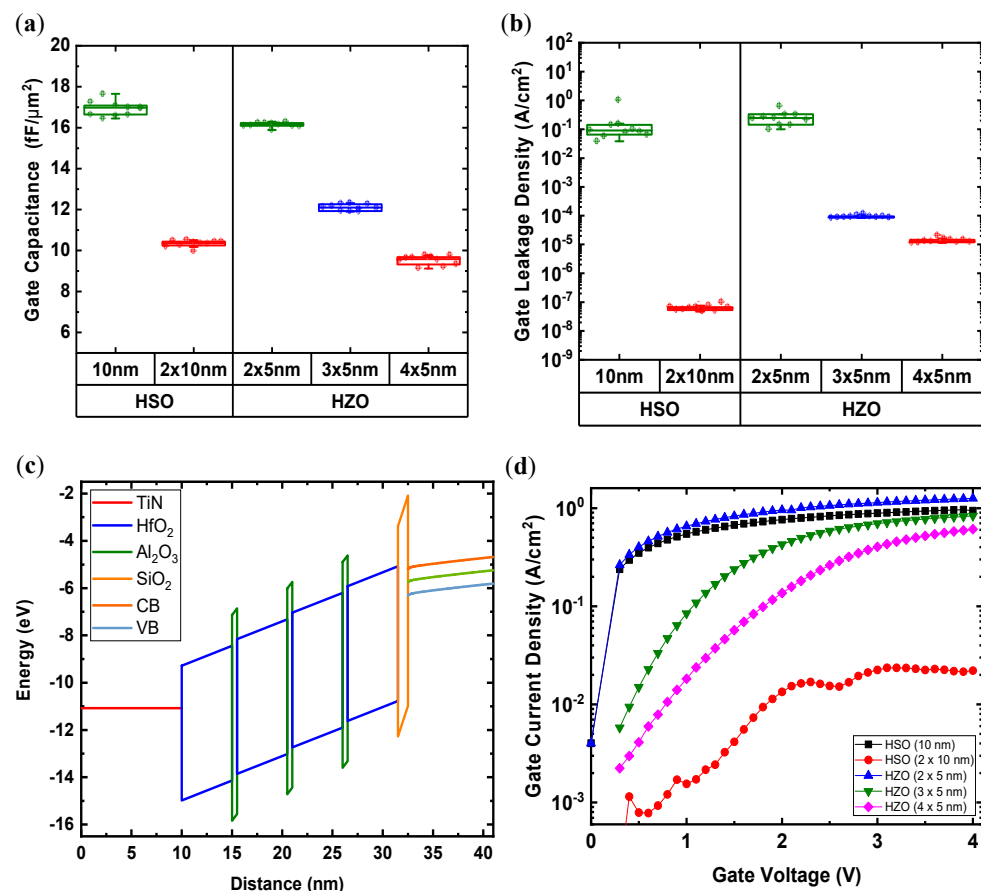
The numerical simulation of the FeFET memory was realized based on an iterative solution of the FET equation with the ferroelectric layer properties incorporated. This approach is central to theoretical FeFET modeling [21–23]. The measured ferroelectric properties as  $P_r$  and  $E_c$  values of the HZO material (Figure 4) were used in the FeFET numerical simulation to estimate the maximum MW of each ferroelectric layer thickness (Figure 5a). In comparison, a saturated high  $P_r$  value ( $24 \mu\text{C}/\text{cm}^2$ ) was used to indicate the potential theoretical reference for the maximum MW of each thickness (5 nm to 20 nm). The increase in the HZO ferroelectric layer thickness (Figure 5a) shows that the calculated MW, based on the measured MFM  $P_r$ , was far lower than the theoretical one. This MW gap increased as the ferroelectric thickness increased as a manifestation of the critical  $P_r$  decrease. This reveals that the ferroelectric  $P_r$  is as an important parameter for achieving the target MW increase with increasing thickness as pointed out in Figure 5b of the simulated MW dependence on the  $P_r$  for (5 nm to 20 nm) ferroelectric thickness. In the low range of  $P_r$  values (Figure 5b), comparable to the ones measured in the MFM configuration (20 nm), the obtained MW becomes significantly lower than the saturated one. To preserve a high  $P_r$  at an increased ferroelectric thickness, the single ferroelectric layer (20 nm) was replaced by a laminate ( $2 \times 10$  nm) stack with an alumina interlayer. The polarization-electric field (P-E) hysteresis in Figure 5c shows a comparison between the single ferroelectric layer and the laminate ferroelectric stack of the same HSO total ferroelectric thickness (20 nm). A higher  $P_r$  was achieved by the ferroelectric stack lamination.



**Figure 5.** The simulated FeFET MW variation with (a) ferroelectric layer thickness based on the measured HZO P-E parameters versus the theoretical ones, (b) the ferroelectric  $P_r$  at different ferroelectric thicknesses shows a lower MW with a  $P_r$  decrease, (c) the benchmark of a single versus laminated MFM-based P-E hysteresis of a 20 nm HSO layer. Reproduced with permission from [17] T. Ali et al., IEDM; published by IEEE, Copyright 2019, IEEE.

In addition, the ferroelectric lamination affected the basic metal-ferroelectric-insulator-semiconductor (MFIS) stack characteristics such as capacitance and leakage. The effect of ferroelectric lamination can be deduced in Figure 6 from the measured stack capacitance

per unit area in accumulation, as well as the current density of the stack leakage. The MFIS stack capacitance per unit area was measured on a capacitor of a  $10^4 \mu\text{m}^2$  size with a gate voltage sweep range ( $-5 \text{ V}$  to  $5 \text{ V}$ ) at a frequency of  $3 \text{ KHz}$ . The gate leakage current was measured on the same capacitor size via a gate voltage sweep ( $-0.2 \text{ V}$  to  $4 \text{ V}$ ) where the leakage current is extracted at a  $3 \text{ V}$  gate voltage. For a benchmark of the different ferroelectric stacks, the accumulation capacitance was extracted at a gate voltage ( $-3 \text{ V}$ ) and plotted in Figure 6a for the HSO and HZO materials. Based on an identical interface layer (IL), a trend of decreased capacitance per unit area occurred as the ferroelectric stack thickness increased. Thereby, the difference in permittivity values as well as the count of alumina interlayers causes a lower HZO stack capacitance compared to the HSO one (Figure 6a) at the same total stack thickness (e.g.,  $20 \text{ nm}$ ).



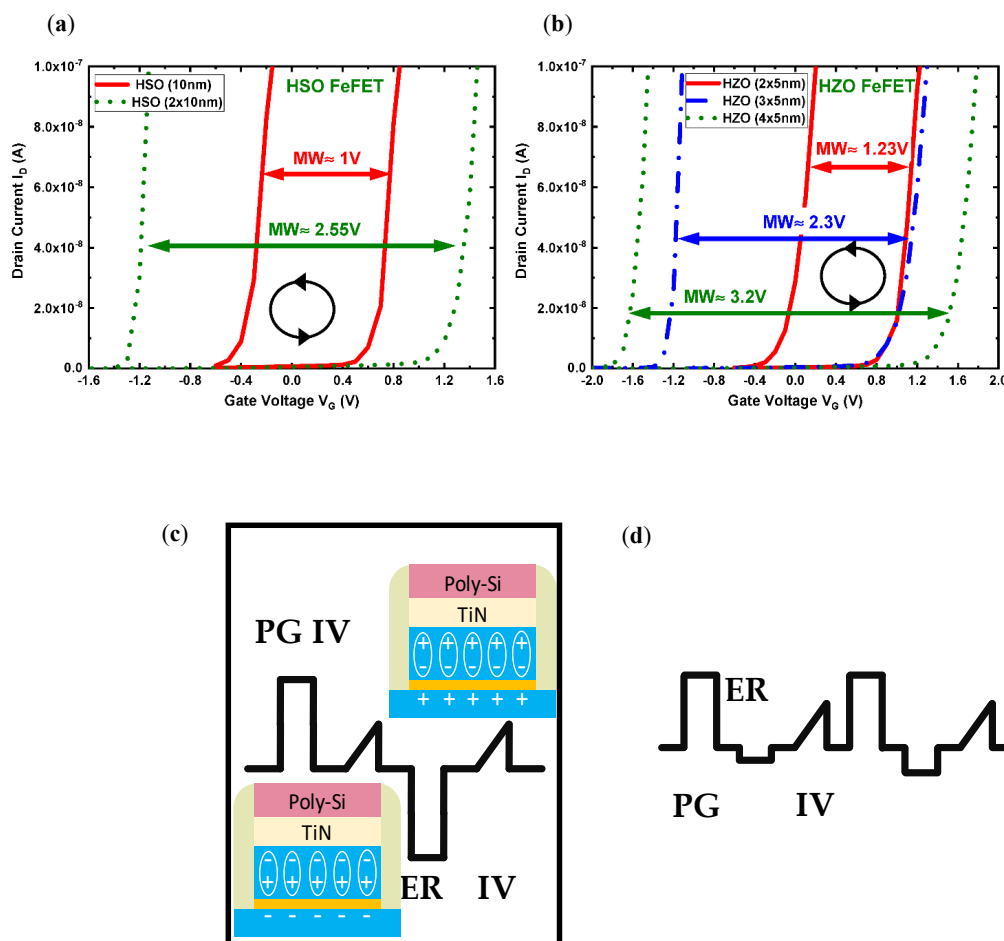
**Figure 6.** The laminate FeFET gate stack characteristics as (a) capacitance per unit area in accumulation obtained from the high-frequency capacitance–voltage measurements and (b) leakage current density obtained from the DC gate current versus gate voltage sweep, (a,b) shows the role of stack structure type and thickness, (c) the energy band diagram of the laminated ferroelectric stack ( $4 \times 5 \text{ nm}$ ) under PG conditions at  $6 \text{ V}$ , (d) gate leakage current density for voltage sweep ( $0 \text{ V}$  to  $4 \text{ V}$ ) benchmarking the different single and FE laminate stacks. (a,b) Reproduced with permission from [17] T. Ali et al., IEDM; published by IEEE, Copyright 2019, IEEE.

For the same SiN based IL, the capacitance change in Figure 6a reflects the opposite trend of an increased operating voltage to achieve the same ferroelectric switching field, which is in part attributed to the lamination effect. Thus, the control of both the total stack thickness and the alumina interlayer count is an essential tradeoff for ferroelectric stack optimization. However, the key merit of the ferroelectric stack lamination is the decrease in the gate current density (Figure 6b,d) that reflects both the effect of the lamination and the stack thickness increase. Due to the higher dielectric bandgap of the alumina interlayers, the ferroelectric stack lamination constitutes an alternative low-high dielectric band energy

profile (Figure 6c) that reduces the gate stack leakage density. In essence, a difference in the leakage properties between the HSO and HZO laminates (20 nm) indicates degraded HZO dielectric properties. This is mainly due to the associated gate first (1050 °C) thermal budget. Thereby, the HZO leakage effect is alleviated by the stack lamination.

### 3.2. The Laminate FeFET Memory Switching

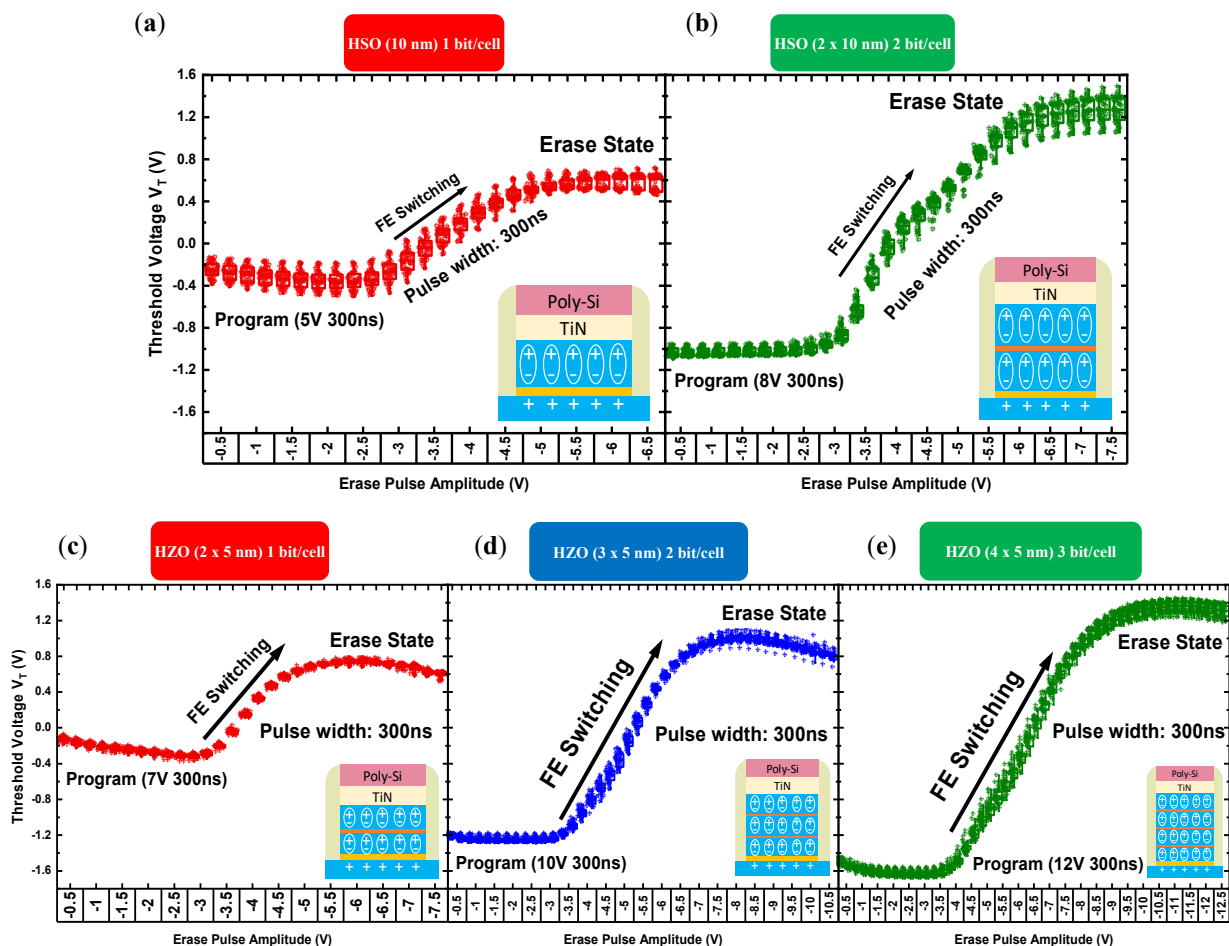
The reversible dipole switching has polarization charges that can modulate the channel conductivity. The program/erase (PG/ER) pulses (Figure 7c) can reversibly switch the dipoles with the internal dipole field affecting the channel surface potential, hence the  $V_T$  shift. Thus, the laminate FeFET memory switches state after the PG/ER pulse which is measured by an  $I_D$ - $V_G$  sweep where a counterclockwise switching i.e., a low/high (PG/ER)  $V_T$  shift, is observed as a sign of ferroelectric switching. This particular  $V_T$  shift direction occurs as the surface charges near the channel which modulate the extent of the channel inversion. However, this switching behavior is also dependent on the ferroelectric stack type as shown in Figure 7a,b which illustrate a different MW size by varying the stack material type and thickness. The MW expression was considered with a detailed analytical treatment of the FeFET stack [24] and is more commonly represented by Equation (1) which considers the remanent polarization ( $P_r$ ), the coercive field ( $E_c$ ), and thickness ( $d_F$ ) as direct factors affecting the MW size.



**Figure 7.** The laminate FeFET counterclockwise  $I_D$ - $V_G$  switching characteristics illustrated as a comparison for the different stack flavors of (a) HSO and (b) HZO material, electrical measurement sequence for (c) the MW switching, (d) the ER amplitude dependence of ferroelectric switching. Reproduced with permission from [17] T. Ali et al., IEDM; published by IEEE, Copyright 2019, IEEE.



The trend in Figure 7a,b shows consistently the role of ferroelectric thickness increase in forming an MW of a higher size. This trend is reproducible for HSO and HZO materials. Although, for the same total ferroelectric stack thickness (e.g., 20 nm), a marked difference between the HSO and HZO can be observed. This indicates the different film properties of HSO and HZO and thus, suggests that other factors such as  $P_r$  and  $E_c$  can affect the MW size. The field-dependent evolution of ferroelectric switching as shown in Figure 8 with an ER pulse amplitude increase gives a valuable insight into the MLC operation. The ER amplitude switching was measured on a device of width  $\times$  length ( $W \times L$ ) ( $25 \mu\text{m} \times 25 \mu\text{m}$ ) with cross wafer statistics measured at a PG/ER pulse width (300 ns). By using a reference PG pulse while gradually increasing the ER pulse amplitude as depicted in Figure 7d, the  $V_T$  shift was controlled to a target level in the MLC window. The PG low  $V_T$  gradually shifted toward the high  $V_T$  (ER state) after each increase in the amplitude of the ER pulse until a saturated ER switching was reached. Hence, the MLC capacity (bit/cell) is dependent on the maximum  $V_T$  shift (dynamic range), which is significantly improved by the ferroelectric stack lamination, thus enabling an MLC storage up to 3 bit/cell.



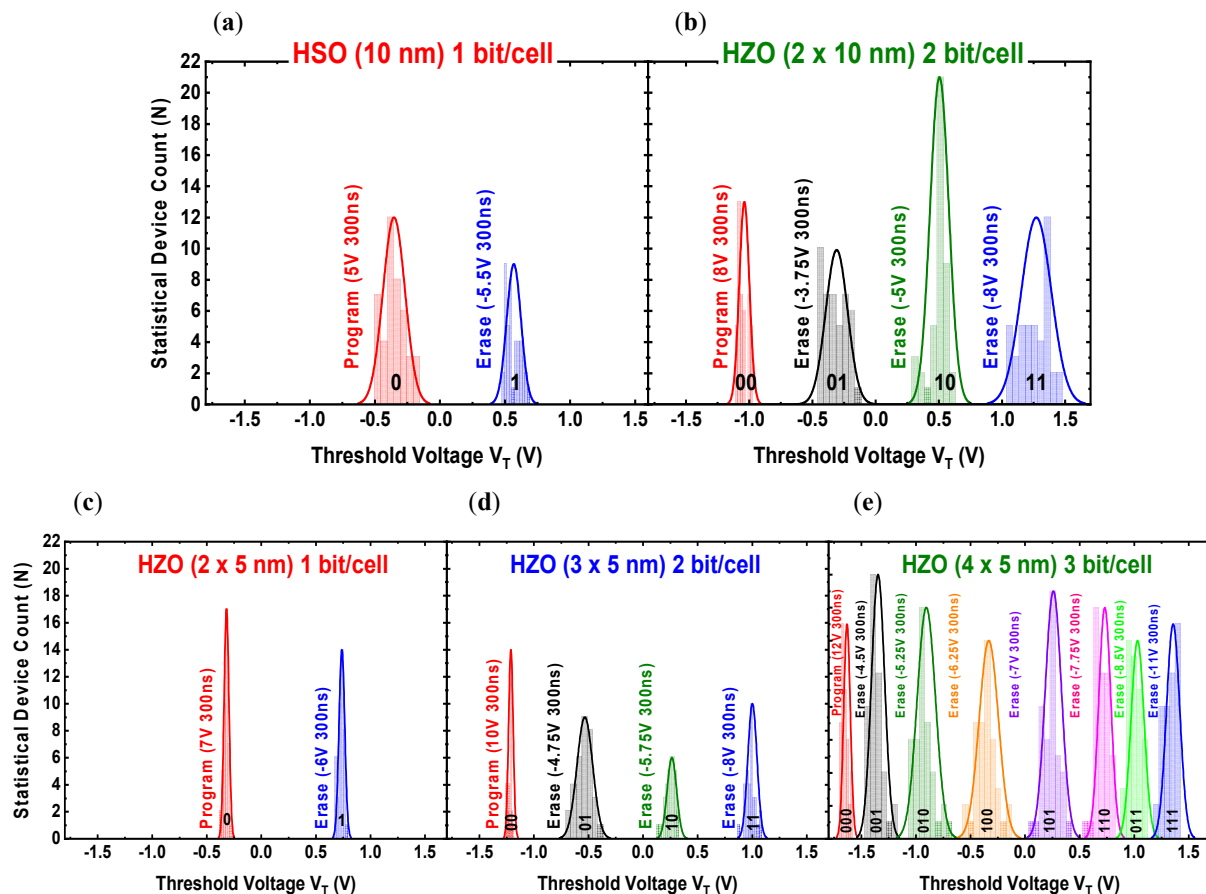
**Figure 8.** (a–e) The cross wafer statistical ER  $V_T$  shift extracted using constant current criterion (10 nA) for an incremental ER amplitude at a 300 ns pulse width on the different stack structures (inset) shows the ferroelectric switching with a higher dynamic range in relation to the laminate stack thickness increase enabling a variety of bit/cell storage of the FeFET. Reproduced with permission from [17] T. Ali et al., IEDM; published by IEEE, Copyright 2019, IEEE.

### 3.3. The Multi-Level Coding Operation (1 bit, 2 bit, 3 bit/cell)

For a higher storage capacity per cell, the quantization of an underlying memory storage mechanism was explored to realize multi-level storage with a distinct separation between the levels. For instance, the charge quantization as in a floating gate or charge

trap concept enables a quantized accumulation of stored charges to be mapped to states beyond the single-level cell [25]. Likewise, the phase-change memory (PCM) relies on the quantization of the resistance change by an induced control of the crystallization level for chalcogenide alloys (GST) [26]. Practically, both concepts are similarly challenged by the aggressive scalability where noise effects, interference between cells, and statistical fluctuations require error correction coding.

Similarly, the FeFET utilizes the quantization of the ferroelectric polarization switching to realize multi-level storage. For different ferroelectric stack thicknesses, the 1–3 bit/cell storage is shown by the  $V_T$  distribution to reflect in Figure 9 the different operating levels. The  $V_T$  histogram distribution in Figure 9 was extracted from the ER  $V_T$  shift of Figure 8 at selected ER amplitudes, as one requirement for reliable MLC storage is the maximized VT shift. In addition, the variability of intermediate states can affect the maximum bit/cell that can be reliably stored. Hence, the single bit/cell operation was reliably stored for the thinner (10 nm) ferroelectric film thickness as in the HSO and HZO-based stacks (Figure 9 a,c). As the ferroelectric layer thickness is increased with lamination, the storage capacity is extended to a two bit/cell as in Figure 9b,d, or even as three bit/cell storage (Figure 9e).



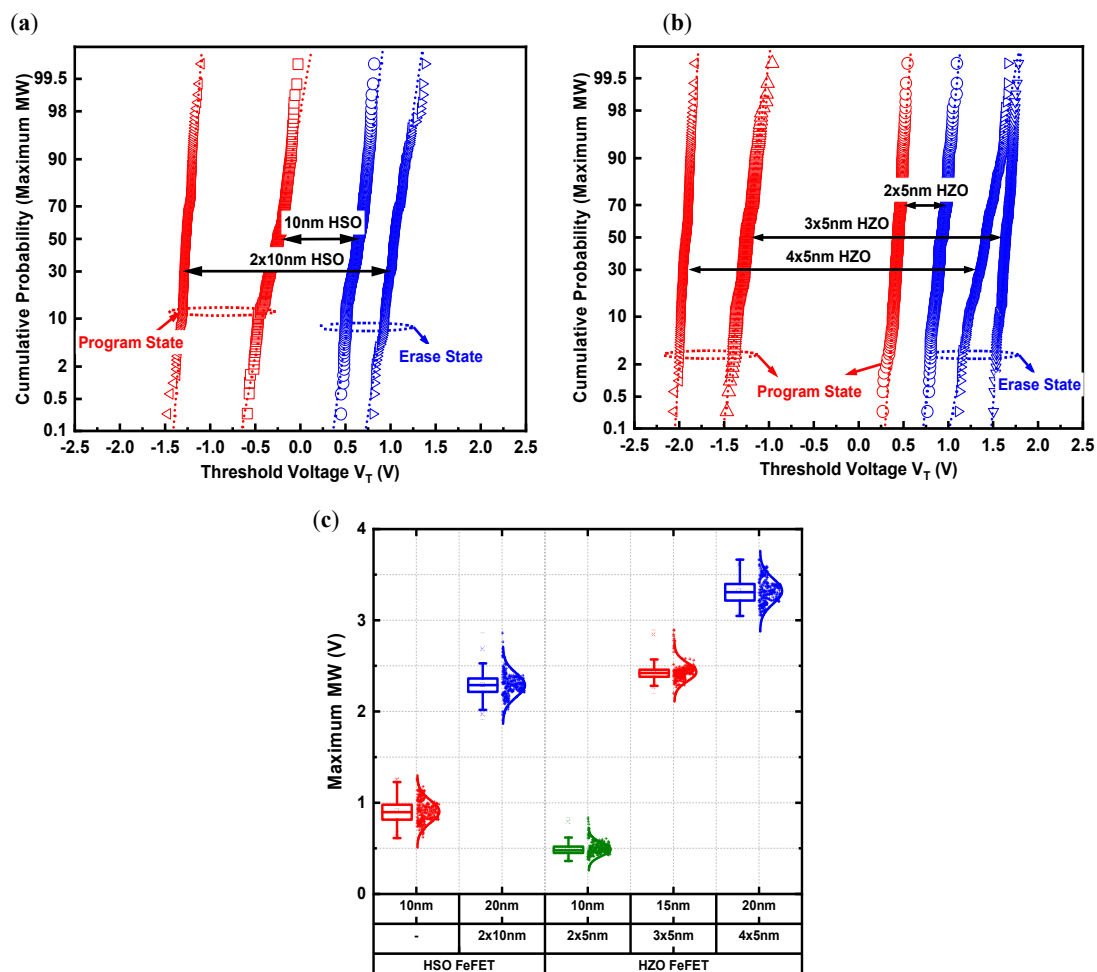
**Figure 9.** (a–e) The corresponding histogram  $V_T$  distribution at selected ER amplitude switching conditions shows the different bit/cell operation capability of the FeFETs indicating an improved MLC density for increased laminate-based ferroelectric thicknesses. Reproduced with permission from [17] T. Ali et al., IEDM; published by IEEE, Copyright 2019, IEEE.

In essence, the MLC operation in Figure 9 is illustrated for a FeFET based  $W \times L$  ( $25 \mu\text{m} \times 25 \mu\text{m}$ ) where the intrinsic polycrystalline film variability is minimal. As outlined earlier, a limited  $V_T$  shift window was present for the HSO material at the same thickness (20 nm) compared to the HZO. This indicates that the alumina interlayer insertion for the HSO stack caused a deviation from the optimal ferroelectric phase. This is indeed in line with the HSO sensitivity to dopant content concentrations [27]. Therefore, the optimal

tuning content and crystallization properties are different for a ferroelectric laminated stack as compared to a single ferroelectric layer. Thus, the careful control of the HSO doping concentration is crucial for optimum ferroelectric phase stabilization especially in the presence of the alumina interlayer. In contrast, the broad ferroelectric phase window in the HZO material indicated stable ferroelectric properties with lamination, and more particularly in FeFET in the form of a higher MW size.

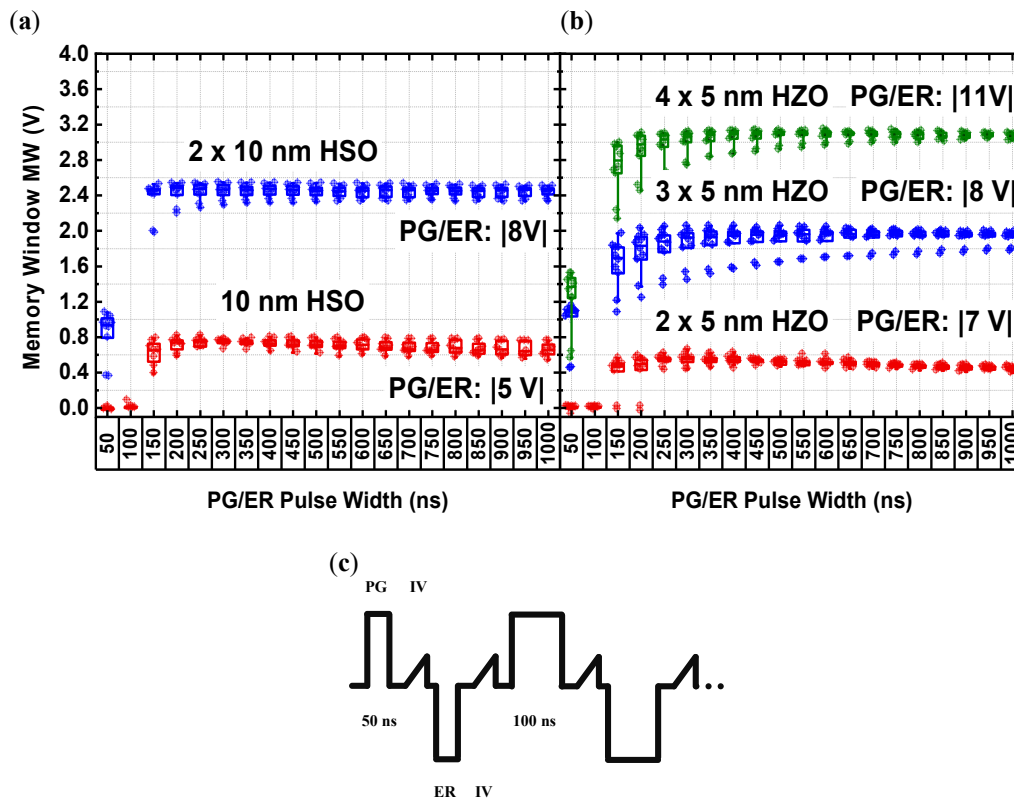
### 3.4. The Maximum MW Dependence on Ferroelectric Stack Thickness

The primary role of the ferroelectric stack lamination is to enable an increased ferroelectric layer thickness without jeopardizing the optimal properties such as the ferroelectric  $P_r$ . At a sufficiently high  $P_r$ , the linear relation between the ferroelectric stack thickness and the MW increase as in Equation (1) remains intact. This aim of the ferroelectric stack lamination for a maximized MW upon an increase in thickness can be pointed out by the global wafer cumulative probability of the PG/ER  $V_T$  shift (Figure 10a,b) based on the obtained conditions of the saturated switching (Figure 8). The increase in the MW to values close to the theoretical and maximum values of the MW shown earlier in Figure 3b indicates significant merits for ferroelectric stack lamination to stabilize the optimal ferroelectric properties at higher film thicknesses.



**Figure 10.** The global wafer PG/ER  $V_T$  distribution, based on the optimal conditions shown in Figure 8, independent of ferroelectric/laminate stack with the cumulative probability for (a) HSO, (b) HZO, and (c) obtained maximum MW in relation to the ferroelectric/laminate thickness. Reproduced with permission from [17] T. Ali et al., IEDM; published by IEEE, Copyright 2019, IEEE.

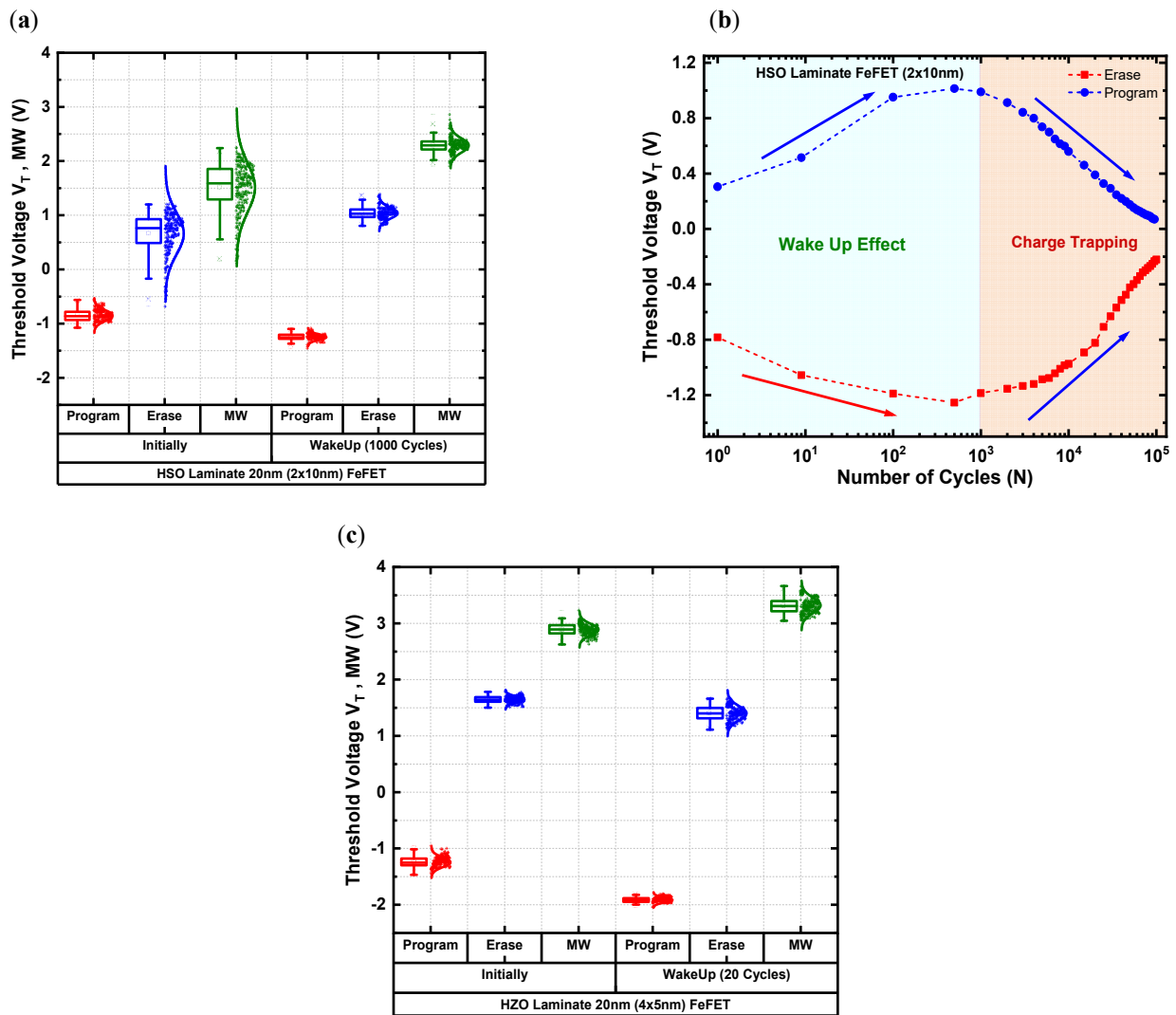
Similarly, the MW in Figure 11 was measured for each ferroelectric stack thickness at an optimal pulse amplitude while sweeping the PG/ER pulse width (50 ns to 1  $\mu$ s) was swept. Figure 11 shows a small MW change beyond the 300 ns pulse width; this indicates a saturated switching at a MW maximum for each thickness. Thus, the field magnitude of switching (Figure 8) as well as the pulse width sweep (Figure 11), both show an increasingly higher MW upon the thickness increase indicating a preserved high  $P_r$  as a result of the lamination. This trend of MW dependence on the ferroelectric stack thickness is illustrated in Figure 10c by the plot of the maximum MW versus the ferroelectric stack thickness.



**Figure 11.** The MW dependence on the write pulse width for (a) the HSO and (b) the HZO ferroelectric laminate stack shows a saturated maximum of the MW at each ferroelectric stack thickness, (c) the measurement test sequence for the MW dependence on the pulse width. Reproduced with permission from [17] T. Ali et al., IEDM; published by IEEE, Copyright 2019, IEEE.

### 3.5. The Role of Wakeup and Charge Trapping

The initially anticipated effect of the insertion of an alumina interlayer appeared in the optimal ferroelectric  $P_r$  and was more critical for the HSO material. However, the further role of the alumina interlayer is important when considering the material phenomenon as a wake-up effect of the HSO and HZO laminates. The HSO global wafer PG/ER  $V_T$  and MW distribution as in Figure 12a measured for FeFET  $W \times L$  (4  $\mu$ m  $\times$  4  $\mu$ m) showed a higher switching variability for pristine devices. This variability is due to the different initial phases in the pristine film. The wakeup cycling causes an induced transition to a dominant ferroelectric phase for a narrower  $V_T$  and for MW distribution. The post wakeup increase in the MW size indicates a higher post wakeup remnant polarization. This effect was monitored by the  $V_T$  evolution over cycling as in Figure 12b where the symmetric |8 V|, 300 ns pulses showed a gradual and symmetric increase in the PG/ER  $V_T$  window to a maximum at  $10^3$  cycles. This increase in the MW size with the wakeup  $P_r$  increase was compensated by a dominant charge trapping effect beyond the  $10^3$  cycles. This lead to the MW closure.



**Figure 12.** The effect of wakeup and charge trapping on the switching characteristics of (a) the HSO laminate stack with (b) the  $V_T$  evolution over cycling; (a) the HSO laminate stack in comparison to (c) the HZO laminate stack. PG/ER and cycling conditions are based on Figure 8. Reproduced with permission from [17] T. Ali et al., IEDM; published by IEEE, Copyright 2019, IEEE.

The trend shown in Figure 12b reveals two different dominant effects inside the stack for  $V_T$  switching as wakeup where a maximized  $V_T$  window is obtained versus charge trapping that leads to  $V_T$  window closure. In contrast, the wake-up effect in particular was less pronounced in the case of the HZO laminate as shown in Figure 12c. In the case of the HZO laminates, the maximum MW was reached in a fewer number of wake-up cycles. In contrast to the HSO material, the HZO initial and post wakeup variability were lower. In the context of the multi-level cell operation, both the wakeup and charge trapping effects can practically hinder initial and steady MLC operations. Additionally, as indicated in Figure 12b, the pre-requirement of wakeup cycles to reach the maximum MW size for reliable MLC operations will in turn limit the maximum enduring range of the device. As indicated in Figure 12a–c, the wakeup effect is strongly dependent on the material and stack type as well as the thermal budget conditions [28].

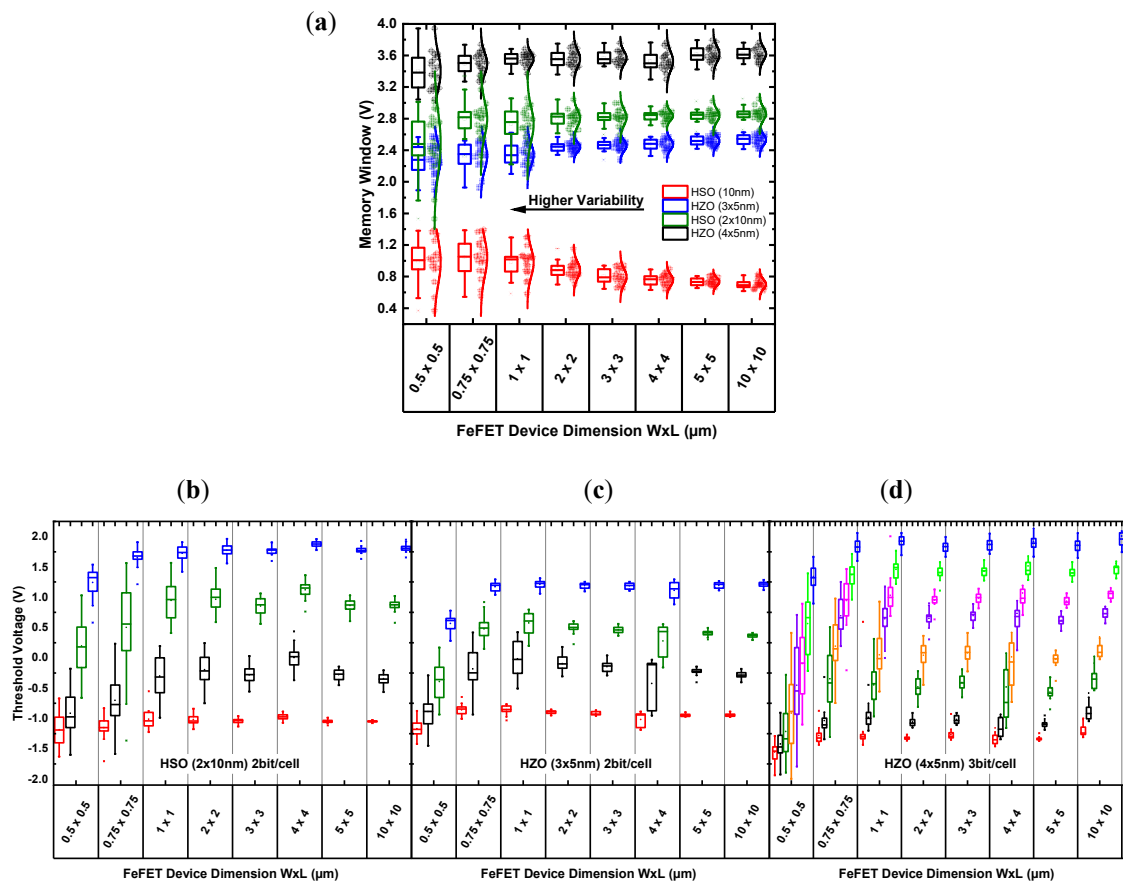


### 3.6. The MLC FeFET Area Dependence

In a polycrystalline ferroelectric film, the obtained properties result from a superposition effect due to a large ensemble of grain sizes and texture distributions [29]. In large ferroelectric areas i.e., FeFETs with large feature sizes, the averaging effect produces comparable ferroelectric properties. Thus, a uniform FeFET response with minimal fluctuations in the  $V_T$  shift is measurable on a statistical level [14]. In contrast, the area downscaling features, in particular, the transition to a more discrete distribution of the orientation-dependent coercive field. In turn, the magnitude factor of the surface potential and hence the  $V_T$  as well as the MW becomes discrete in distribution and thus raises stronger statistical fluctuations. At ultimate scalability, the discrete type of the distribution of countable grains reduces to a single grain producing further statistical fluctuations. However, a single grain also features just a single, sharp switching transition, also known as instant switching [30].

From an MLC operation perspective, the statistical fluctuations as well as the instant switching as features of the ferroelectric area scalability are key challenges for an MLC-based FeFET. An instant switching FeFET has no accompanying intermediate states and is thus impractical for MLC storage. Likewise, statistical fluctuations increase the overlap in distributions and prevent a reliable separation between the MLC states without complex error correction algorithms. Hence, the area dependence of the FeFET variability becomes an important reliability factor especially for the MLC storage. The MW variability versus the area is measured for FeFETs with dimensions in the range from  $W \times L$  ( $10 \mu\text{m} \times 10 \mu\text{m}$ ) to ( $0.5 \mu\text{m} \times 0.5 \mu\text{m}$ ) of the different HSO and HZO based ferroelectric stacks.

In Figure 13a, the large FeFETs show a small MW variation and feature a transition toward an increased MW variation as the FeFET area is scaled. As outlined earlier, the high variability affects the MLC storage due to the higher variation in the intermediate levels as shown in Figure 13b–d for a 2–3 bit/cell operation, particularly with the evolution toward a smaller device area. This size dependent variability is also a strong function of the type of ferroelectric material, stack structure control, and essentially the thermal budget. One of these optimization aspects is achieved by the ferroelectric stack lamination. For the thin ferroelectric layer, the grains exhibit columnar growth between the two electrodes. The stack lamination provides an interruption barrier for the columnar grain growth. In turn, this serves to improve the ferroelectric stack granularity. This enables the gradual switching transition in the form of an increased count of the intermediate storage levels as shown in Figure 14a. In contrast, the instant switching dominates for the single ferroelectric layer without lamination considering the same  $W \times L$  ( $0.5 \mu\text{m} \times 0.5 \mu\text{m}$ ) FeFET dimensions. The instant switching reflects a single grain formation where the average grain size growth is dependent on the applied thermal budget to crystalize the film [20,26]. Another key merit, as shown in Figure 14b, is the narrow  $V_T$  distribution when the HZO ferroelectric stack is laminated ( $2 \times 5 \text{ nm}$ ). This enables a reliable 2 bit/cell storage. In contrast, the HSO of the same thickness (10 nm) without lamination showed a broader  $V_T$  distribution thereby preventing a reliable 2 bit/cell storage.

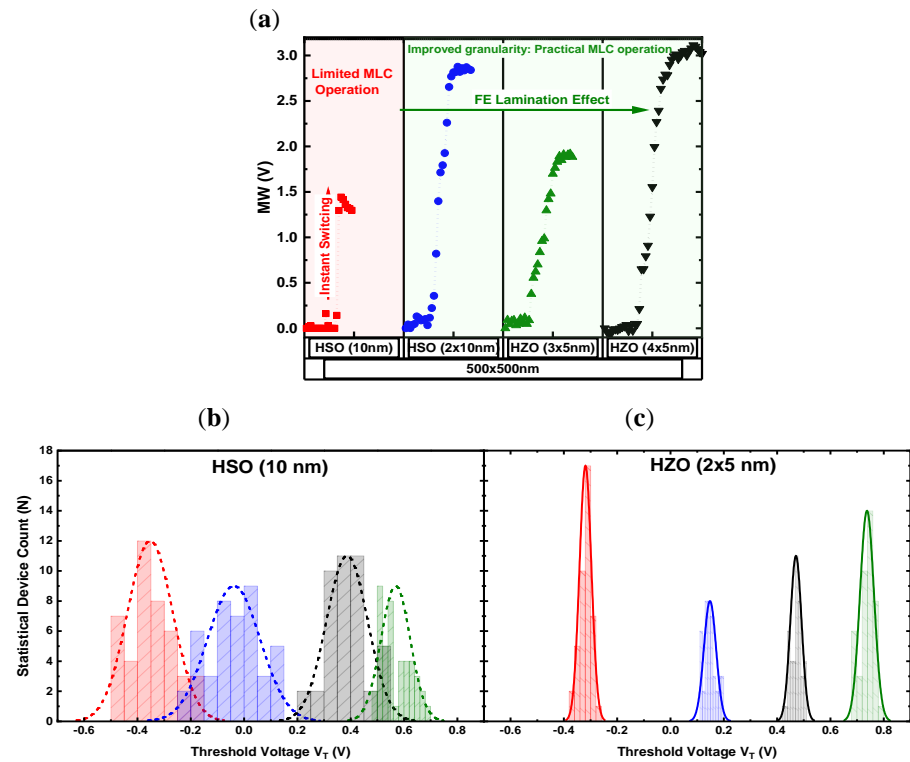


**Figure 13.** The cross wafer statistical MW/MLC operation in relation to the FeFET area for the different ferroelectric/laminate stacks with (a) maximum MW and (b–d) the evolution of 2–3 bit threshold voltage levels upon area decrease, (a–d) indicates a higher variability in the statistical MLC levels upon area scaling. Reproduced with permission from [17] T. Ali et al., IEDM; published by IEEE, Copyright 2019, IEEE.

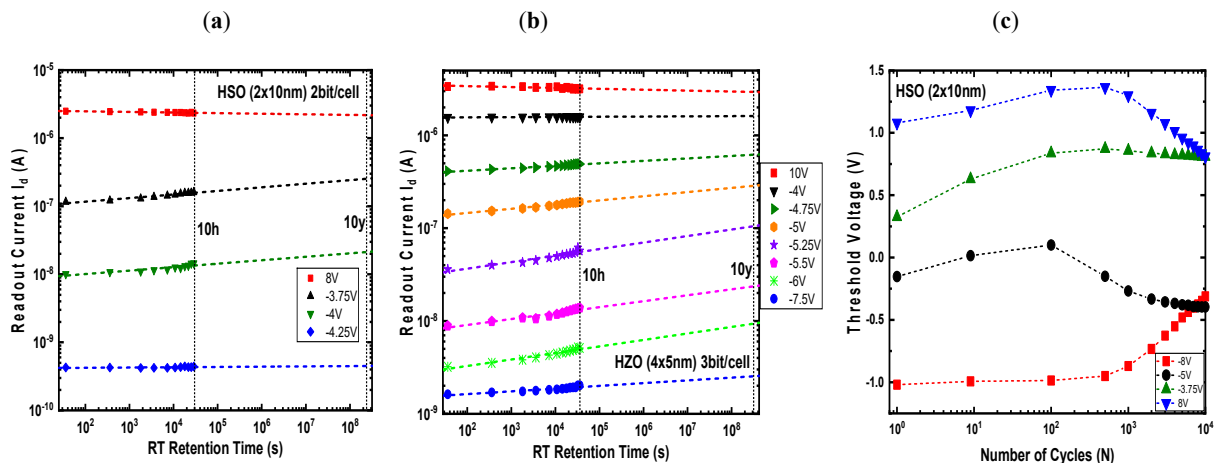
### 3.7. The MLC Retention and Endurance

To define the  $V_T$  shift of each MLC storage level, the FeFET operates partially in a ferroelectric sub-loop switching. At the sub-loop operation, the switchable dipoles have a preferential orientation that favors a low voltage unsaturated switching. However, this has at the same time the net effect of a lower  $E_c$  and renders the dipoles more susceptible to reversible switching. Hence, the retention stability of the different  $V_T$  levels is an important factor of reliable MLC storage. The retention was measured as 2 bit/cell (HSO) and 3 bit/cell (HZO) by initially programming the FeFET and applying ER pulses of different amplitudes per each storage level; the readout current of each state was then monitored for 10 h at room temperature (RT).

Figure 15 shows the MLC retention with a stable evolution of the readout current versus the retention time of each storage level. This was further extrapolated to the 10 years retention time indicating a stable MLC storage. The endurance characteristics of the stored multi-levels is illustrated for a 2 bit/cell operation measured at a 300 ns pulse width at the corresponding four levels of the HSO ( $2 \times 10$  nm) ferroelectric stack. The endurance as in Figure 15 was preceded by initial wakeup cycles to achieve the MW size of an MLC 2 bit/cell storage, and this was followed by the endurance of  $10^4$  cycles. Initially, the separate 2 bit/cell levels were present up to  $10^3$  cycles and were reduced for higher cycling ranges due to the charge trapping effects causing a degradation of the lowest and highest  $V_T$  levels.



**Figure 14.** The role of ferroelectric stack lamination on (a) MW switching with a transition from instant to gradual switching, (b–c) 2 bit/cell levels for HSO (10 nm) and HZO (2 × 5 nm) illustrating narrower distributions for the HZO laminate stack; (a–c) indicates improved film granularity and lower variability induced by lamination. Reproduced with permission from [17] T. Ali et al., IEDM; published by IEEE, Copyright 2019, IEEE.



**Figure 15.** The laminate FeFET MLC retention for (a) the HSO 2 bit/cell and (b) the HZO 3 bit/cell measured to 10 h (RT) and extrapolated for the 10 years criterion, (c) The laminate MLC endurance (2 bit/cell) with  $10^4$  cycles shows  $V_T$  degradation due to charge trapping. Reproduced with permission from [17] T. Ali et al., IEDM; published by IEEE, Copyright 2019, IEEE.

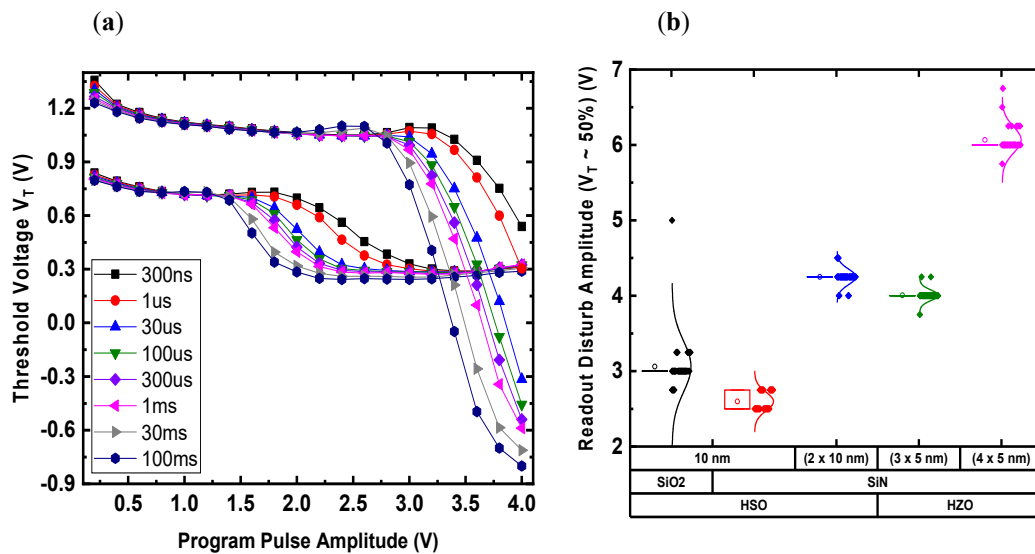
Table 1 gives an overview summary of the laminate FeFET performance in the benchmark with the recent reports on the FeFET concept compared to the Flash and RRAM concepts. The laminate FeFET concept offers a gate stack and a material engineering approach for realizing a multi-level storage solution that can extend the storage density of planar or vertical FeFETs.

**Table 1.** Benchmark of the laminate based FeFET performance parameters with recent reports of the FeFET, Flash, and RRAM concepts, Reproduced with permission from [17] T. Ali et al., IEDM; published by IEEE, Copyright 2019, IEEE.

Performance Metric	Planar FeFET [31]	Vertical FeFET [11]	This work Laminate Based MLC FeFET	Flash NAND [32]	Vertical RRAM [33]
Program Voltage	4.2 V	10 V	8 V (2b/cell), 10 V (3b/cell)	>11 V	2.8 V (MLC)
Write Time	10 ns	100 ns	300 ns	>100 $\mu$ s	100 ns
Endurance	1E5	1E4	1E4	1E4	>1E10
Retention	10 years @85 °C	10 years @85 °C	10 years @RT	10 years @85 °C	>1E4sec @125 °C
Energy per Bit	<1 fJ	<1 fJ	<1 fJ	<1 nJ	10 pJ
Bit/Cell	1	1	Up to 3	Up to 4	Up to 4

### 3.8. The Pass Voltage Disturb Effect

The high coercive field in the fluorite structure-based ferroelectrics have several advantages for the FeFET concept, particularly in terms of the maximum MW and the retention reliability. The aggressive ferroelectric thickness scaling renders the net operating voltage ( $V_c = E_c * d_F$ ) increase, upon a higher coercive field, insignificant when compared to the low coercive field perovskite structure-based ferroelectrics. Another practical consideration for the higher coercive field is the disturbance properties when the FeFET operates in a memory array configuration. The readout of a selected cell relies on the application of the pass voltage (NAND configuration) or the inhibit voltage (AND configuration) of the unselected cells. This pass voltage provokes a cell disturbance that becomes particularly critical for a stored state with an opposite polarity e.g., an ER state under a positive pass/inhibit voltage. Due to the nucleation limited switching (NLS) behavior of the fluorite structure ferroelectrics, the voltage amplitude and time can influence the cell disturbance. This characteristic is explored in Figure 16a. The ER state was initially written, the positive amplitude was screened at different times (300 ns to 100 ms) and the  $V_T$  shift toward the PG state was monitored. The classical tradeoff between the pulse amplitude and the pulse time defines the onset of the  $V_T$  shift. The laminate HSO ( $2 \times 10$  nm) showed a larger margin for the disturbance free operation compared to the same HSO material with a single 10 nm thickness. For an MFIS-based FeFET, the disturbance characteristic is a function of the interface layer type and the FE stack optimization as shown in Figure 16b. The disturbance amplitude was extracted for the onset of the 50%  $V_T$  shift (ER to PG transition). For the same FE material (HSO at 10 nm), the  $\text{SiO}_2$  IL showed a disturbance voltage that was higher compared to the SiN in line with the higher permittivity effect for the case of SiN, i.e., a higher field was present across the ferroelectric layer. The stack lamination for the same SiN-based interface layer shows higher pass disturbance voltages. For the same total ferroelectric layer thickness (20 nm), the increase in the number of lamination layers in HZO ( $4 \times 5$  nm) gave a higher voltage margin of the disturbance compared to the HSO ( $2 \times 10$  nm). The stack lamination is a tuning knob that represents tradeoffs between the increased pass/inhibit voltage disturbance margin, the operating voltage increase, and variability reduction.



**Figure 16.** The impact of the applied voltage amplitude on the disturbance characteristics of the FeFET illustrated for (a) two different stacks of HSO (10 nm) and laminate HSO ( $2 \times 10$  nm) measured at different disturbance pulse widths, (b) the onset of readout disturbance amplitude for 50%  $V_T$  (ER to PG transition), plotted versus the different stack/IL type.

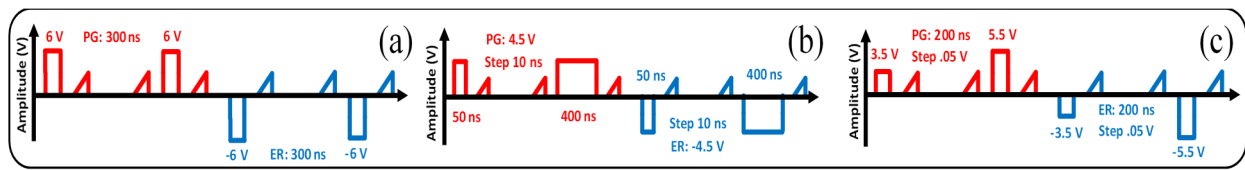
### 3.9. The Laminate FeFET-Based Synaptic Device

In biological neuro-synaptic behavior, the neurotransmitters that are released by a pre-synaptic neuron bind to the receptors of a post-synaptic neuron to modulate the flow of ions and thus the membrane potential of the post-synaptic neuron. In an excitatory/inhibitory (E/I) post-synaptic potential (PSP) process, the flow of ions generates net positive/negative charges and results in an increased/decreased membrane potential, respectively. In the simplest form, a neuron produces an output spike as the membrane potential reaches a pre-defined firing threshold potential. Although this may reflect rather deterministic behavior, the neurons can also respond in a stochastic way with a probability of a firing event, increasing with the input stimulus [34].

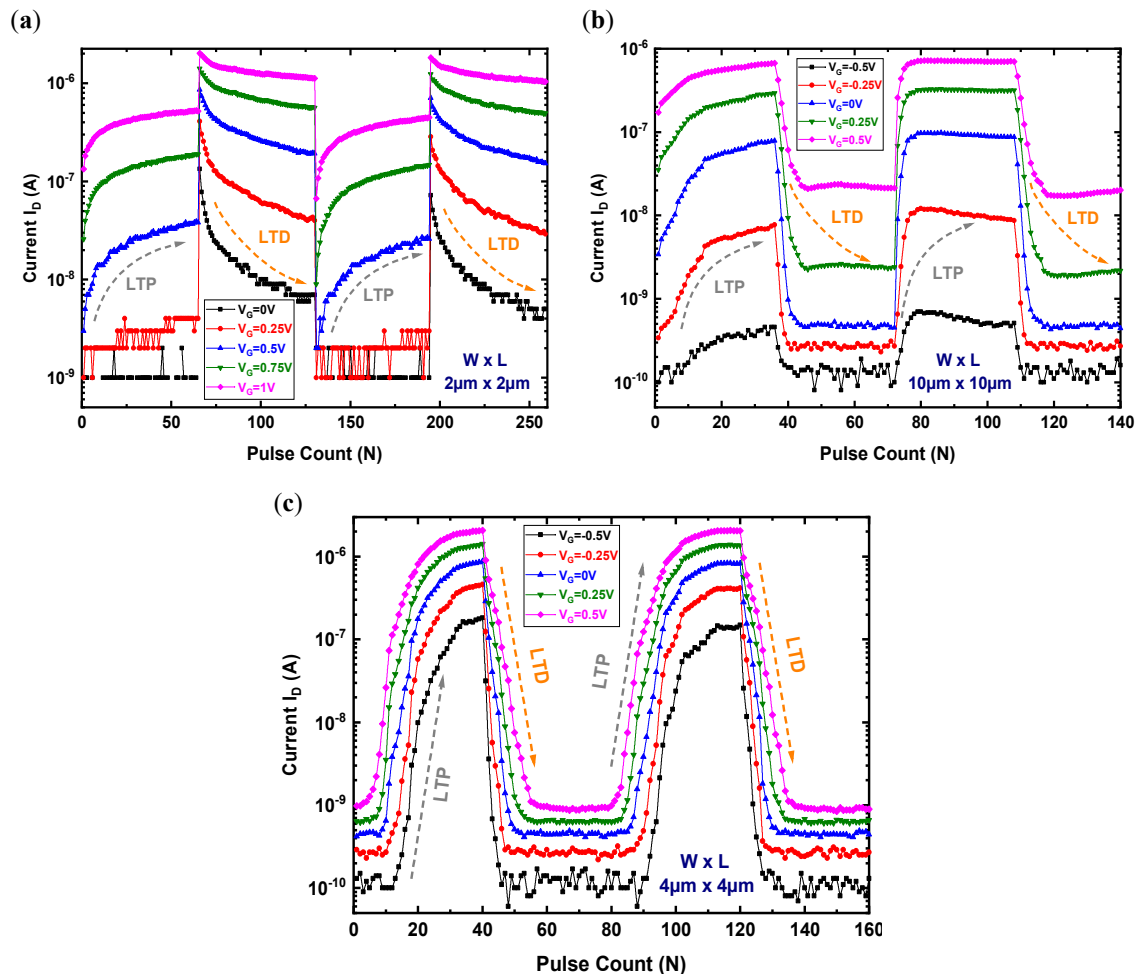
This particular feature of stochastic firing can be emulated by the scalable FeFET concept due to the instant and also stochastic switching behavior at the ultimate area scalability [18]. At the scaled area, a single grain controls the FeFET  $V_T$  where a saturated switching occurs once the threshold switching field is reached. Hence, an optimization of the FeFET considers, at the same area, a rather reduced grain count inside the ferroelectric film as well as an increased grain size to achieve the spiking-based instant switching. Practically, the FeFET scaling trend produces dimension ranges that are smaller than the achieved grain size of a ferroelectric film. However, the critical upper dimension at which the instant switching could dominate remains strongly dependent on the process optimization especially in terms of the thermal budget where the grain growth is affected [20].

In strong contrast to that aim of emulating the neuron behavior, the synaptic weight storage relies on a fine modulation of the switching polarization to achieve a controlled multi-level weight update. As opposed to the spiking-based FeFETs, the optimization for multi-level storage relies on an increased grain count and a broader texture distribution, which is partially achieved by the ferroelectric lamination. The long-term synaptic potentiation/depression (LTP/LTD) was studied for the ferroelectric HSO laminate stack ( $2 \times 10$  nm) using three different test schemes [35] as depicted in Figure 17a–c. The synaptic weight update as the current  $I_D$  versus the pulse count was plotted in Figure 18a–c for each sequence and at different set points of the  $V_G$  readout. The measurement sequence of the LTP/LTD emulation was applied twice for the reproducible current trend.





**Figure 17.** The different types of measurement test sequences for emulating the synaptic weight update in FeFET as (a) PG/ER pulse train at a constant amplitude and pulse width, (b) a constant amplitude sequence  $|4.5 \text{ V}|$  with incremental pulse widths in 10 ns steps, (c) a constant pulse width sequence (200 ns) with incremental pulse amplitudes in 50 mV steps.

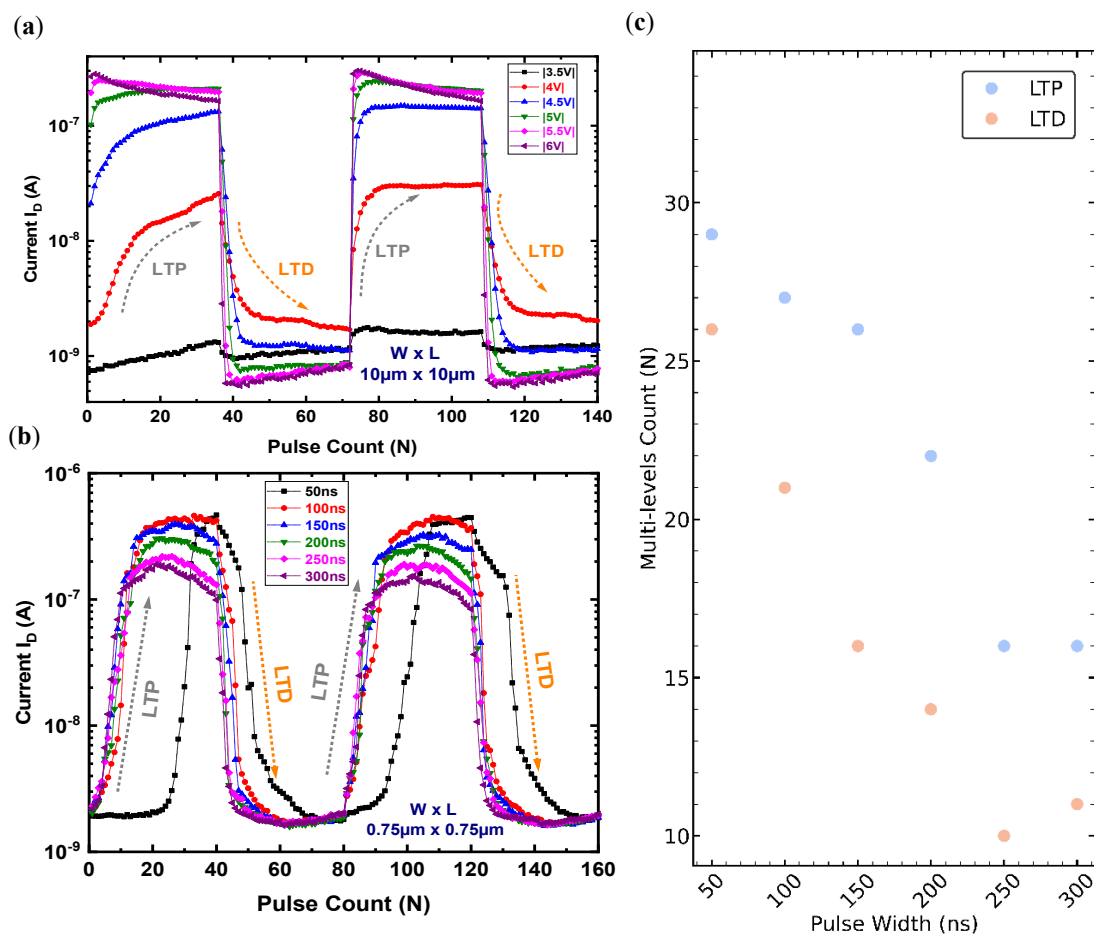


**Figure 18.** The laminar FeFET as a synaptic device shown by two cycles of the LTP/LTD operation using (a) PG/ER pulse train (sequence 1), (b) constant amplitude for the pulse width sweep (sequence 2), (c) constant pulse width for an amplitude sweep (sequence 3).

In the first sequence, a PG/ER pulse train using an amplitude of  $|6 \text{ V}|$ , 300 ns was applied. This condition was lower than the one used for the saturated switching. Based on the accumulative switching behavior of the ferroelectric materials, the LTP/LTD as shown in Figure 18a reflected a  $V_T$  decrease/increase, and thus produced an increase/decrease in the current, respectively. The LTP/LTD can similarly be achieved using the second sequence (Figure 17b) where the pulse width sweep (50 ns to 400 ns) at a constant amplitude  $|4.5 \text{ V}|$  was used to modulate the current as shown in Figure 18b. A similarity in the trends of Figure 18b is related to the dynamic range of current modulation as well as the current magnitude in relation to the set point of the  $V_G$  readout. An increase in the  $V_G$  readout shows a systematic shift of the full LTP/LTD curves toward higher current values. Likewise, the dynamic range of the current modulation decreased as the  $V_G$  readout increased. Both

the LTP/LTD trends in Figure 18b reflect a narrow FeFET switching window as per the LTP/LTD pulse conditions applied where a limited field has unsaturated ferroelectric switching, as is visible in the limited maximum of the dynamic current range.

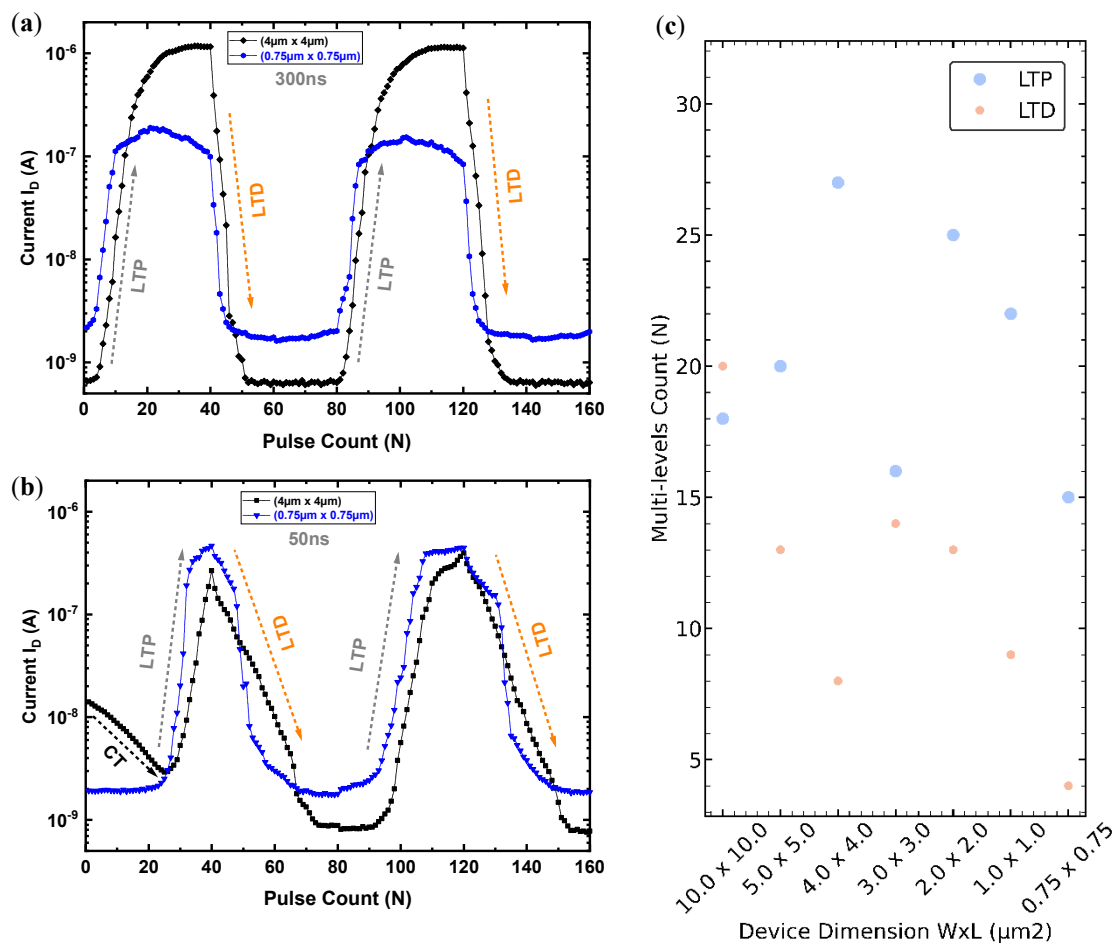
As the third sequence, the pulse amplitude sweep was used in Figure 17c at a constant pulse width (200 ns) to capture the full window of the LTP/LTD as shown in Figure 18c for the different  $V_G$  readout. The fine increase in the amplitude generated an increased number of levels with approximately three orders of magnitude current change, and the effective increase in levels with the amplitude was consistent with the ferroelectric stack lamination. Although the second and third sequences of LTP/LTD in Figure 18b,c were studied at a constant selected pulse amplitude (|4.5 V|) or pulse width (200 ns), the impact of different amplitudes or pulse widths can be illustrated in Figure 19a,b for each sequence, respectively. For the second sequence, the pulse amplitude sweep had, as was outlined earlier, an increase in the current dynamic range as the amplitude increases (e.g., |4 V|, |4.5 V|) shown in Figure 19a. At higher amplitudes such as |6 V|, a decrease in the saturation current reflects a dominant charge trapping effect that prevails over the saturated ferroelectric switching. Although to a lesser extent, a similar effect was present for the third sequence at the different values of the constant pulse width (50 ns to 300 ns) in Figure 19b. Importantly, at a shorter pulse width such as 50 ns, a higher amplitude and hence a higher pulse count was needed to cause a current modulation i.e., ferroelectric switching. This is due to the tradeoff between the field and time-dependent ferroelectric switching [36]. Hence, the LTP/LTD curve of the 50 ns pulse width was relatively shifted in Figure 19b to a higher pulse count.



**Figure 19.** The FeFET synaptic LTP/LTD using (a) different amplitude conditions for the pulse width sweep (sequence 2), (b) different pulse width conditions for the amplitude sweep (sequence 3), (c) the impact of the pulse width sweep in sequence 3 on the multi-levels count.

Although the higher pulse width ( $>50$  ns) appears indifferent in the LTP/LTD trend of Figure 19b, an extraction of the multi-level count gives a rather valuable insight. The multi-levels were counted at 1 nA search resolution of the second LTP/LTD cycle while excluding the low and high current saturation ranges (Figure 19b). The impact of varying the write pulse width of the third sequence is shown in Figure 19c where the maximum number of achieved levels is inversely proportional to the pulse width. At the 50 ns pulse width, the multi-level count was at a maximum and decreased toward the 300 ns conditions. This reveals that the sequence type, pulse amplitude, and pulse width conditions have different switching dynamics of the ferroelectric material and ultimately affect the LTP/LTD response shape as well as the multi-level count.

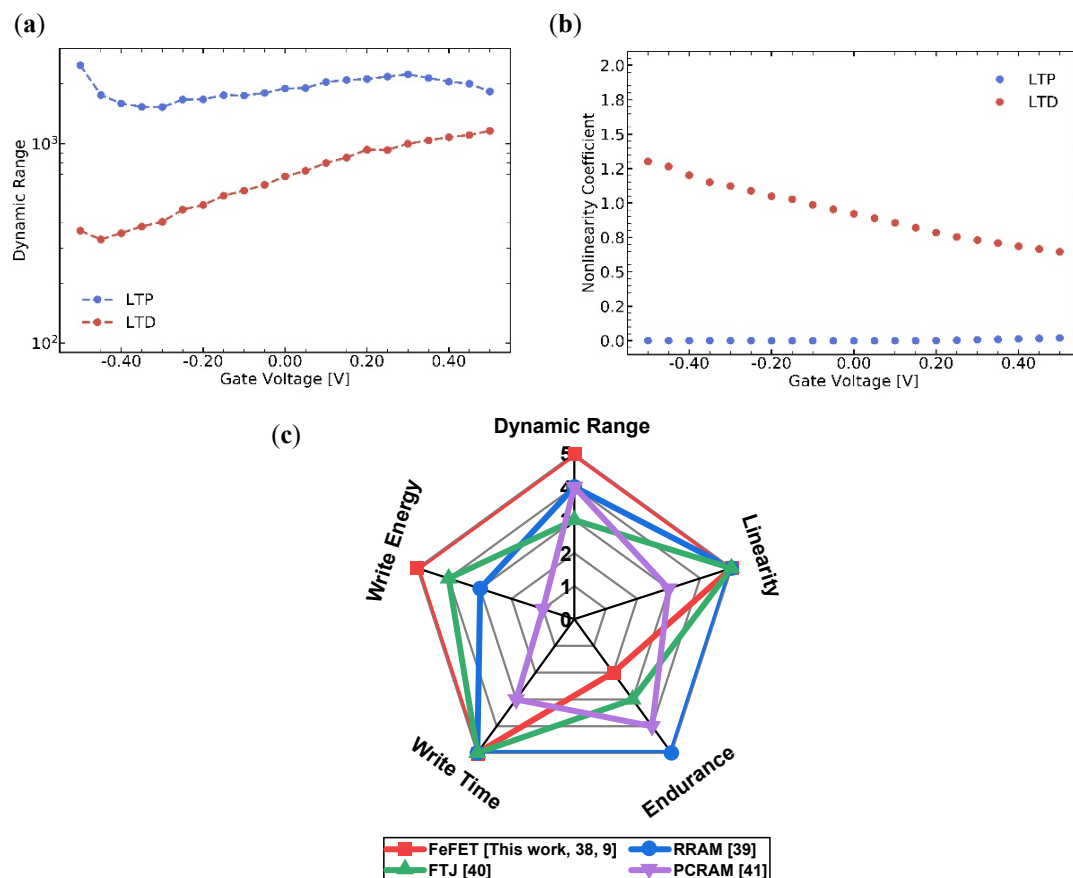
Additionally, the LTP/LTD multi-levels count was proportional to the area as in Figure 20c with the dimension sweep from  $(10\ \mu\text{m} \times 10\ \mu\text{m})$  to  $(0.75\ \mu\text{m} \times 0.75\ \mu\text{m})$  indicating a decrease in the multi-levels count. The impact of the pulse width and the area can be further summarized in Figure 20a,b by the comparison of selected devices  $(4\ \mu\text{m} \times 4\ \mu\text{m})$  versus  $(0.75\ \mu\text{m} \times 0.75\ \mu\text{m})$  at the 50 ns and 300 ns pulse width conditions. Although the multi-levels count declined as the area shrank, the clear advantage of the ferroelectric stack lamination appears in the actual presence of these intermediate levels in comparison to the instant switching behavior as indicated earlier in Figure 14a. This one aspect of ferroelectric stack optimization indicates the possible variability reduction in scaled FeFET devices.



**Figure 20.** The comparison of the FeFET synaptic LTP/LTD using the pulse amplitude-based sequence 3 at two different pulse widths (a) 300 ns and (b) 50 ns shown for large  $(4\ \mu\text{m} \times 4\ \mu\text{m})$  versus small  $(0.75\ \mu\text{m} \times 0.75\ \mu\text{m})$  device dimensions, (c) the multi-level count versus the device dimension sweep.

### 3.10. The Laminate FeFET Based Synaptic Metrics

An optimal electronic synapse is characterized by certain performance criteria. These are stated in terms of the LTP/LTD maximum dynamic range (DR) and nonlinearity coefficients. An ideal synapse has extremely linear and symmetric LTP/LTD responses at maximized  $I_{\text{on}}$  to  $I_{\text{off}}$  current ratios i.e., the weight update covers a wide DR. The FeFET synaptic LTP/LTD can be characterized based on a fitting model as proposed by Yu et al. for extracting the nonlinearity coefficient  $\alpha$  [37]. For a FeFET-based synapse, the DR and nonlinearity becomes a function of the readout voltage as shown in Figure 21a,b. The DR and nonlinearity coefficients were extracted from the synaptic LTP/LTD that was measured using the amplitude-based sequence as shown earlier in Figure 18c. The DR was extracted as the weight ratio between the LTP/LTD current measured after the first and final pulse of the sequence in Figure 17c. The LTP showed a higher DR compared to the LTD one in the current transition in Figure 18c. For a symmetric synaptic response, the DR becomes equal for the LTP/LTD operation. The LTP in Figure 21b shows excellent linearity whereas in the LTD case, the linearity improves as the readout voltage increases. The linearity coefficient dependence on the readout voltage is directly linked to the different operation regime of the FeFET  $I_D$ - $V_G$ . For a higher readout voltage, the improved linearity reflects a gradual response at an even current  $I_D$ - $V_G$  shift for the ER pulse amplitude increase. The FeFET concept [9,38] is compared in Figure 21c with other technologies [39–41]. The high dynamic range, low energy, and linearity are among the key merits of using the FeFET as a synaptic device.



**Figure 21.** The synaptic LTP and LTD figure of merits as (a) the dynamic range and (b) nonlinearity coefficients versus the readout voltage; the DR and nonlinearity were extracted from the synaptic LTP/LTD measured using the amplitude-based sequence (Figure 17c for the 200 ns pulse width) on the device dimension ( $4 \mu\text{m} \times 4 \mu\text{m}$ ), (c) benchmark of the different technology candidates for the synapse performance metrics.

#### 4. Conclusions

The effect and merits of the ferroelectric layer lamination in HSO and HZO materials for FeFET applications has been reported. The HSO and HZO ferroelectric laminations enable a thickness-independent FE stack operation by stabilizing the optimal ferroelectric phase at higher ferroelectric layer thicknesses. The increase in the ferroelectric layer thickness at the optimal ferroelectric phase via lamination enables a maximized memory window size for reliable multi-level coding storage. The FeFET operation shows for the different stack types a promising multi-level coding operation as a 1–3 bit/cell with a memory window that varies up to a maximum of 3.5 V. The multi-level coding operation shows a stable multi-level room temperature retention of 10 h that was further extrapolated to 10 years. The multi-level endurance of the 2 bit/cell was illustrated up to 104 cycles, when the endurance becomes limited by the interference between the storage levels due to the charge trapping effect. The HSO and HZO materials indicated distinct differences in response to the lamination in terms of wakeup, variability, and charge trapping. The HSO material showed a stronger wake-up effect where extended cycles were necessary to achieve full wake-up. The HSO material showed a higher variability of the pristine and post wakeup operation compared to the HZO ones. Overall, the FE lamination enabled increased intermediate switching levels and suppressed the instant switching behavior upon scaled device dimension, thus serving to reduce the device variability. This improvement is particularly useful for emulating the synaptic potentiation and depression. The laminate stacks were studied in terms of the long-term potentiation and depression with respect to the optimal pulsing conditions and area dependence.

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